15A Sink/Source, Single-Channel, Reinforced Isolated SiC/IGBT Gate Driver with Active Protection

1. Features

- **15A Peak Sink Current and 15A Peak Source Current**
- **OUTH and OUTL Split Outputs**
- **Drive High-power SiC MOSFET and IGBT with up to 2121 V_{PK} Operating Voltage**
- **Up to 33V Output Drive Supply Range(V_{DD}-V_{EE}) with 12V VDD UVLO Detection and Power-Good Indication RDY**
- **Robust Galvanic Isolation**
  - High lifetime: >40 years
  - Up to 5.7kV_{RMS} isolation rating
  - Common-mode transient immunity (CMTI) > ±150V/ns
- **Input Features Fast Transient/Pulse Reject (< 40ns, typical)**
- **Integrated Desaturation (DESAT) Protection with 200ns Fast-Response**
- **4A Internal Active Miller Clamp**
- **Inputs and Outputs Features up to 5V Over-shoot/Under-shoot Transient Immunity**
- **Shoot Through Protection(CA-IS3215S_ and CA-IS3216S_ only)**
- **Fast Disable/Enable Control ($\overline{RST}$/EN)**
- **Over-current Alarm $\overline{FLT}$ and Reset from $\overline{RST}$/EN**
- **Propagation Delay :**
  - 130ns propagation delay (maximum)
  - 30ns pulse skew
  - 30ns part to part skew (maximum)
- **400mA (IGBT)/1A (SiC) Soft turn-off Current during Fault Occurs**
- **16-pin Wide-body SOIC Package with Creepage and Clearance >8mm**
- **-40°C to +150°C Operating Junction Temperature (T_J) Range**
- **Safety regulatory approvals**
  - VDE Reinforced isolation and Basic isolation per DIN EN IEC 60747-17 (VDE 0884-17): 2021-10
  - UL certification per UL 1577 for 1 minute
  - CQC certification per GB 4943.1-2022
  - TUV certification
- **Reliability certification:**
  - AEC-Q100, Grade 1

2. Applications

- HEV and EV Traction Inverter
- On Board Charger (OBC)
- Automotive High-voltage DC-DC Convertor

3. General Description

The CA-IS3215/6 devices are a family of single-channel reinforced isolated gate driver capable of sinking 15A and sourcing 15A peak-current. These devices operate with dual supplies or a single supply of up to 33V wide voltage range of V_{DD} - V_{EE}, making them ideal to drive high-power MOSFET, IGBT or silicon-carbide(SiC) transistors in various inverter, motor control or isolated power supply systems. The CA-IS3215/6 gate drivers integrate extensive active protection, such as active Miller clamp, UVLO detection on both control-side and driver-side supply, over-current and short-circuit fault alarm and protection, to optimize SiC and IGBT control and improve system reliability.

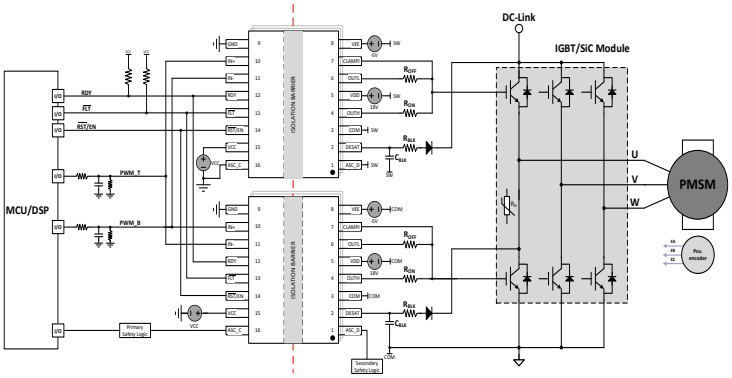
All devices have integrated digital galvanic isolation between control-side and driver-side using Chipanalog's proprietary SiO_2 capacitive isolation technology which features isolation for a withstand voltage rating of up to 5.7kV_{RMS} for 60 seconds with minimum common-mode transient immunity (CMTI) of 150V/ns, support up to 1500V_{RMS} isolation working voltage and 12.8kV_{PK} surge rating.

The CA-IS3215/6 devices are available in a 16-pin wide-body SOIC package with creepage and clearance > 8mm. All devices are rated for operation at junction temperatures of -40°C to +150°C. Higher operation temperature range extends gate driver designs in the industrial and automotive applications.

Device Information

Part Number	Package	Package Size (Nominal Value)
CA-IS3215xxW-Q1	SOIC16-WB(W)	10.3mm x 7.5mm
CA-IS3216xxW-Q1	SOIC16-WB(W)	10.3mm x 7.5mm

Simplified Schematic



4. Ordering Information

Table 4-1. Ordering Information

Part #	Power Switch	DESAT Threshold	Soft turn-off Current	Dead-time for Shoot Through Protection	Internal/External Clamp	Package
CA-IS3215NNW-Q1	IGBT	9 V	400 mA	N.A.	CLAMPI	SOIC16-WB(W)
CA-IS3215LNW-Q1	IGBT	9 V	400 mA	N.A.	CLAMPI	SOIC16-WB(W)
CA-IS3215ENW-Q1	IGBT	9 V	400 mA	N.A.	CLAMPI	SOIC16-WB(W)
CA-IS3215VNW-Q1	IGBT	9 V	400 mA	N.A.	CLAMPI	SOIC16-WB(W)
CA-IS3215NEW-Q1	IGBT	9 V	400 mA	N.A.	CLAMPE	SOIC16-WB(W)
CA-IS3215SNW-Q1	IGBT	9 V	400 mA	800 ns	CLAMPI	SOIC16-WB(W)
CA-IS3215SEW-Q1	IGBT	9 V	400 mA	800 ns	CLAMPE	SOIC16-WB(W)
CA-IS3216NNW-Q1	SiC	6 V	1 A	N.A.	CLAMPI	SOIC16-WB(W)
CA-IS3216NEW-Q1	SiC	6 V	1 A	N.A.	CLAMPE	SOIC16-WB(W)
CA-IS3216SNW-Q1	SiC	6 V	1 A	140 ns	CLAMPI	SOIC16-WB(W)
CA-IS3216SEW-Q1	SiC	6 V	1 A	140 ns	CLAMPE	SOIC16-WB(W)

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5. Pin Configuration and Description

5.1. CA-IS321xNNW-Q1 and CA-IS321xSNW-Q1 Pin Configuration and Description

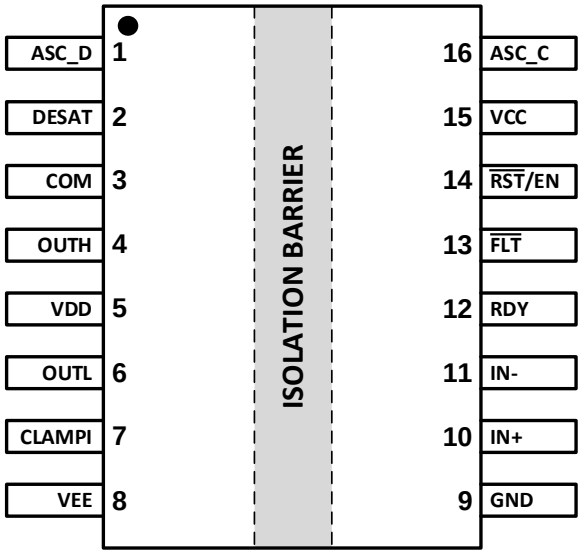


Figure 5-1 CA-IS321xNNW-Q1/ CA-IS321xSNW-Q1 Pin Configuration

Table 5-1 Pin Description

Pin Name	Pin Number	Type[1]	Description
ASC_D	1	I	Active short circuit (ASC) control input (active high) for driver-side. Drive ASC_D high to initial the ASC protection and force the driver output to high-level during fault occurs. Connect this pin to COM if not used.
DESAT	2	I	Desaturation protection input.
COM	3	P	Gate driver common pin. Connect COM to external IGBT's emitter pin or SiC MOSFET's source pin.
OUTH	4	O	Positive gate drive output.
VDD	5	P	Positive power supply input for gate driver. Bypass VDD to COM with at least 10μF capacitor as close as possible to the pin VDD.
OUTL	6	O	Negative gate drive output.
CLAMPI	7	I	Internal active Miller clamp input. Connect CLAMPI to the gate of the power MOSFET.
VEE	8	P	Negative power supply input for gate driver. Bypass VEE to COM with at least 10μF capacitor as close as possible to the pin VEE.
GND	9	G	Ground reference for control-side.
IN+	10	I	Non-inverting driver input on control-side. It has internal pulldown to GND.
IN–	11	I	Inverting driver input on control-side. It has internal pullup to VCC.
RDY	12	O	Active-high, open-drain, power-good output. RDY goes high when VCC and VDD are both above their respective UVLO thresholds, indicating that the device is powered up and ready for operation.
$\overline{\text{FLT}}$	13	O	Active-low, open-drain output fault indicator. $\overline{\text{FLT}}$ goes low to indicate that over-current or short-circuit fault occurs.
$\overline{\text{RST}}$/EN	14	I	Reset and enable control input. $\overline{\text{RST}}$/EN has internal pulldown. 1) Enable /Shutdown control for driver-side. Put $\overline{\text{RST}}$/EN low to turn-off the external power transistors; 2) Resets the desaturation condition indicator output at pin $\overline{\text{FLT}}$. Put $\overline{\text{RST}}$/EN to low for more than 800ns, assert $\overline{\text{FLT}}$ reset at the rising edge of $\overline{\text{RST}}$/EN and reset DESAT fault indication latch at pin $\overline{\text{FLT}}$.
VCC	15	P	3.0V o 5.5V power supply input for control-side. Bypass VCC to GND with at least 1μF ceramic capacitor as close as possible to VCC pin.
ASC_C	16	I	Active short circuit (ASC) input for control-side. ASC_C has internal pulldown. If ASC_C is high, OUTH/OUTL is pulled high. If ASC_C is low, the OUTH/OUTL pins follow the IN+ and IN_ pin logical truth table, see Table 8-1. Connect ASC_C to GND if not used.

Note:
1. P = power supply, G = GND, I = input, O = output

5.2. CA-IS3215LNW-Q1 and CA-IS3215ENW-Q1 Pin Configuration and Description

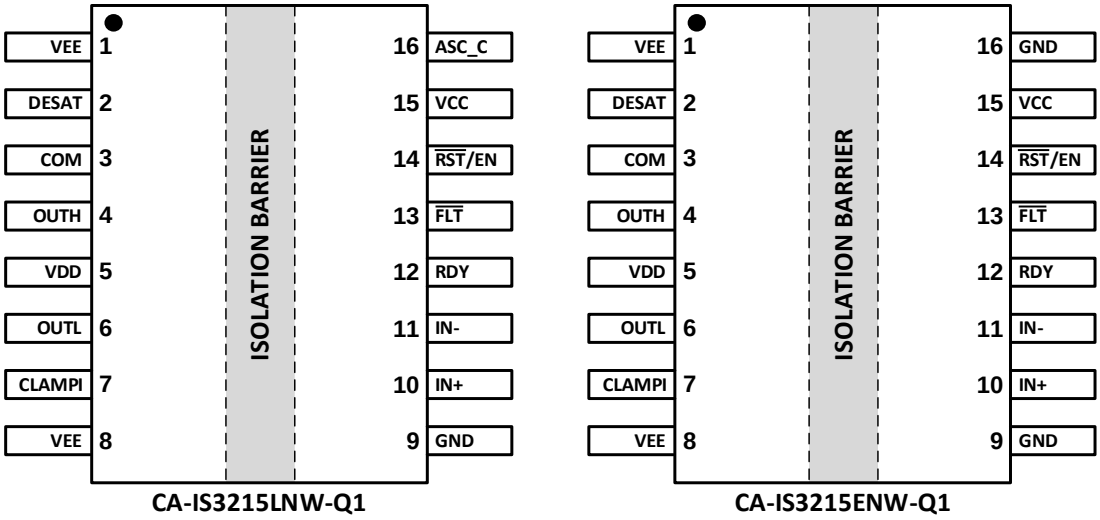


Figure 5-2 CA-IS3215LNW-Q1 and CA-IS3215ENW-Q1 Pin Configuration

Table 5-2 Pin Description

Pin Name	Pin Number		Type[1]	Description
	CA-IS3215LNW	CA-IS3215ENW		
DESAT	2	2	I	Desaturation protection input.
COM	3	3	P	Gate driver common pin. Connect COM to external IGBT's emitter pin or SiC MOSFET's source pin.
OUTH	4	4	O	Positive gate drive output.
VDD	5	5	P	Positive power supply input for gate driver. Bypass VDD to COM with at least 10μF capacitor as close as possible to the pin VDD.
OUTL	6	6	O	Negative gate drive output.
CLAMPI	7	7	I	Internal active Miller clamp input. Connect CLAMPI to the gate of the power MOSFET.
VEE	1, 8	1, 8	P	Negative power supply input for gate driver. Bypass VEE to COM with at least 10μF capacitor as close as possible to the pin VEE.
GND	9	9, 16	G	Ground reference for control-side.
IN+	10	10	I	Non-inverting driver input on control-side. It has internal pulldown to GND.
IN–	11	11	I	Inverting driver input on control-side. It has internal pullup to VCC.
RDY	12	12	O	Active-high, open-drain, power-good output. RDY goes high when VCC and VDD are both above their respective UVLO thresholds, indicating that the device is powered up and ready for operation.
$\overline{\text{FLT}}$	13	13	O	Active-low, open-drain output fault indicator. $\overline{\text{FLT}}$ goes low to indicate that over-current or short-circuit fault occurs.
$\overline{\text{RST}}$/EN	14	14	I	Reset and enable control input. $\overline{\text{RST}}$/EN has internal pulldown. 3) Enable /Shutdown control for driver-side. Put $\overline{\text{RST}}$/EN low to turn-off the external power transistors; 4) Resets the desaturation condition indicator output at pin $\overline{\text{FLT}}$. Put $\overline{\text{RST}}$/EN to low for more than 800ns, assert $\overline{\text{FLT}}$ reset at the rising edge of $\overline{\text{RST}}$/EN and reset DESAT fault indication latch at pin $\overline{\text{FLT}}$.
VCC	15	15	P	3.0V o 5.5V power supply input for control-side. Bypass VCC to GND with at least 1μF ceramic capacitor as close as possible to VCC pin.
ASC_C	16	-	I	Active short circuit (ASC) input for control-side. ASC_C has internal pulldown. If ASC_C is high, OUTH/OUTL is pulled high. If ASC_C is low, the OUTH/OUTL pins follow the IN+ and IN_ pin logical truth table, see Table 8-1. Connect ASC_C to GND if not used.

Note:
1. P = power supply, G = GND, I = input, O = output

5.3. CA-IS3215VNW-Q1 Pin Configuration and Description

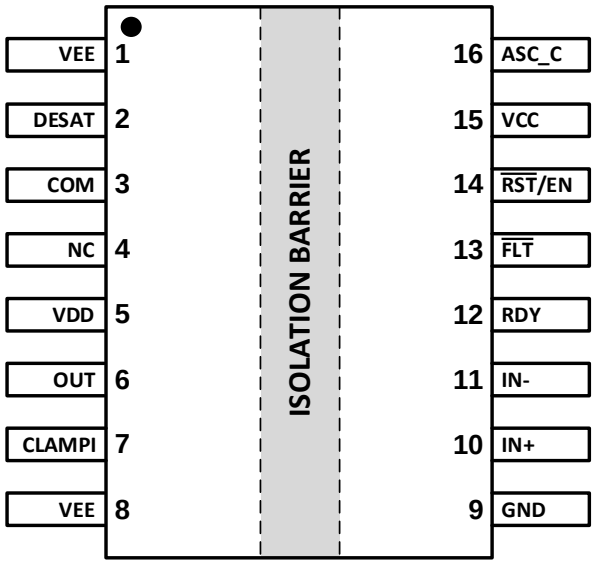


Figure 5-3 CA-IS3215VNW-Q1 Pin Configuration

Table 5-3 Pin Description

Pin Name	Pin Number	Type[1]	Description
DESAT	2	I	Desaturation protection input.
COM	3	P	Gate driver common pin. Connect COM to external IGBT's emitter pin or SiC MOSFET's source pin.
NC	4	-	Not connection
VDD	5	P	Positive power supply input for gate driver. Bypass VDD to COM with at least 10μF capacitor as close as possible to the pin VDD.
OUT	6	O	Gate drive output.
CLAMPI	7	I	Internal active Miller clamp input. Connect CLAMPI to the gate of the power MOSFET.
VEE	1, 8	P	Negative power supply input for gate driver. Bypass VEE to COM with at least 10μF capacitor as close as possible to the pin VEE.
GND	9	G	Ground reference for control-side.
IN+	10	I	Non-inverting driver input on control-side. It has internal pulldown to GND.
IN–	11	I	Inverting driver input on control-side. It has internal pullup to VCC.
RDY	12	O	Active-high, open-drain, power-good output. RDY goes high when VCC and VDD are both above their respective UVLO thresholds, indicating that the device is powered up and ready for operation.
$\overline{\text{FLT}}$	13	O	Active-low, open-drain output fault indicator. $\overline{\text{FLT}}$ goes low to indicate that over-current or short-circuit fault occurs.
$\overline{\text{RST}}$/EN	14	I	Reset and enable control input. $\overline{\text{RST}}$/EN has internal pulldown. 5) Enable /Shutdown control for driver-side. Put $\overline{\text{RST}}$/EN low to turn-off the external power transistors; 6) Resets the desaturation condition indicator output at pin $\overline{\text{FLT}}$. Put $\overline{\text{RST}}$/EN to low for more than 800ns, assert $\overline{\text{FLT}}$ reset at the rising edge of $\overline{\text{RST}}$/EN and reset DESAT fault indication latch at pin $\overline{\text{FLT}}$.
VCC	15	P	3.0V o 5.5V power supply input for control-side. Bypass VCC to GND with at least 1μF ceramic capacitor as close as possible to VCC pin.
ASC_C	16	I	Active short circuit (ASC) input for control-side. ASC_C has internal pulldown. If ASC_C is high, OUTH/OUTL is pulled high. If ASC_C is low, the OUTH/OUTL pins follow the IN+ and IN_ pin logical truth table, see Table 8-1. Connect ASC_C to GND if not used.

Note:
1. P = power supply, G = GND, I = input, O = output

5.4. CA-IS321xNEW-Q1 and CA-IS321xSEW-Q1Pin Configuration and Description

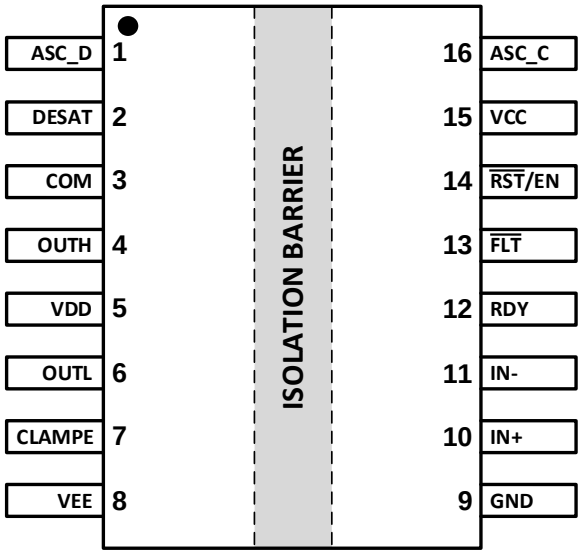


Figure 5-4 CA-IS321xNEW-Q1/ CA-IS321xSEW-Q1 Pin Configuration

Table 5-4 Pin Description

Pin Name	Pin Number	Type[1]	Description
ASC_D	1	I	Active short circuit (ASC) control input (active high) for driver-side. Drive ASC_D high to initial the ASC function and force the driver output to high-level during fault occurs. Connect this pin to COM if not used.
DESAT	2	I	Desaturation protection input.
COM	3	P	Gate driver common pin. Connect COM to the IGBT's emitter pin or SiC MOSFET's source pin.
OUTH	4	O	Positive gate drive output.
VDD	5	P	Positive power supply input for gate driver. Bypass VDD to COM with at least 10μF capacitor as close as possible to the pin VDD.
OUTL	6	O	Negative gate drive output.
CLAMPE	7	O	External active Miller clamp input. Connect CLAMPE to the gate of the external Miller clamp MOSFET. Leave this pin float if not used.
VEE	8	P	Negative power supply input for gate driver. Bypass VEE to COM with at least 10μF capacitor as close as possible to the pin VEE.
GND	9	G	Ground reference for control-side.
IN+	10	I	Non-inverting driver input on control-side. It has internal pulldown to GND.
IN–	11	I	Inverting driver input on control-side. It has internal pullup to VCC.
RDY	12	O	Active-high, open-drain, power-good output. RDY goes high when VCC and VDD are both above their respective UVLO thresholds, indicating that the device is powered up and ready for operation.
$\overline{\text{FLT}}$	13	O	Active-low, open-drain output fault indicator. $\overline{\text{FLT}}$ goes low to indicate that over-current or short-circuit fault occurs.
$\overline{\text{RST}}$/EN	14	I	Reset and enable control input. $\overline{\text{RST}}$/EN has internal pulldown. 1) Enable /Shutdown control for driver-side. Put $\overline{\text{RST}}$/EN low to turn-off the external power transistors; 2) Resets the desaturation condition indicator output at pin $\overline{\text{FLT}}$. Put $\overline{\text{RST}}$/EN to low for more than 800ns, assert $\overline{\text{FLT}}$ reset at the rising edge of $\overline{\text{RST}}$/EN and reset DESAT fault indication latch at pin $\overline{\text{FLT}}$.
VCC	15	P	3.0V o 5.5V power supply input for control-side. Bypass VCC to GND with at least 1μF ceramic capacitor as close as possible to VCC pin.
ASC_C	16	I	Active short circuit (ASC) input for control-side. ASC_C has internal pulldown. If ASC_C is high, OUTH/OUTL is pulled high. If ASC_C is low, the OUTH/OUTL pins follow the IN+ and IN_ pin logical truth table, see Table 8-1. Connect ASC_C to GND if not used.

Note:
1. P = power supply, G = GND, I = input, O = output

6. Specifications

6.1. Absolute Maximum Ratings[1]

Over operating free-air temperature range unless otherwise specified.

Parameters		Minimum	Maximum	Unit
VCC	VCC–GND	–0.3	6	V
VDD	VDD–COM	–0.3	36	V
VEE	VEE–COM	–17.5	0.3	V
V_{MAX}	VDD–VEE	–0.3	36	V
IN+, IN–, $\overline{RST}$/EN, ASC_C	DC	GND–0.3	VCC	V
DESAT	Referenced to COM	COM–0.3	VDD+0.3	V
ASC_D	Referenced to COM	–0.3	VDD+0.3	V
OUTH, OUTL, CLAMPI	DC	VEE–0.3	VDD	V
RDY, $\overline{FLT}$		GND–0.3	VCC	V
$I_{\overline{FLT}}$, I_{RDY}	Input current for pin $\overline{FLT}$ and pin RDY		20	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. Bench test result.

6.2. ESD Ratings

			Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per AEC-Q100-002[1]		±3000	V
	Charged device model (CDM), per AEC-Q100-01		±2000	

Note:

1. AEC Q100-002 indicates that HBM stressing should comply with ANSI/ESDA/JEDEC JS-001 specifications.

6.3. Recommended Operating Conditions

Over operating free-air temperature range unless otherwise specified.

Parameters			Minimum	Maximum	Unit
VCC	VCC–GND		3.0	5.5	V
VDD	VDD–COM		13	33	V
VMAX	VDD–VEE		–	33	V
IN+, IN–, $\overline{RST}$/EN, ASC_C	Referenced to GND.	Logic-high input	0.7xV_{CC}	V_{CC}	V
		Logic-low input	0	0.3×V_{CC}	
ASC_D	Referenced to COM.		0	5.5	V
$t_{RST/EN}$	Fault-latch reset pulse width		800		ns
T_A	Junction temperature		–40	125	°C
T_J	Ambient temperature		–40	150	°C

6.4. Thermal Information

Thermal Metric		SOIC16-WB	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	°C/W

6.5. Power Ratings

Parameters		Test Conditions	Typical Value	Unit
P_D	Maximum input and output power dissipation	VCC=5V, VDD–COM=20V, COM–VEE=5V, IN+/IN– = 5V, 150kHz square wave with 50% duty cycle, C_L = 10nF, T_A=25°C	982.5	mW
P_{D1}	Maximum input power dissipation		17.5	mW
P_{D2}	Maximum output power dissipation		965	mW

6.6. Insulation Specifications

Parameters		Test Conditions	Specifications W	Unit
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 24	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)； IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) [2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification);	8000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	9600	
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	9846	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification) 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~1	pF
R_{IO}	Isolation resistance, input to output[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5700	V_{RMS}

Notes:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

6.7. Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17: 2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2022	Certified according to EN IEC 62368-1:2020 +A11 and EN61010-1: 2010+A1
Reinforced isolation(SOIC16-WB): V_{IOTM}: 8000 V_{pk} V_{IORM}: 2121 V_{pk} V_{IOSM}: 12800 V_{pk}	Protection voltage: SOIC16-WB: 5.7 kV_{RMS}	SOIC16-WB: Reinforced (Altitude ≤ 5000 m)	EN IEC 62368-1: SOIC16-WB: 5.7 kV_{RMS} EN61010-1: SOIC16-WB: 5.7 kV_{RMS}
Certificate number: 40057278 CA-IS3215ENW-Q1：Pending	Certificate number: E511334 CA-IS3215ENW-Q1：Pending	Certificate number: CQC23001406424 CA-IS3215ENW-Q1：Pending	Client reference number: 2253313 CA-IS3215ENW-Q1：Pending

6.8. Safety Limits

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Safety input, output or supply current	$R_{\theta JA}$=68.3°C/W, VDD=15V, VEE=–5V, T_J=150°C, T_A=25°C			61	mA
		$R_{\theta JA}$=68.3°C/W, VDD=20V, VEE=–5V, T_J=150°C, T_A=25°C			49	
P_S	Safety power dissipation	$R_{\theta JA}$=68.3°C/W, VDD=20V, VEE=–5V, T_J=150°C, T_A=25°C			1200	mW
T_S	Maximum safety temperature				150	°C

6.9. Electrical Characteristics

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.[1, 2]

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
VCC UVLO threshold and delay						
V_{VCC_ON}	VCC raising	VCC–GND	2.55	2.7	2.85	V
V_{VCC_OFF}	VCC falling		2.35	2.5	2.65	
V_{VCC_HYS}	Undervoltage-lockout threshold hysteresis			0.2		
t_{VCCFIL}	VCC UVLO detection deglitch time			5		μs
$t_{VCC+ \text{ to } OUT}$	VCC power up delay, UVLO raising to output high	IN+=VCC, IN–=GND		30	70	
$t_{VCC- \text{ to } OUT}$	VCC power down delay, UVLO falling to output low			7	15	
$t_{VCC+ \text{ to } RDY}$	VCC power up delay, UVLO raising to RDY high	$\overline{RST}$/EN=VCC		30	70	
$t_{VCC- \text{ to } RDY}$	VCC power down delay, UVLO falling to RDY low			7	15	
$t_{VCC0 \text{ to } RDY}$	VCC power on from 0V, to RDY high	$\overline{RST}$/EN=VCC, VCC power up from 0V		150		
VDD UVLO threshold and delay						
V_{VDD_ON}	VDD raising	VDD–COM	11.0	12.0	13.0	V
V_{VDD_OFF}	VDD falling		10.0	11.0	12.0	
V_{VDD_HYS}	Undervoltage-lockout threshold hysteresis			1.0		
t_{VDDFIL}	VDD UVLO detection deglitch time			5		μs
$t_{VDD+ \text{ to } OUT}$	VDD power up delay, UVLO raising to output high	IN+=VCC, IN–=GND		7	15	
$t_{VDD- \text{ to } OUT}$	VDD power down delay, UVLO falling to output low			7	15	
$t_{VDD+ \text{ to } RDY}$	VDD power up delay, UVLO raising to RDY high	$\overline{RST}$/EN=VCC		7	15	
$t_{VDD- \text{ to } RDY}$	VDD power down delay, UVLO falling to RDY low			7	15	
$t_{VDD0 \text{ to } RDY}$	VDD power on from 0V to RDY high	VDD power up from 0V		100		
VCC, VDD supply current						
I_{VCCQ}	V_{CC} quiescent current	OUT(H)=high	1.4	2.3	3.5	mA
		OUT(L)=low	0.8	1.5	2.3	
I_{VDDQ}	V_{DD} quiescent current	OUT=high/low	2.5	3.7	5.3	
I_{VEEQ}	V_{EE} quiescent current	OUT=High/Low	2.1	3.1	4.7	

Notes:

1. Inflow current is positive and outflow current is negative.

All voltage is referenced to COM unless otherwise noted.

Electrical Characteristics (continued)

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. [1, 2]

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
Logic input: IN+, IN–, $\overline{RST}$/EN, ASC_C						
V_{INH}	Logic-high input voltage	VCC=3.3V		1.85	2.31	V
V_{INL}	Logic-low input voltage		0.99	1.52		V
V_{INHYS}	Input hysteresis			0.33		V
I_{IH}	Logic-high input leakage	V_{IN}=VCC		90		μA
I_{IL}	Logic-low input leakage	V_{IN}=GND		–90		μA
R_{IND}	Input pulldown resistance	IN+, $\overline{RST}$/EN, ASC_C; See Figure 8-1		55		kΩ
R_{INU}	Input pullup resistance	IN–, See Figure 8-1		55		kΩ
t_{INFIL}	IN+, IN–, $\overline{RST}$/EN, ASC_C input deglitch time (rising or falling)	f =50kHz, see Figure 7-3,Figure 7-4	28	40	60	ns
		Only for CA-IS3215SxW and CA-IS3216SxW		10		ns
t_{RSTFIL}	$\overline{FLT}$ filter reset time	See Figure 7-9	400	550	800	ns
Gate driver						
I_{OUTH}	Peak sourcing current	C_{VDD}=10μF, C_L=0.18μF, f_S=1kHz	10	15		A
I_{OUTL}	Peak sink current	C_{VEE}=10μF, C_L=0.18μF, f_S=1kHz	10	15		A
R_{OUTH}	Pullup resistance	I_{OUT}=–0.1A		1.6		Ω
R_{OUTL}	Pulldown resistance	I_{OUT}=0.1A		0.23		Ω
V_{OUTH}	Output high voltage	I_{OUT}=–0.2A, VDD=18V		17.6		V
V_{OUTL}	Output low voltage	I_{OUT}=0.2A		50		mV
Active pulldown						
V_{OUTPD}	Active pulldown, OUTH, OUTL	I_{OUTL}=1A, VDD=OPEN, VEE=COM		2.0		V
Internal active Miller clamp (CA-IS321xxNW-Q1)						
V_{CLMPTH}	Miller clamp threshold	Referenced to VEE	1.5	2.0	2.5	V
V_{CLAMPI}	Low-level output clamp voltage	I_{CLAMPI}=1A		VEE+0.4		V
I_{CLAMPI}	Low-level output clamp current	V_{CLAMPI}=0V, VEE=–4V		4		A
R_{CLAMPI}	Miller clamp pulldown resistance	I_{CLAMPI}=0.2A		0.4		Ω
$t_{DCLAMPI}$	Miller clamp delay time	C_L=1.8nF, see Figure 7-5		15	50	ns
External active Miller clamp (CA-IS321xxEW-Q1)						
V_{CLMPTH}	Miller clamp threshold	Referenced to VEE	1.5	2.0	2.5	V
V_{CLAMPE}	High-level output voltage		4.8	5.0	5.3	V
$I_{CLAMPEH}$	Pullup peak current	C_{CLAMPE}=10nF	0.12	0.25		A
$I_{CLAMPEL}$	Pulldown peak current		0.12	0.25		A
$t_{CLAMPER}$	Rising time	C_{CLAMPE}=330pF, see Figure 7-6		20	40	ns
$t_{DCLAMPE}$	Miller clamp turn-on time			40	70	ns
Short-circuit clamp						
$V_{CLP-OUT(H)}$	V_{OUTH}–VDD	OUT=Low, $I_{OUT(H)}$=500mA, t_{CLP}=10μs		0.73		V
$V_{CLP-OUT(L)}$	V_{OUTL}–VDD	OUT=High, $I_{OUT(L)}$=500mA, t_{CLP}=10μs		1.3		V
$V_{CLP-CLAMPI}$	V_{CLAMPI}–VDD	OUT=High, I_{CLAMPI}=–20mA, t_{CLP}= 10μs		1.3		V
DESAT protection						
I_{CHG}	Capacitor charge current	V_{DESAT}=2.0V	445	500	570	μA
I_{DCHG}	Capacitor discharge current	V_{DESAT}=6.0V	12	23		mA
V_{DESAT}	Detection threshold	CA-IS3215xxW-Q1	8.2	9.1	10	V
		CA-IS3216xxW-Q1	5.4	6	6.6	V
$t_{DESATLEB}$	Leading edge blanking time		200	265	400	ns
$t_{DESATFIL}$	DESAT filter deglitch time		100	230	280	ns
$t_{DEFATOFF}$	DESAT to OUT(L) propagation delay	C_L=10nF	150	230	300	ns
$t_{DESATFLT}$	DESAT to $\overline{FLT}$ output low		300	410	600	ns

Notes:

1. Inflow current is positive and outflow current is negative.
2. All voltage is referenced to COM unless otherwise noted.

Electrical Characteristics (continued)

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. [1, 2]

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
Internal soft turn-off						
I_{STO}	Soft turn-off current under fault condition	CA-IS3215xxW-Q1	250	400	570	mA
		CA-IS3216xxW-Q1	600	1	1.4	A
ASC_C primary-side active short-circuit protection						
t_{ASCC_R}	ASC_C to output rising delay	ASC_C from Low to High	80	145	200	ns
t_{ASCC_F}	ASC_C to output falling delay	ASC_C from High to Low	80	145	200	ns
ASC_D secondary-side active short-circuit protection						
V_{ASCL}	ASC_D low-level input threshold		1.0	1.5	2.0	V
V_{ASCH}	ASC_D high-level input threshold		2.0	2.5	3.0	V
t_{ASC_r}	ASC_D to output rising delay		390	630	1120	ns
t_{ASC_f}	ASC_D to output falling delay		152	300	477	ns
$I_{IH\_ASC\_D}$	ASC_D high-level input leakage	V_{ASC_D}=5V			20	μA
$I_{IL\_ASC\_D}$	ASC_D low-level input leakage	V_{ASC_D}=COM	-20			μA
$\overline{FLT}$, RDY reporting						
t_{RDYHLD}	Minimum VDD or VCC UVLO time to assert RDY low output	See Figure 7-7, Figure 7-8	0.55	0.82	1	ms
$t_{FLTMUTE}$	Fault output mute-time	Reset $\overline{FLT}$ output latching via $\overline{RST}$/EN, see Figure 7-9	0.55	0.82	1	ms
R_{ODON}	Open-drain output on-time	I_{ODON}=5mA		30		Ω
V_{ODL}	Open-drain output low	I_{ODON}=5mA			0.3	V

Notes:
1. Inflow current is positive and outflow current is negative.
2. All voltage is referenced to COM unless otherwise noted.

6.10. Switching Characteristics

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
t_{PDHL_1}	Propagation delay, high to low	CA-IS3215NxW-Q1, CA-IS3216NxW-Q1	60	90	130	ns
t_{PDLH_1}	Propagation delay, low to high	See Figure 7-1	60	90	130	
t_{PDHL_2}	Propagation delay, high to low	CA-IS3215SxW-Q1, CA-IS3216SxW-Q1	60	100	150	
t_{PDLH_2}	Propagation delay, low to high	See Figure 7-2	60	100	150	
PWD	Pulse width distortion $\lvert t_{PDHL}-t_{PDLH} \rvert$	See Figure 7-1, Figure 7-2			30	
$t_{sk\text{-}pp}$	Part to part skew	Propagation delay (rising and falling)			30	
t_r	Driver output rise time	C_L=10nF, see Figure 7-1, Figure 7-2		30		
t_f	Driver output fall time	C_L=10nF, see Figure 7-1, Figure 7-2		30		
f_{MAX}	Maximum switching frequency				1	MHz
t_{DEAD}	Dead time for shoot through protection	CA-IS3215SxW-Q1	550	800	1000	ns
		CA-IS3216SxW-Q1	80	140	200	ns
CMTI	Common mode noise immunity	IN+=High, IN-=Low, see Figure 7-15, Figure 7-16	150			V/ns
		IN+=Low, IN-=Low, see Figure 7-15, Figure 7-16	150			

Notes:
1. Inflow current is positive and outflow current is negative.
2. All voltage is referenced to COM unless otherwise noted.

6.11. Typical Characteristics

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.

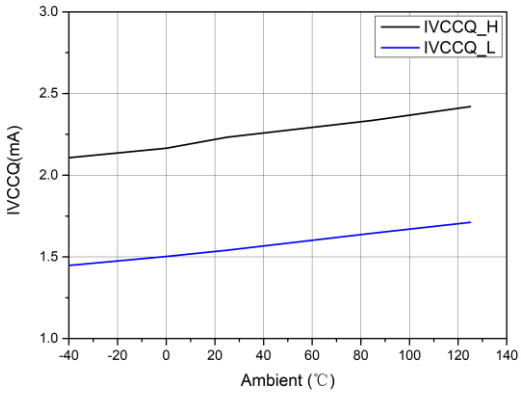


Figure 6-1. VCC quiescent current vs. temperature

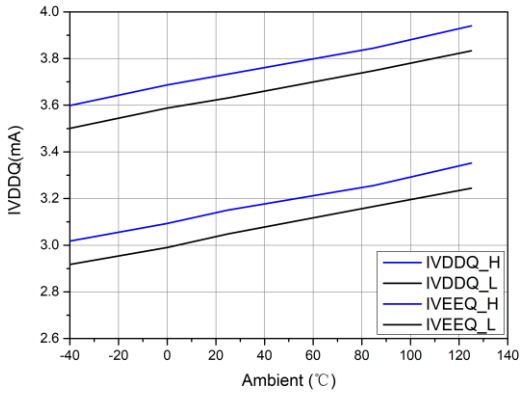


Figure 6-2. VDD & VEE quiescent current vs. temperature

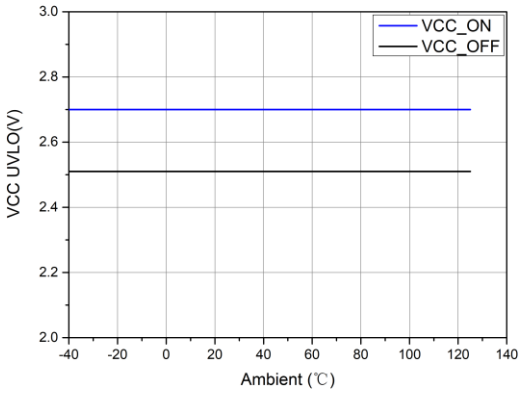


Figure 6-3. VCC UVLO vs. temperature

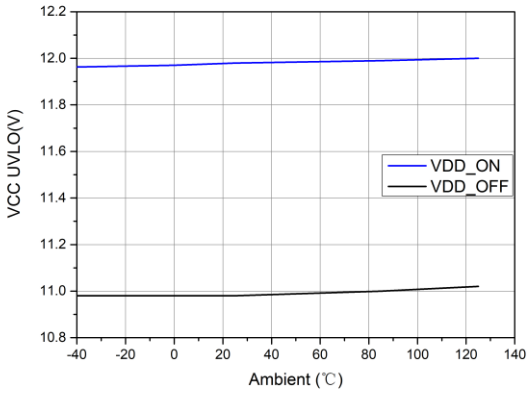


Figure 6-4. VDD UVLO vs. temperature

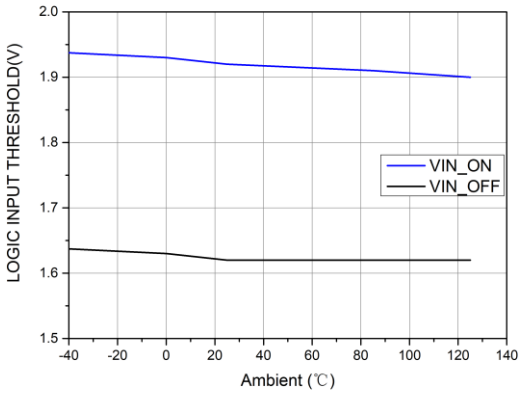


Figure 6-5. Logic input threshold vs. temperature

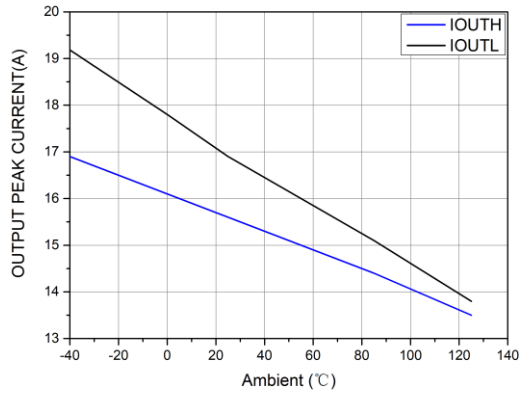


Figure 6-6. Output peak current vs. temperature (C_L=180nF)

（Continued）

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.

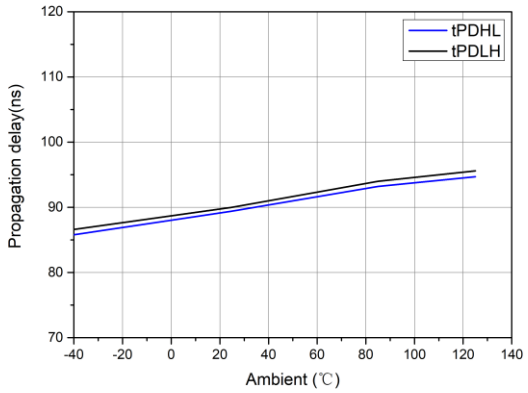


Figure 6-7. Propagation delay vs. temperature

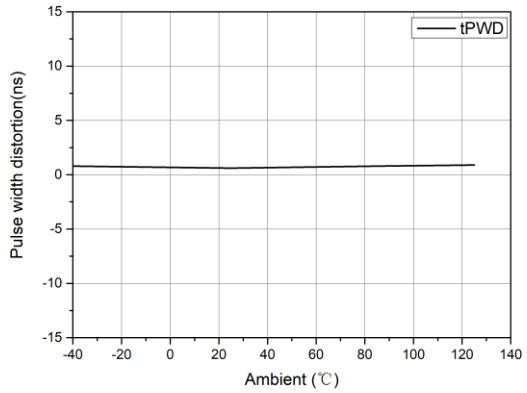


Figure 6-8. PWD vs. temperature

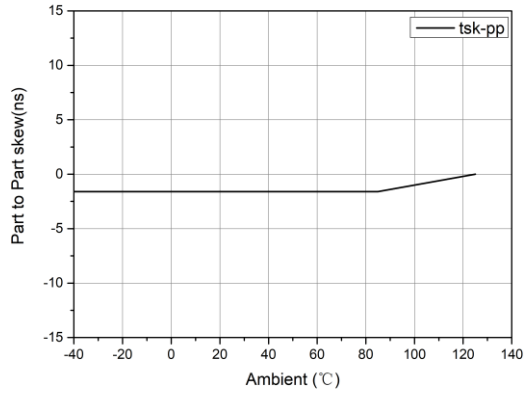


Figure 6-9. Delay matching vs. temperature

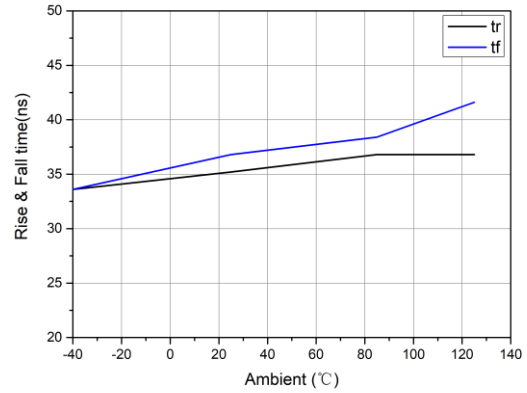


Figure 6-10. Rise & Fall time vs. temperature

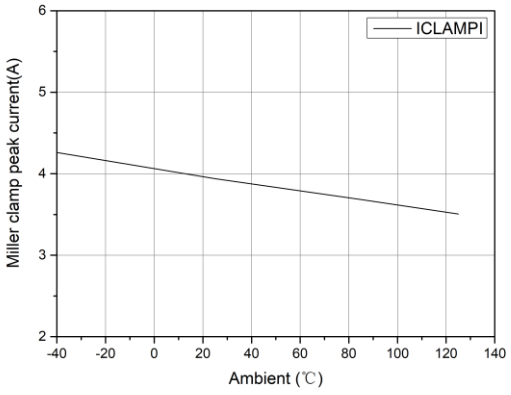


Figure 6-11. Miller clamp current vs. temperature

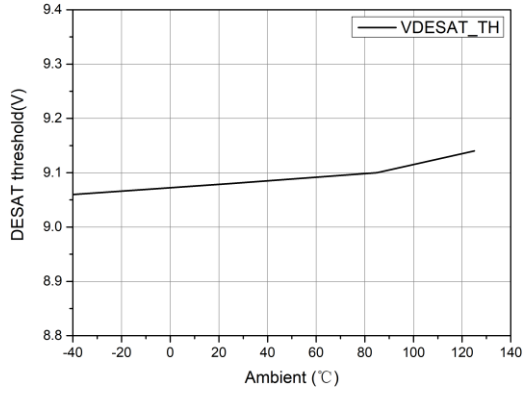


Figure 6-12. DESAT threshold vs. temperature

（Continued）

V_{CC} = 3.3V or 5V, connect a 1μF bypass capacitor between VCC and GND; VDD-COM = 20V, 18V or 15V; COM–VEE=0V, 5V, 8V or 15V; C_L=100pF; -40°C < T_J < +150°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.

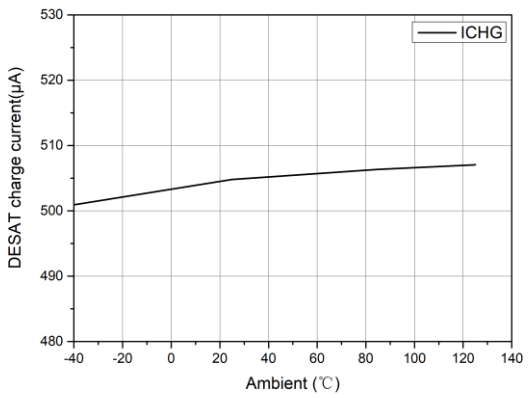


Figure 6-13. DESAT charge current vs. temperature

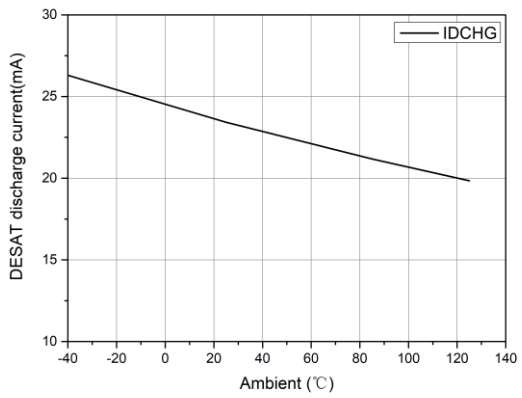


Figure 6-14. DESAT discharge current vs. temperature

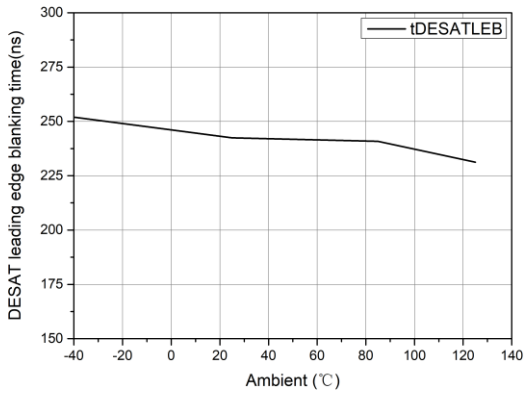


Figure 6-15. DESAT blanking time vs. temperature

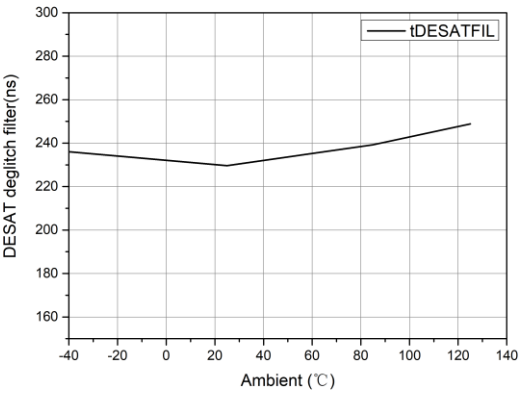


Figure 6-16. DESAT filter time vs. temperature

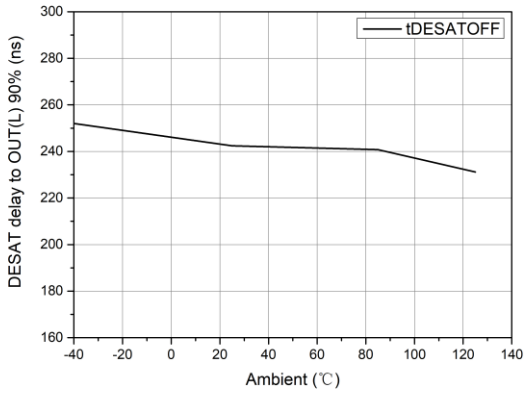


Figure 6-17. DESAT to OFF delay vs. temperature

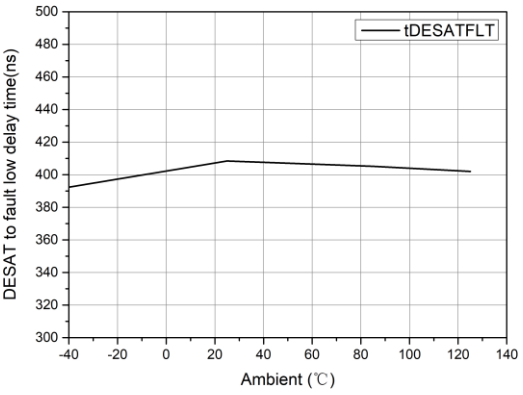


Figure 6-18. DESAT to Fault delay vs. temperature

7. Parameter Measurement Information

7.1. Propagation Delay

Figure 7-1 and Figure 7-2 shows the definition and measurement for the non-inverting or inverting input propagation delay (t_{PDLH}, t_{PDHL}).

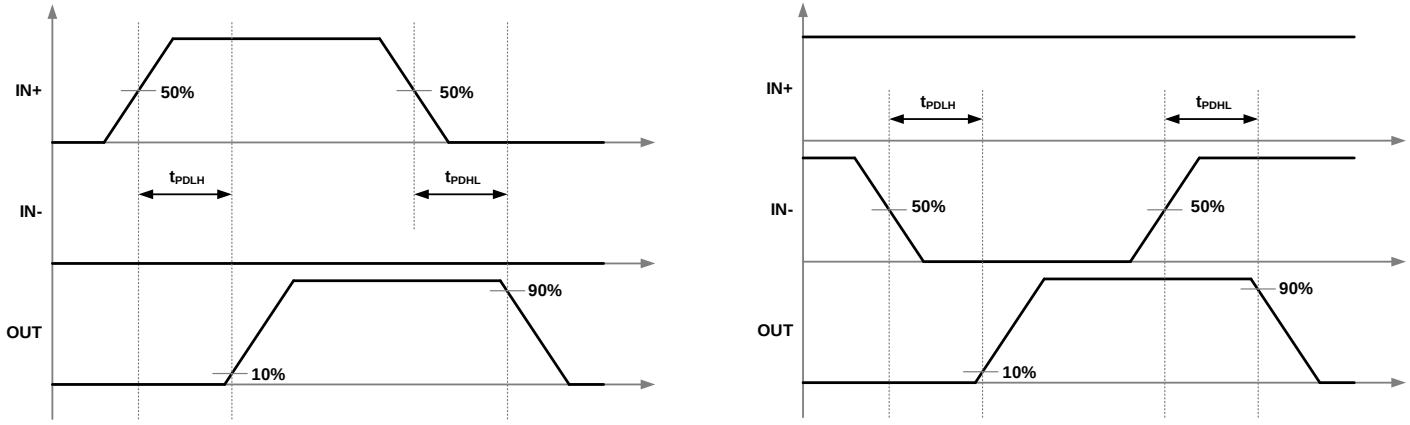


Figure 7-1 Noninverting(Left) and Inverting(Right) propagation delay measurement (Without DT protection)

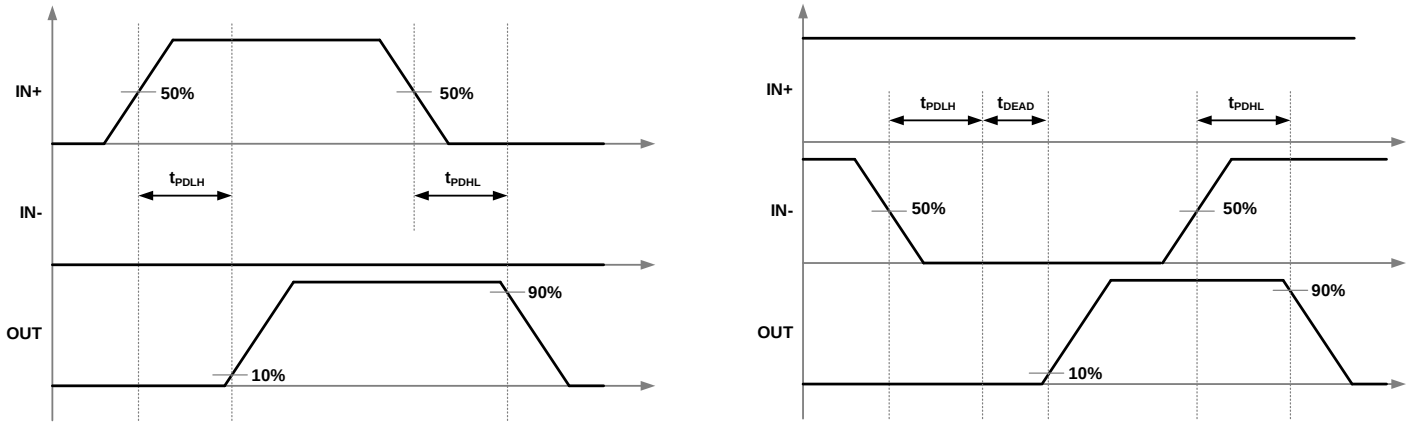


Figure 7-2 Noninverting(Left) and Inverting(Right) propagation delay measurement (With DT protection)

7.2. Input Glitch Filter

Fast common-mode transients and accidental small pulses can inject noise and glitches on the control inputs (IN+, IN–, $\overline{RST}$/EN, ASC_C pins) because of parasitic coupling. In order to increase the robustness of gate driver, the CA-IS3215/6 devices feature a 40ns glitch filter per control input to reduce glitches and noise at the input, and make sure there is no wrong output responses or accidental driver operation. For example, if the IN+ or IN_ PWM pulse width is lease than t_{INFIL}, the input signal will be filtered out and there will be no responses on gate driver output. Figure 7-3 shows the ON/OFF pulse deglitch filter effect on IN+ input; Figure 7-4 shows the ON/OFF pulse deglitch filter effect on IN_ input.

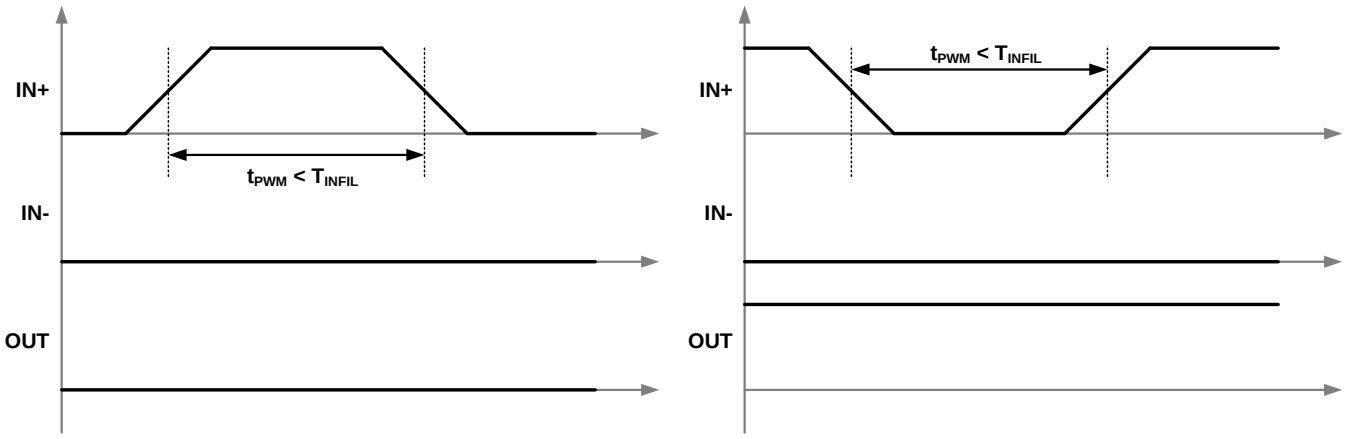


Figure 7-3 IN+ ON/OFF deglitch filter

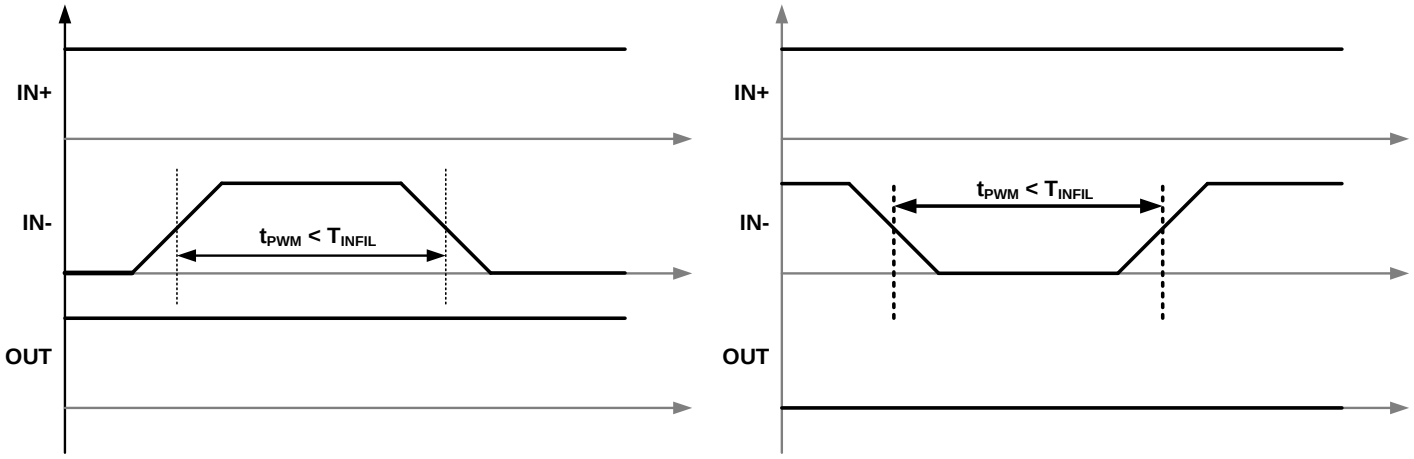


Figure 7-4 IN– ON/OFF filter

7.3. Active Miller Clamp

7.3.1. Internal Active Miller Clamp

For the gate driver with single supply or dual supplies with small negative turn-off voltage on driver-side, the active Miller clamp circuit provides a very low-impedance path to direct the Miller current. This configuration can prevent the power transistors from unintentionally turning-on because of high dV/dt current induced from the Miller effect, see Figure 7-5 for a Miller clamp timing diagram.

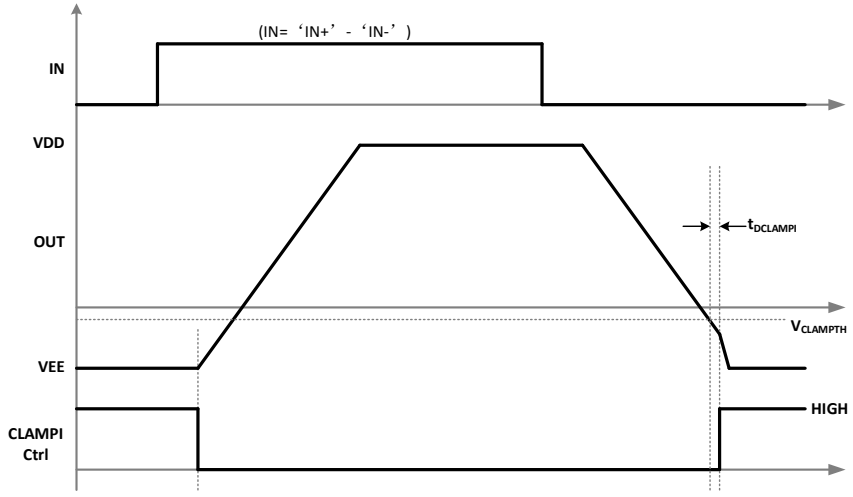


Figure 7-5 Internal active Miller clamp timing diagram

7.3.2. External active Miller clamp

The external active Miller clamp circuit allows designer to flexibly select MOSFET. It provides a low-impedance path for the gate to direct Miller current, this configuration can prevent the external power transistors from unintentionally turning-on because of high dV/dt current induced from the Miller effect, see Figure 7-6 for a Miller clamp timing diagram.

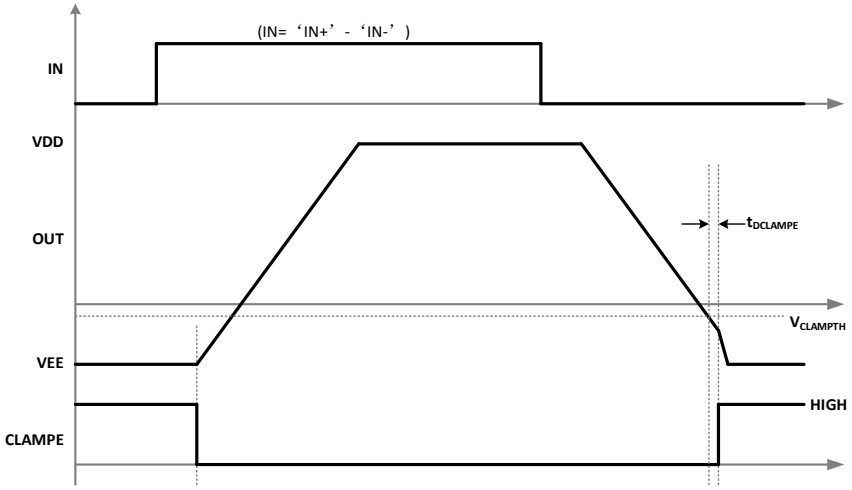


Figure 7-6 External active Miller clamp timing diagram

7.4. Power-up UVLO Delay

The VCC and VDD supplies are both internally monitored for undervoltage conditions. UVLO is a key protection function. It can prevent the power transistors from unintentionally turning-on when control-side or driver-side supply is in UVLO condition during power-up, power-down, or during normal operation due to a sagging supply voltage.

7.4.1. VCC UVLO

Figure 7-7 shows the behavior of the outputs during power-up and power-down, including UVLO ON/OFF threshold, deglitch filter, response time, and RDY timing diagram.

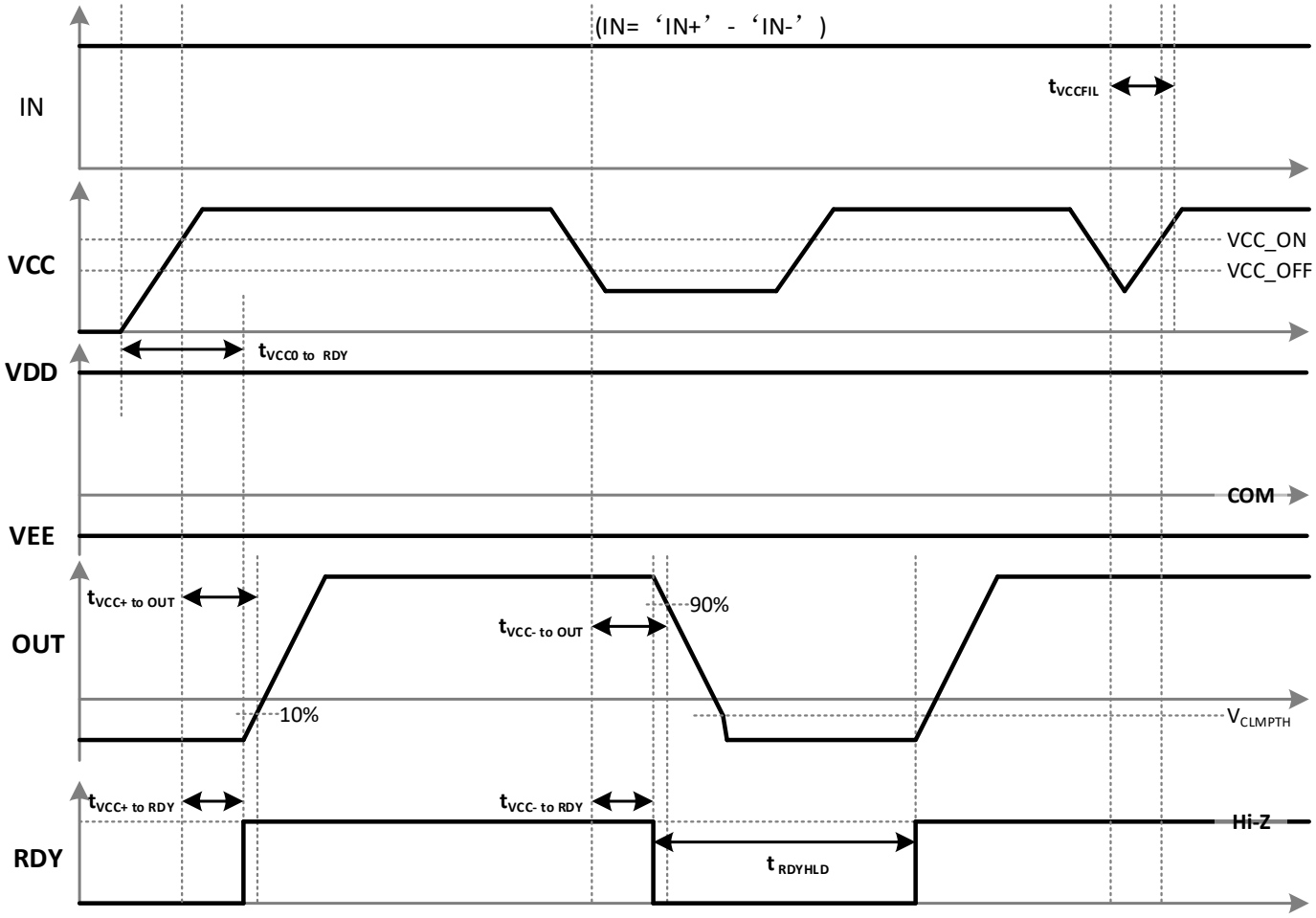


Figure 7-7 VCC UVLO timing diagram

7.4.2. VDD UVLO

Figure 7-8 shows the behavior of the outputs during power-up and power-down, including UVLO ON/OFF threshold, deglitch filter, response time, and RDY timing diagram.

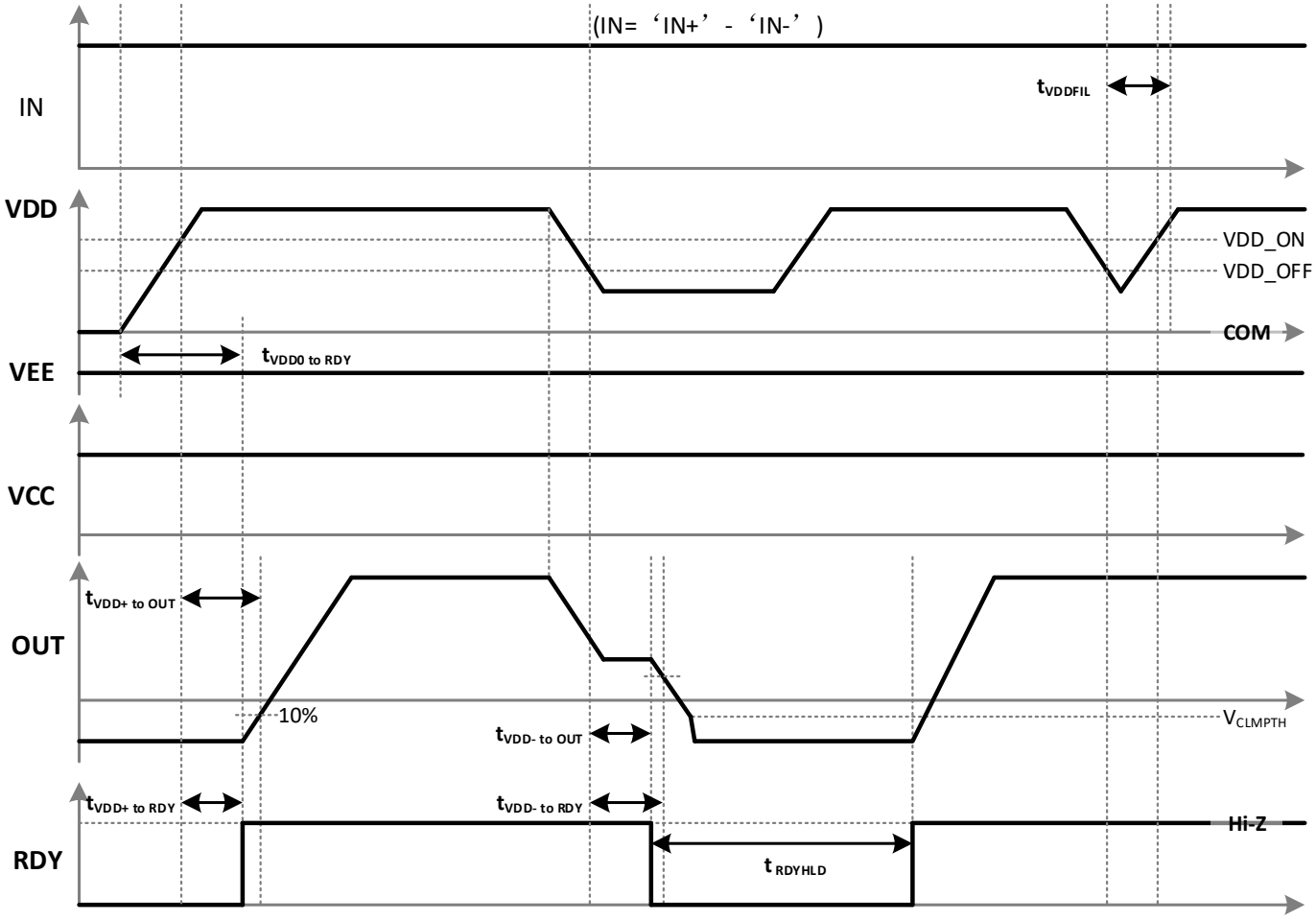


Figure 7-8 VDD UVLO timing diagram

7.5. DESAT Protection

7.5.1. DESAT Protection with Soft turn-off

Desaturation (DESAT) protection circuit monitors V_{DS} voltage of SiC or V_{CE} voltage of IGBT under over-current conditions. Figure 7-9 shows the DESAT operation timing diagram during the power transistors turn-on transition.

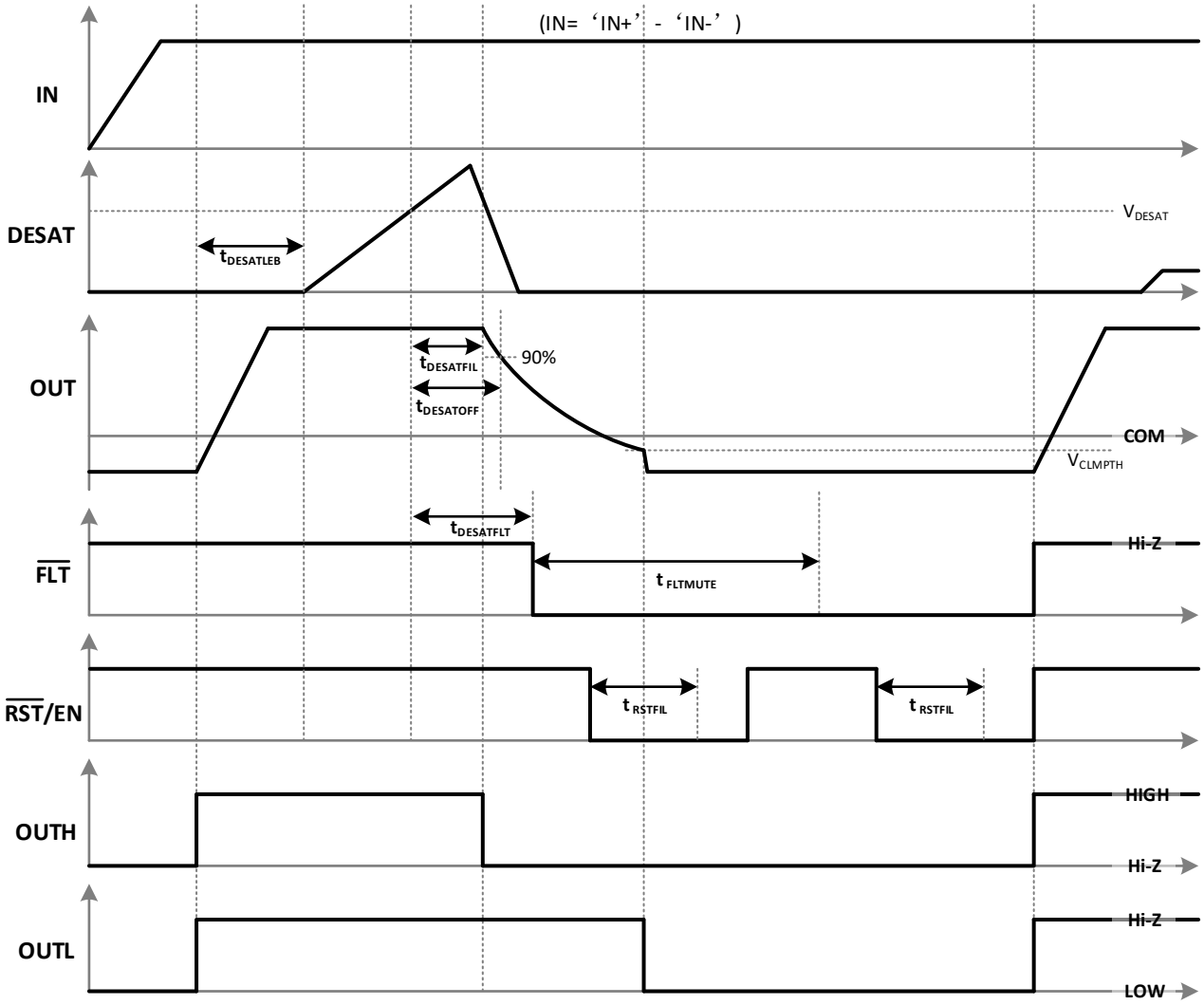


Figure 7-9 DESAT operation timing diagram during turn-on transition

Figure 7-10 shows the DESAT operation timing diagram during the power transistors is on.

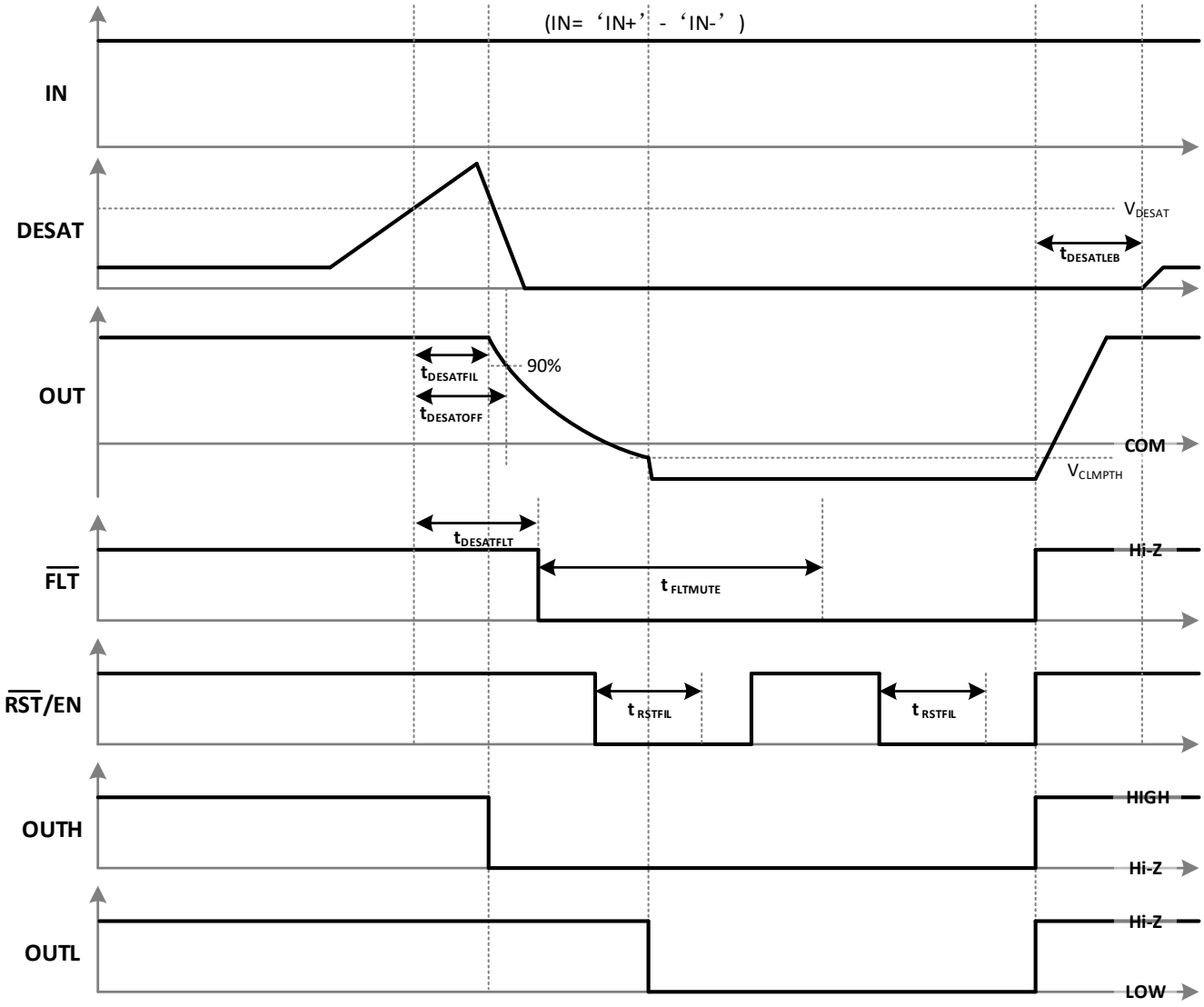


Figure 7-10 DESAT operation timing diagram during power transistors is on

7.6. Active Short-circuit Protection (ASC)

7.6.1. Active Short-circuit Protection on Control-side ASC_C

Figure 7-11 shows the control side ASC_C protection timing diagram during VCC UVLO; Figure 7-12 shows the ASC_C protection timing diagram during VDD UVLO on the control side.

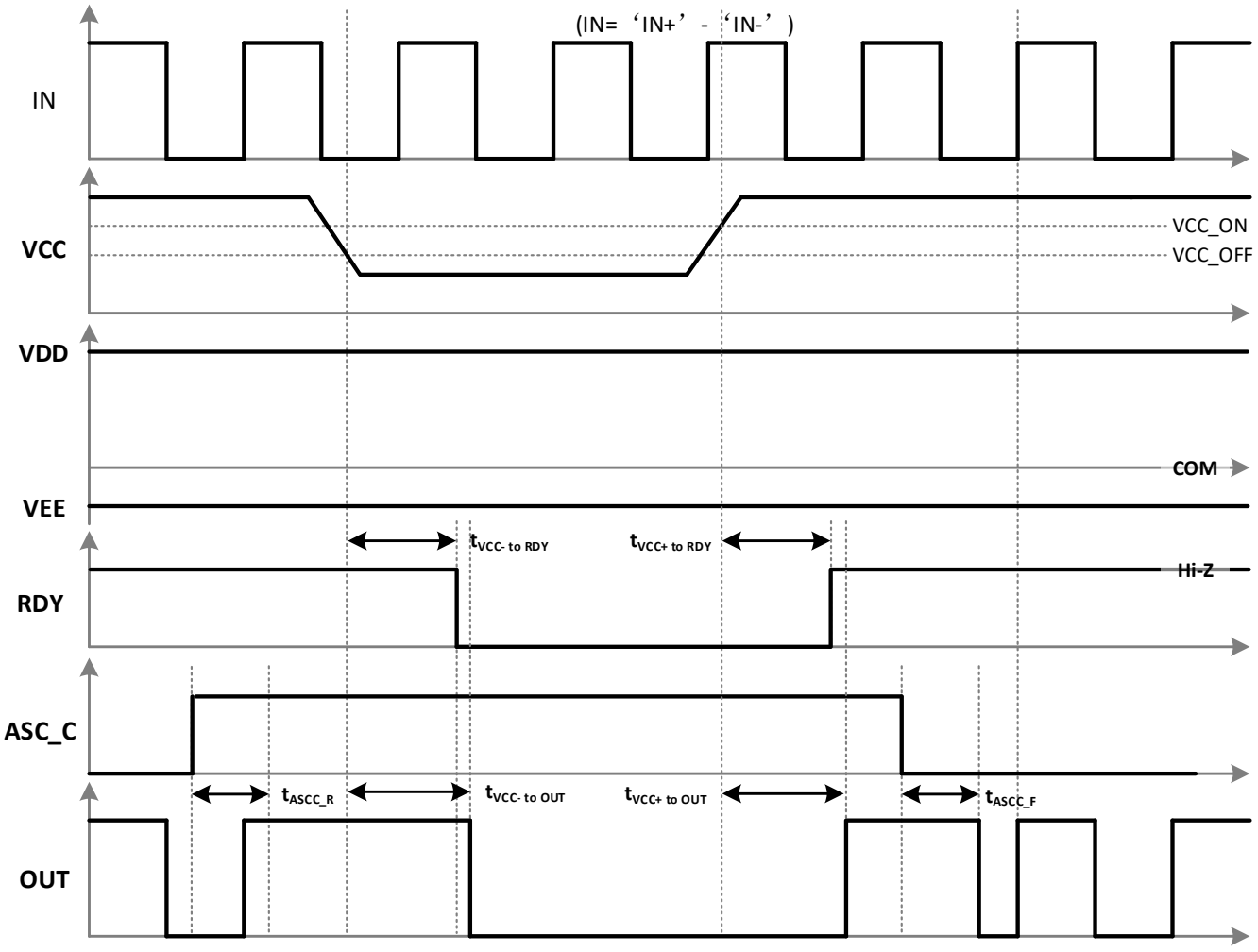


Figure 7-11 ASC_C protection timing during VCC UVLO

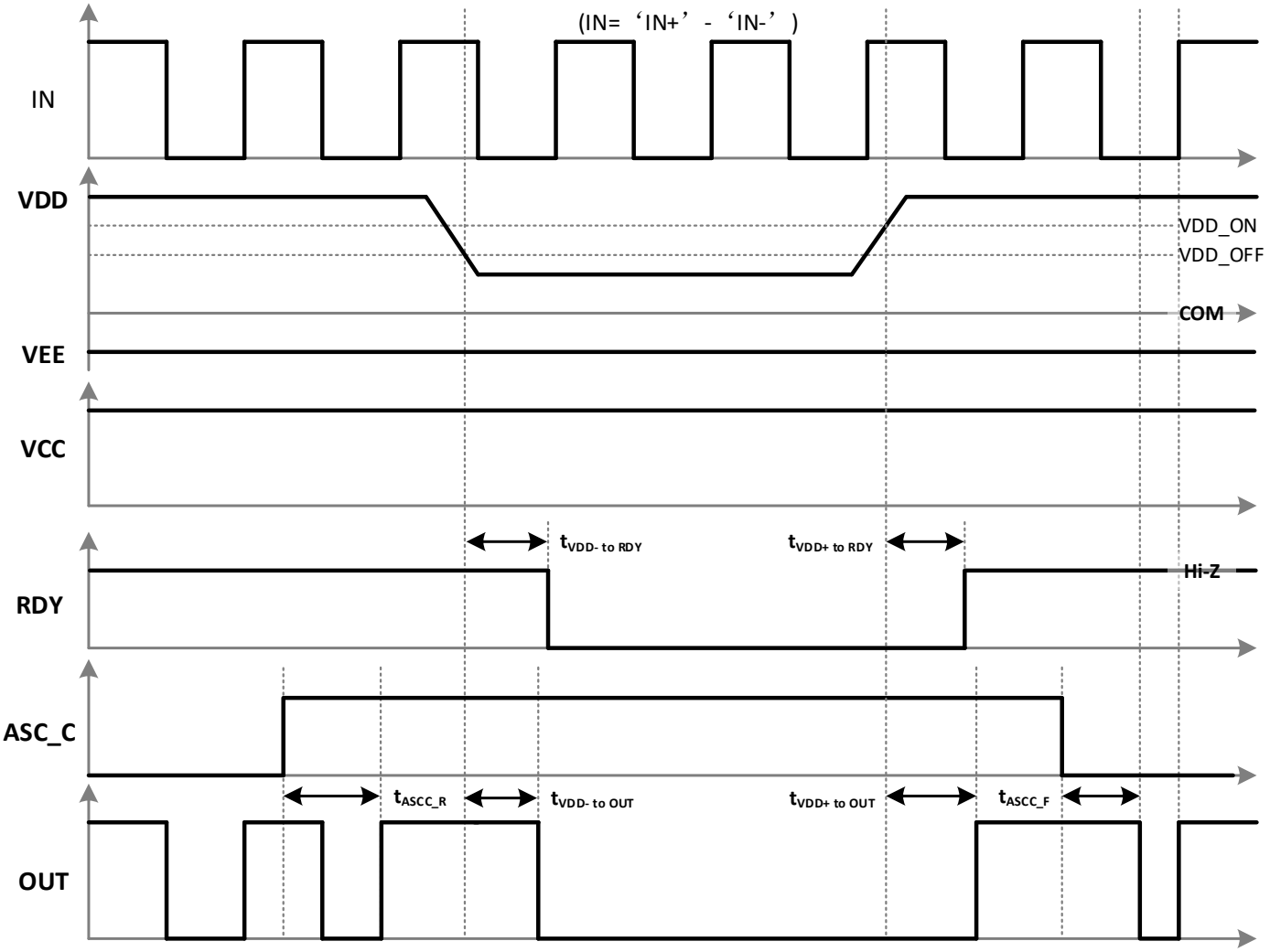


Figure 7-12 ASC_C protection timing during VDD UVLO

7.6.2. Active Short-circuit Protection on Driver-side ASC_D

Figure 7-13 shows the driver side ASC_D protection timing diagram during VCC UVLO.

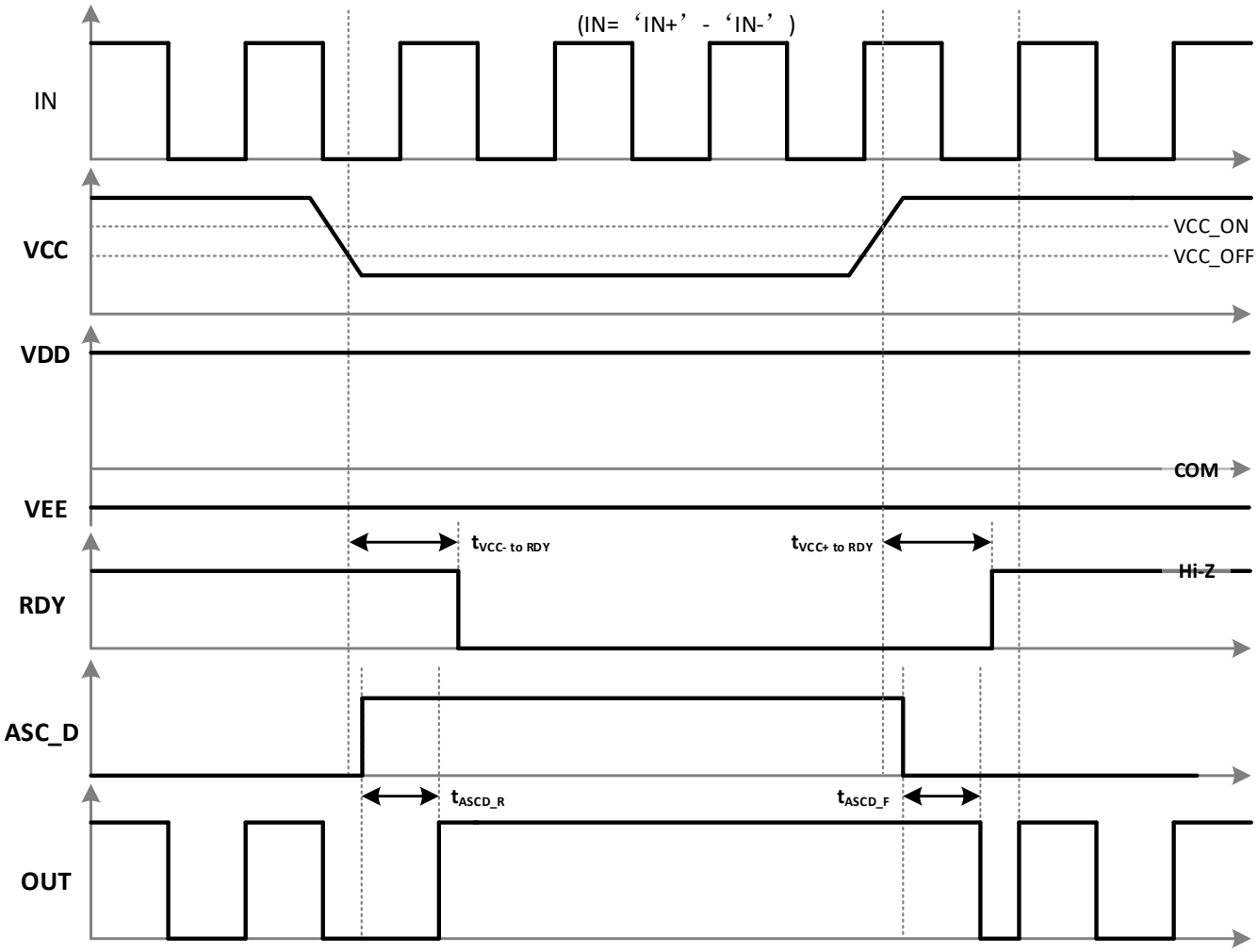


Figure 7-13 ASC_D protection timing during VCC UVLO

Figure 7-14 shows the ASC_D protection timing diagram during VDD UVLO on the driver side.

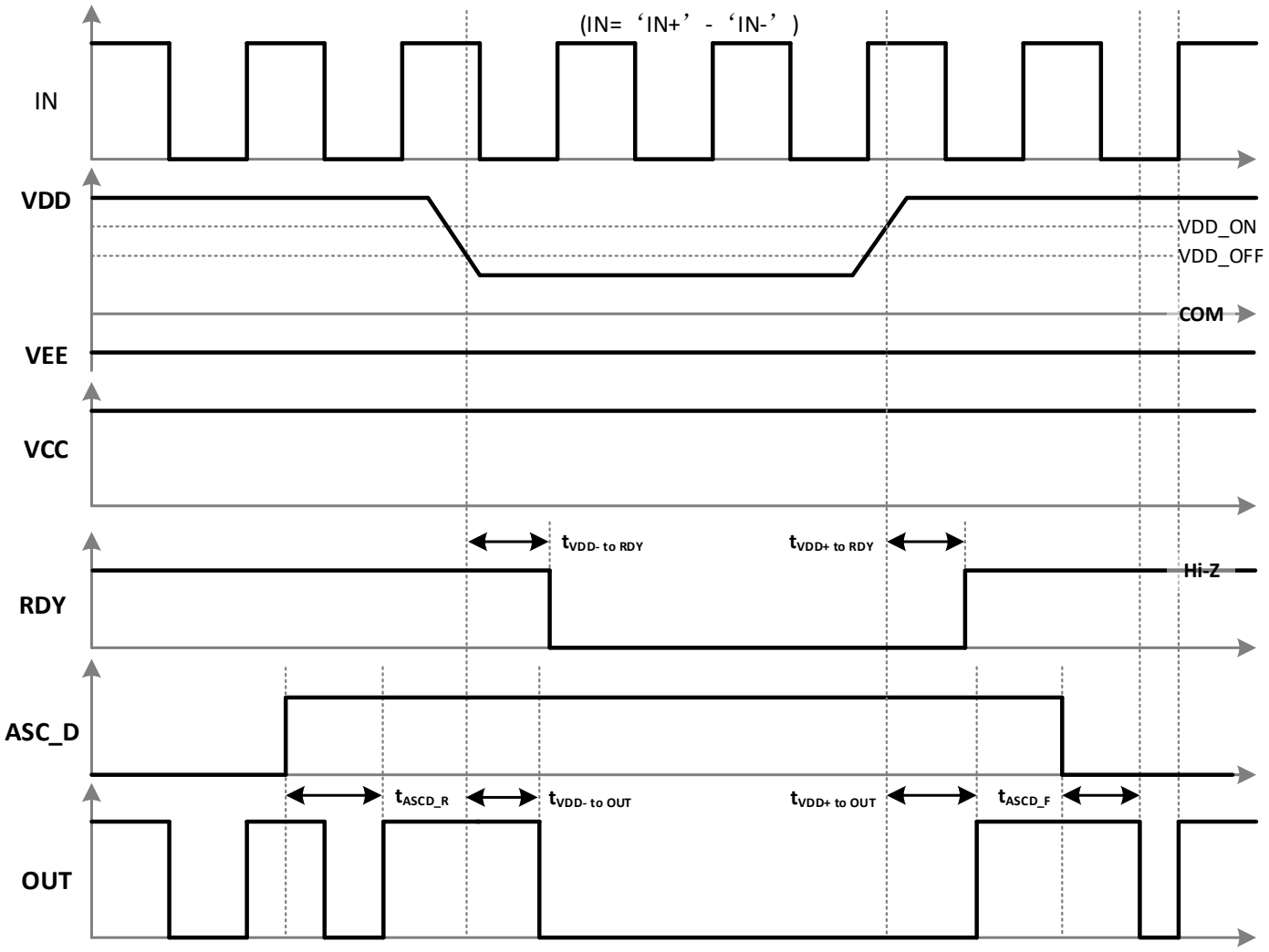


Figure 7-14 ASC_D protection timing during VDD UVLO

7.7. CMTI Test Circuit

Figure 7-15 and Figure 7-16 are the CMTI test configuration for the CA-IS3215/6 products.

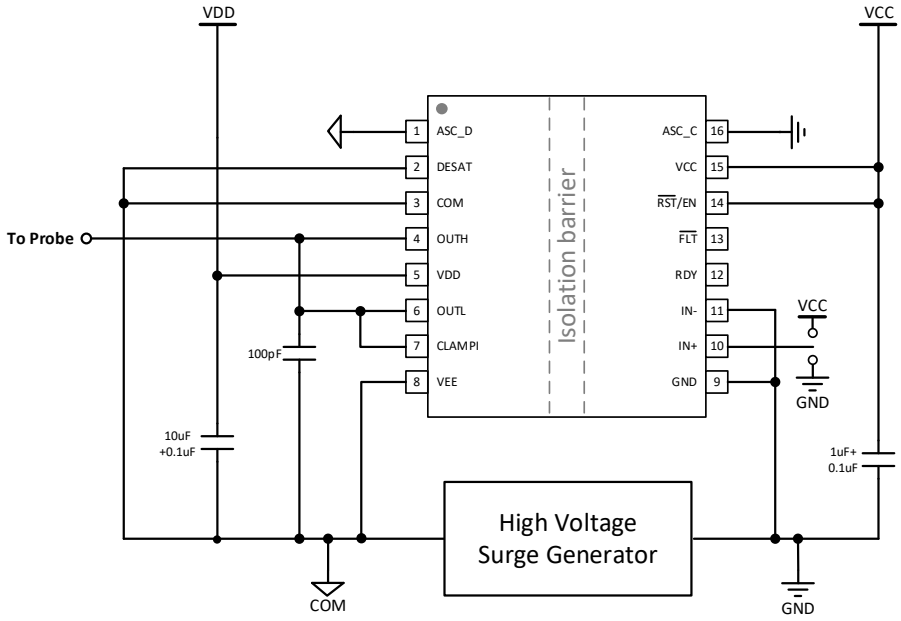


Figure 7-15 Common-mode transient immunity test circuit (CA-IS3215/6xNW)

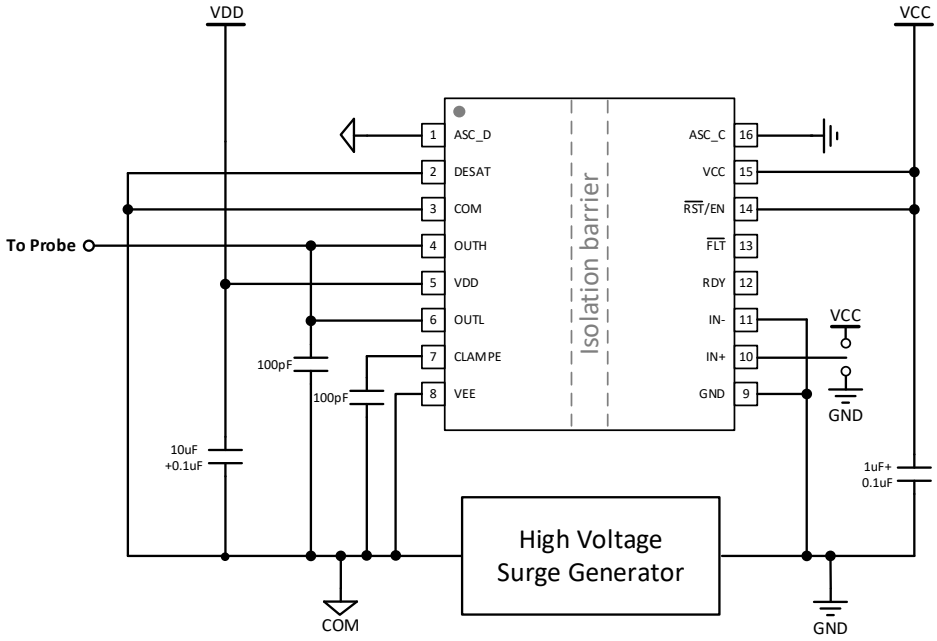


Figure 7-16 Common-mode transient immunity test circuit (CA-IS3215/6xEW)

8. Detailed Description

8.1. Overview

To quickly switch the high-power transistors to reduce switching power dissipation, a high-current, high-frequency gate driver is often placed between the controller (DSP or MCU) output and the gate of power transistors, because the controllers are not capable of delivering sufficient current to drive the gates of power transistors. The CA-IS3215/6 family of single channel, reinforced isolated gate drivers is designed to meet this kind of requirements.

These isolated gate drivers capable of sinking 15A, sourcing 15A peak-current, and the minimum peak-current is not less than 10A. The integrated digital galvanic isolation between control-side and driver-side using Chipanalog's proprietary SiO_2 capacitive isolation technology can support up to $1500V_{RMS}$ isolation working voltage and $12.8kV_{PK}$ surge rating. High current drive capability, fast switching time and ultra-low propagation delay skew make them ideal to reduce the switching losses in the high-frequency, small size power system design; The minimum CMTI of 150V/ns ensures the reliability of the system under fast switching operation. The CA-IS3215/6 devices operate with dual supplies or a single supply of 13V to 33V wide voltage range of $V_{DD} – V_{EE}$ with 12V UVLO threshold and support unbalanced dual supplies operation, is well suited to drive power MOSFET, IGBT or silicon-carbide(SiC) transistors in HEV/EV inverter, motor control, solar inverter, industrial power supply etc. high-power design applications.

The CA-IS3215/6 devices integrated advanced fault detection and protection functions to improve the reliability and robustness of SiC MOSFET and IGBT driving. The 12V VDD UVLO is suitable for power switches with gate-drive voltage ≥ 15V. The active Miller clamp protection can prevent the power transistors from unintentionally turning on because of high current induced from the Miller effect. Also, the devices feature fast DESAT detection and fault alarm to the low-voltage control side(DSP/MCU). When the device detects a DESAT fault, it will trigger a Soft turn-off, thereby minimizing short-circuit energy and reducing overshoot voltage on the power switch. Fixed dead-time (CA-IS3215S_/ CA-IS3216S_) and internal logic circuitry prevent shoot-through during output-state changes.

8.2. Functional Block Diagram

Figure 8-1 and Figure 8-2 provide a simplified block diagram for the CA-IS321xxNW-Q1 and CA-IS321xxEW-Q1, respectively. It shows the main elements of CA-IS3215/6, including input stage, output stage, fault detection and active protection, ASC control, VCC and VDD UVLO, digital isolator etc. functional groups. Their operations are described separately in the following sections.

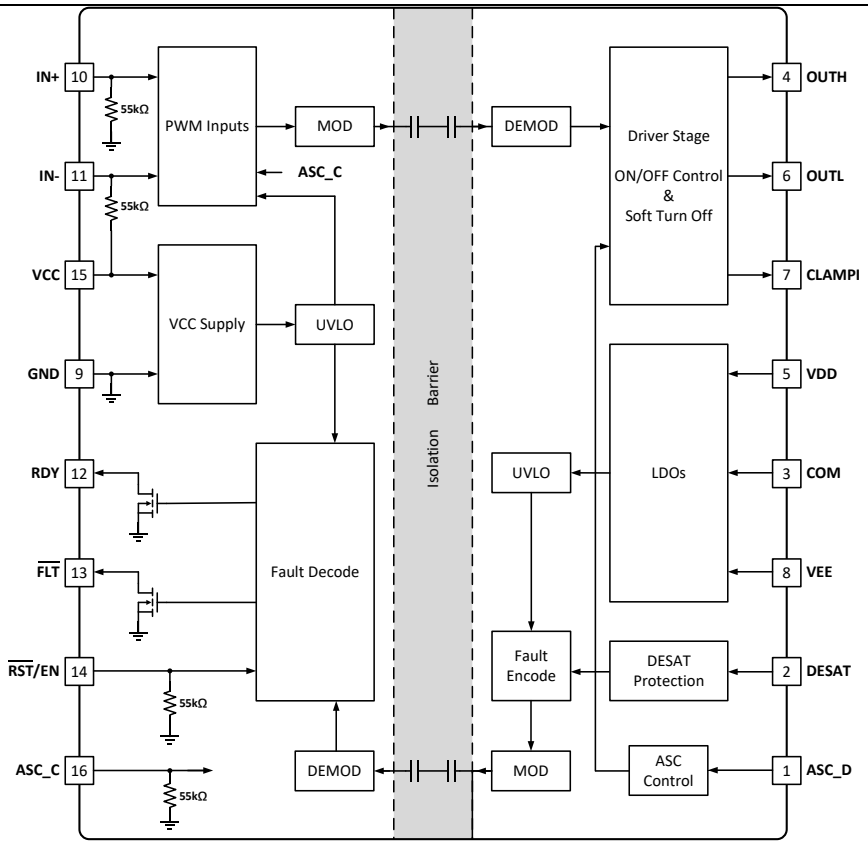


Figure 8-1 CA-IS321xxNW-Q1 functional block diagram

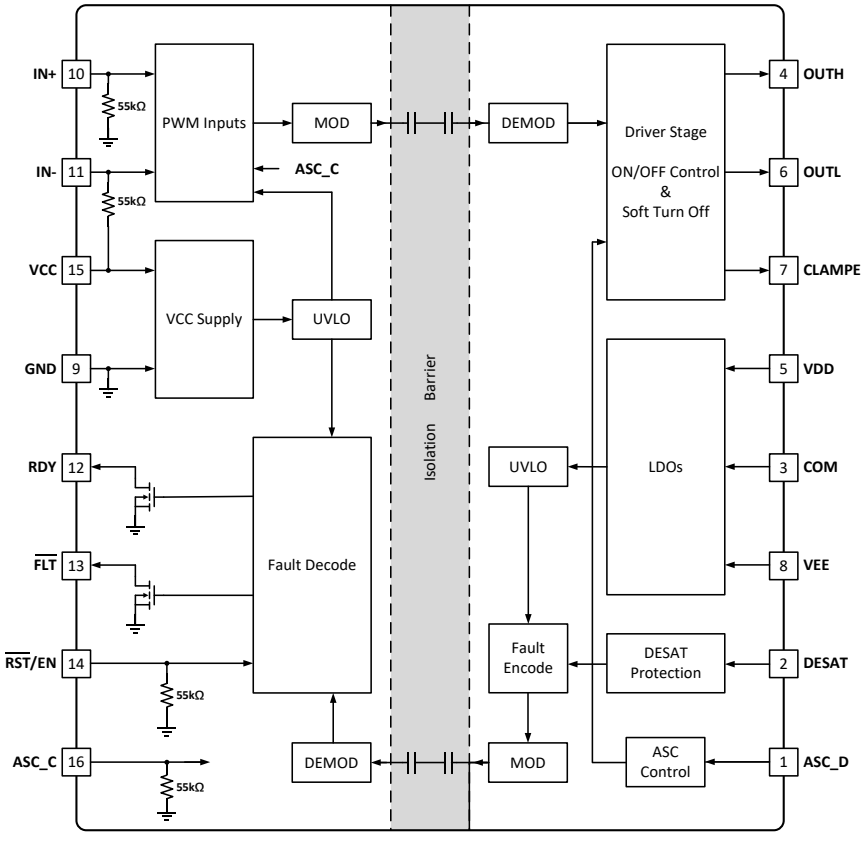


Figure 8-2 CA-IS321xxEW-Q1 functional block diagram

8.3. Input Stage

Fast common-mode transients and accidental small pulses can inject noise and glitches on the control inputs (IN+, IN–, $\overline{RST}$/EN, ASC_C pins) because of parasitic coupling. In order to increase the robustness of gate driver, the CA-IS3215/6 devices integrated a 40ns (t_{INFIL}) glitch filter at each control input to reduce glitches and noise at the input, make sure there is no wrong output responses or accidental driver operation. If the input signal pulse width is lease than t_{INFIL}, the input signal will be filtered out and there will be no responses on gate driver output. Figure 7-3 and Figure 7-4 show the ON/OFF pulse deglitch filter effect on IN+/IN_ inputs.

8.4. Driver Output Stage

The output driver stage of the CA-IS3215/6 integrates a pull-up structure and a pull-down structure. They have distinct current sourcing/sinking(±15A) capabilities to control the external transistors (SiC MOSFET, IGBT modules or the parallel discrete devices) directly. Figure 8-3 shows the output stage circuit, in the output stage, a p-channel MOSFET and an additional n-channel MOSFET in parallel combined into the pull-up structure. The n-channel MOSFET only turns on for a short period of time during the output low-to-high transition and provides a boost current to enable the fast turn-on of the device. The on-resistance of this n-channel MOSFET is R_{NMOS} when activated; Figure 8-3. R_{OH} is the on-resistance of the P-channel MOSFET only, R_{NMOS} << R_{OH}. When the driver output is changing from low to high, the n-channel MOSFET is turned on until the voltage of OUTH pin reaches V_{DD} -3V. Thus, the effective on-resistance of the output pull-up stage is dependent on R_{NMOS}, same as R_{OL} (the CA-IS3215/6 output stage integrated same n-channel MOSFET for the pull-up and pull-down circuit) during NMOS turn-on phase, it is much lower than R_{OH}. After this, the voltage of OUTH is pulled to VDD through the p-channel MOSFET. The very low pull-up resistance provides large driving capacity, thus shortening the charging time of the power transistor's input capacitor and reducing the switching loss.

The pull-down circuit of CA-IS3215/6 is simply composed of an n-channel MOSFET. The voltage of OUTL is pulled to VEE through the pull-down NMOS. R_{OL} in Figure 8-3. is the on-resistance of the pull-down n-channel MOSFET, see Electrical Characteristics for more detail. This very low pull-down resistance not only achieve high sinking current, reduce turn-off time, but also help improve noise immunity considering Miller effect.

Because of the very low turn-on impedance of the output stage MOSFETs, the CA-IS3215/6 isolated gate drivers can provide rail-to-rail outputs (output voltage swings between V_{DD} and V_{EE}).

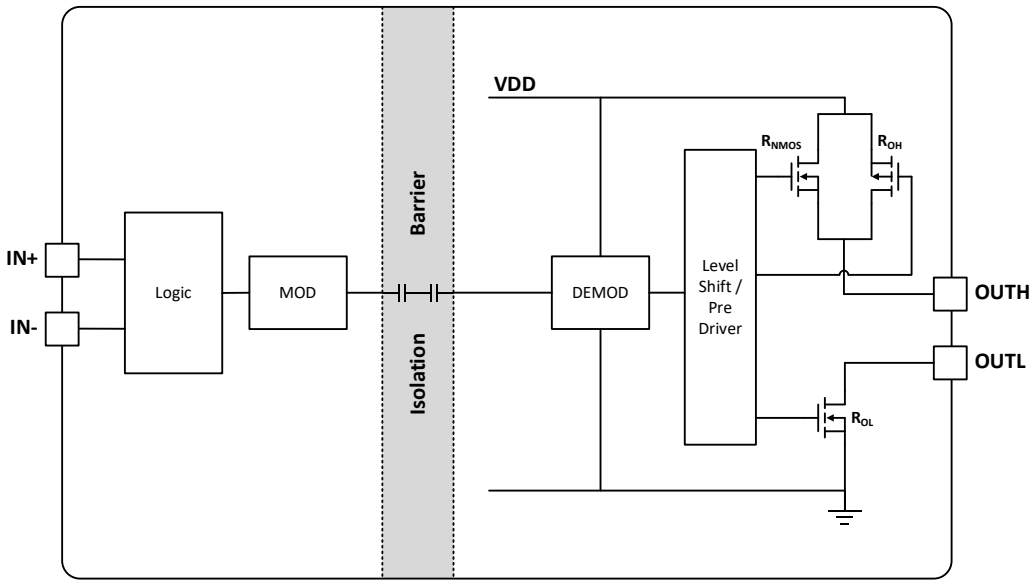


Figure 8-3 Gate-driver output stage

8.5. Protection Functions

8.5.1. VCC and VDD Undervoltage Lockout (UVLO)

The CA-IS3215/6 devices feature undervoltage detection for VCC and VDD both supplies. The VDD UVLO is referenced to COM. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. Once an undervoltage condition is detected on either supply, the output is set to logic-low to turn off the external power transistor, regardless of the inputs state.

For IGBT and SiC MOSFET, the turn-on resistance will be reduced as the gate-emitter voltage or gate-source voltage increases. If the power transistors is turned on at low driver voltage, the conduction loss will increase significantly. This may cause thermal issue. So the UVLO protection not only reduces power consumption of gate driver at low supply voltage, but also improves power transistors operating efficiency. The CA-IS3215/6 features 12V VDD UVLO threshold with 1V hysteresis which ensure robust system performance under noisy conditions.

Once an undervoltage condition is cleared and the supply voltage has returned to a valid level, the CA-IS3215/6 gate drivers transition to normal mode after the power-up delay time ($t_{VCC+\ to\ OUT}$ or $t_{VDD+\ to\ OUT}$) has expired. Both VCC UVLO and VDD UVLO have hysteresis to avoid chattering when there is ground noise from the power supply, also allows the device to accept small drops in supply voltage and ensures stable operation. Table 8-1 illustrates the VCC UVLO and VDD UVLO feature logic, Figure 7-6 and Figure 7-7 show the VCC UVLO and VDD UVLO protection timing diagram. The CA-IS3215 and CA-IS3216 also feature a RDY signal to indicate that the devices have been powered properly and is ready for normal operation. RDY goes high when VCC and VDD are both above their respective UVLO thresholds.

8.5.2. Active Pulldown

The CA-3215/6 has an active pulldown function to turn-off the external power transistor when VDD is open and prevent the external power transistor from falsely turning-on before the device is back to control. See Figure 8-4, when the driver output stages are in power-off or VDD is open, the OUTH/OUTL pins are placed in high-impedance and clamped to VEE.

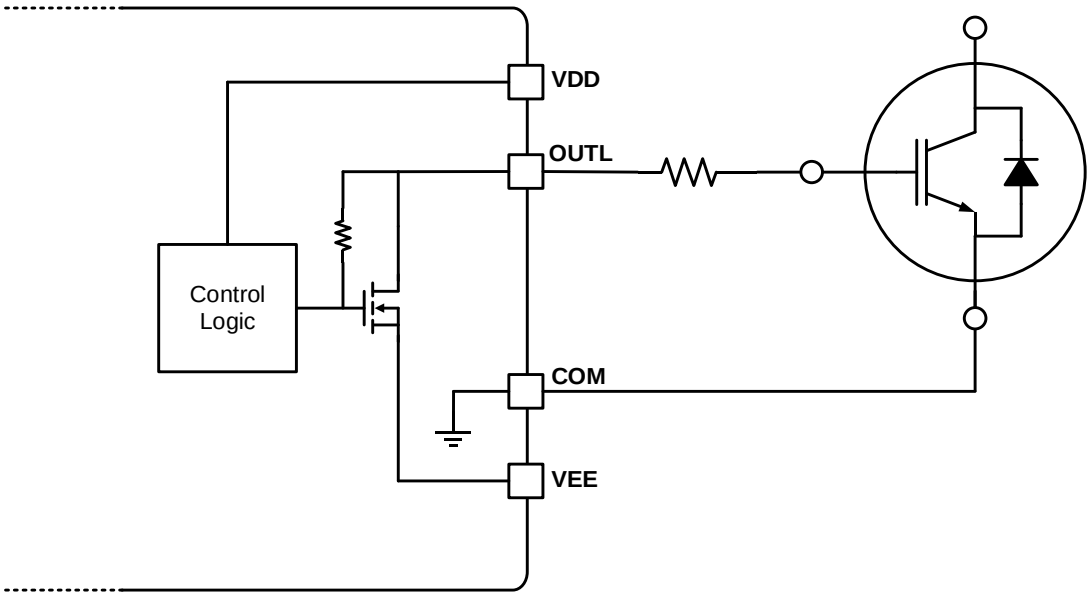


Figure 8-4 Active pulldown

8.5.3. Short-Circuit Clamping

The output stage of the CA-IS3215/CA-IS3216 features internal short-circuit clamping function that clamp the driver output (OUTH/OUTL) and CLAMPI(for CA-IS3215xNW/CA-IS3216NW) voltage, pull the OUTH/OUTL and CLAMPI voltage slightly higher than V_{DD} supply during short-circuit conditions. This protects the external transistors from gate-source or gate-emitter overvoltage breakdown. The internal conduction diode between OUTH/OUTL/CLAMPI and VDD can be used to provide larger current conduction capability, ensure system reliability.

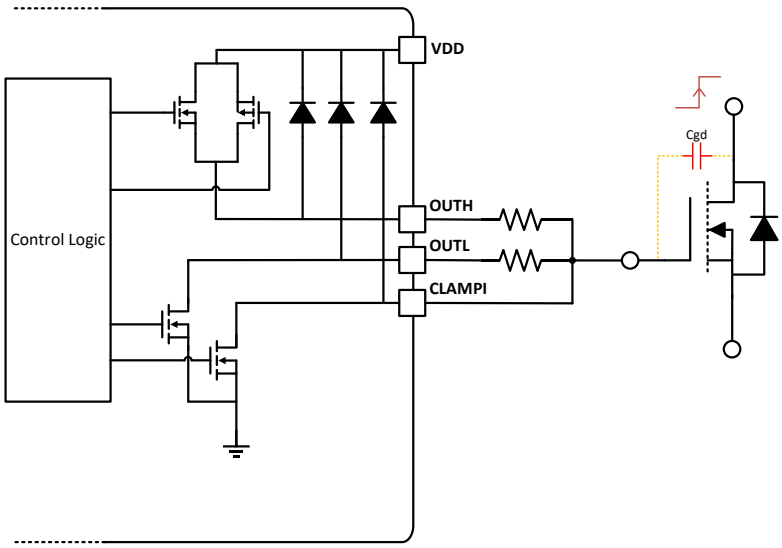


Figure 8-5 Short-circuit clamping

8.5.4. Active Miller Clamp

The CA-IS3215/6 has active Miller clamp protection as shown in Figure 8-6 to prevent the false turn-on while the gate-driver is in off state. In the synchronous rectifier operation applications, the body diode conducts the current during deadtime while a power transistor is turned-off, the drain-source or collector-emitter voltage remains the same. The dV/dt happens when another power transistor turns on. The low internal pulldown resistance of the CA-IS3215/6 offers strong pull-down which keeps OUTL to low-level, close to VEE voltage. However, in the typical application circuit, a external gate resistor is used to limit the dV/dt current. During another power transistor is turning-on transient, the miller effect can cause a voltage drop on the external gate resistor, which boost the collector-emitter voltage or gate-source voltage. Once this voltage reaches or is higher than the turn-on threshold voltage of power transistor, will cause shoot through and damage the external power devices. In this case, the internal Miller clamp of CA-IS3215Xnw/CA-IS3216xNW can provide effective protection. For example, when the external high-side transistor is turned on after the external low-side transistor is turned off, the internal Miller clamp transistor starts to engage when the Miller clamp pin voltage drops below the 2V (referenced to VEE) threshold, and it provides a low-impedance path to direct the Miller current to VEE. Refer to Figure 7-5 for the internal Miller clamp timing diagram.

The CA-IS3215xEW/CA-IS3216xEW provides external active miller clamp input which drives an external MOSFET. The external MOSFET is triggered when the gate voltage is lower than V_{CLMPTH} (2.0V referenced to VEE, typical) and create a low impedance path to avoid the false turn-on problem of power transistors. Refer to Figure 7-6 for the external Miller clamp timing diagram.

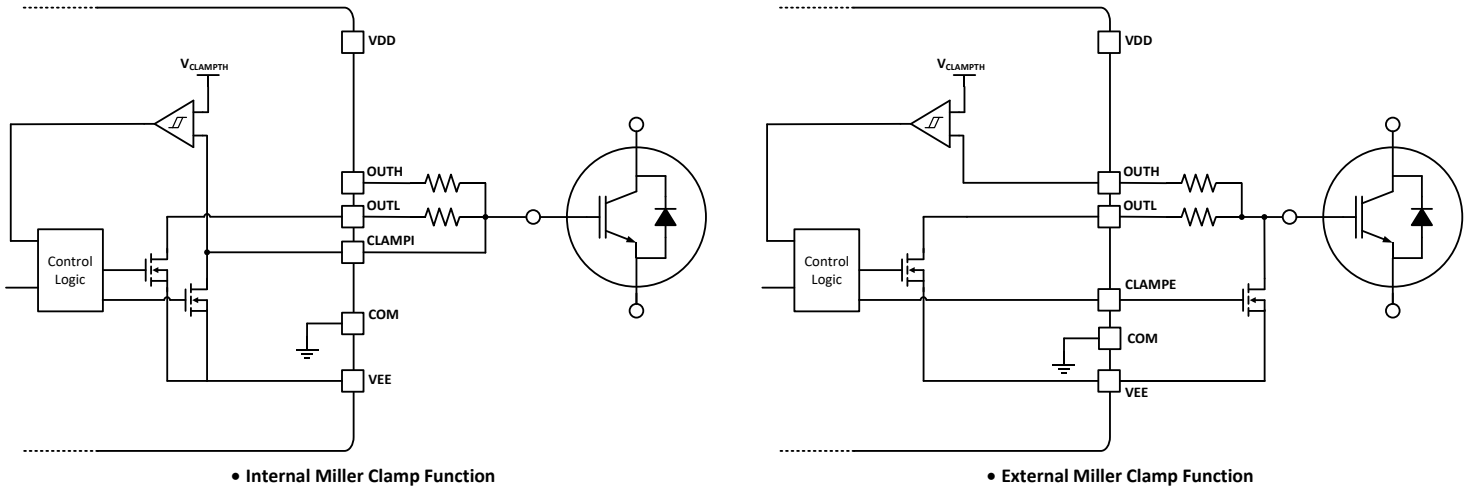


Figure 8-6 Active Miller clamp

8.5.5. Desaturation (DESAT) Protection

The CA-IS3215/6 provides fast-response over-current protection and short-circuit protection to prevent SiC MOSFET or IGBT breakdown under fault conditions. See Figure 8-7 the desaturation detection circuit. The circuit consists of a resistor, a blanking capacitor, and a diode. The IGBT gate-driver CA-IS3215S has 9V fixed DESAT threshold (as shown in Figure 8-7), the SiC MOSFET gate-driver CA-IS3216 has 6V fixed DESAT threshold. When the power transistors turns on, a current source charges the blanking capacitor and the diode is conducted. The typical value of the internal current source is 500μA. During normal operation, the DESAT voltage is clamped at low-level through the internal MOSFET to avoid erroneous triggering of DESAT protection. Also, the internal pulldown MOSFET is used to discharge the voltage of DESAT pin when the power transistors are turned off. The internal current source of the DESAT pin is active only during the driver in ON state, which means the over-current and short-circuit protection only works when the power transistors are in ON state. The CA-IS3215/6 features a 265ns internal leading edge blanking time ($t_{DESATLEB}$) after the OUTH switches to high state. The internal current source is enabled to charge the external blanking capacitor after the internal leading edge blanking time. When short circuit happens, the capacitor voltage is quickly charged to the threshold voltage which triggers the gate-driver turned-off.

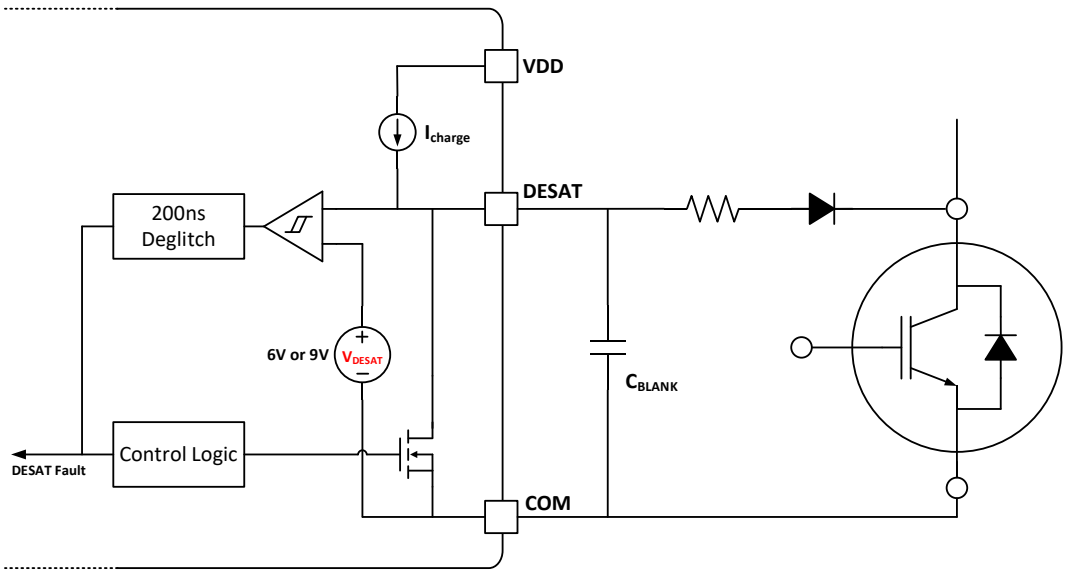


Figure 8-7 DESAT protection

8.5.6. Soft turn-off

When over-current and short-circuit protection is triggered, the CA-IS3215/6 will initial soft turn-off, to turn-off power transistors slowly, see Figure 8-8. When over-current and short-circuit faults occur, IGBT goes through a quick transition from the active region to desaturation region. The collector current of IGBT is limited by gate voltage will be reduced slowly. This can reduce IGBT's overshoot voltage and avoid IGBT breakdown. There is a tradeoff between the overshoot voltage and short-circuit (or over-current) energy. The Soft turn-off time should be designed long enough to limit the overshoot voltage, also the shutdown time must not be too long that the large over-current energy dissipation can breakdown the power transistors. The CA-IS3215 IGBT gate-driver features a 400mA Soft turn-off current, and the CA-IS3216 SiC MOSFET gate-driver features 1A Soft turn-off current, ensure the power devices safely turned-off during short-circuit or over-current occurs. See Figure 7-9 and Figure 7-10 soft turn-off timing diagram.

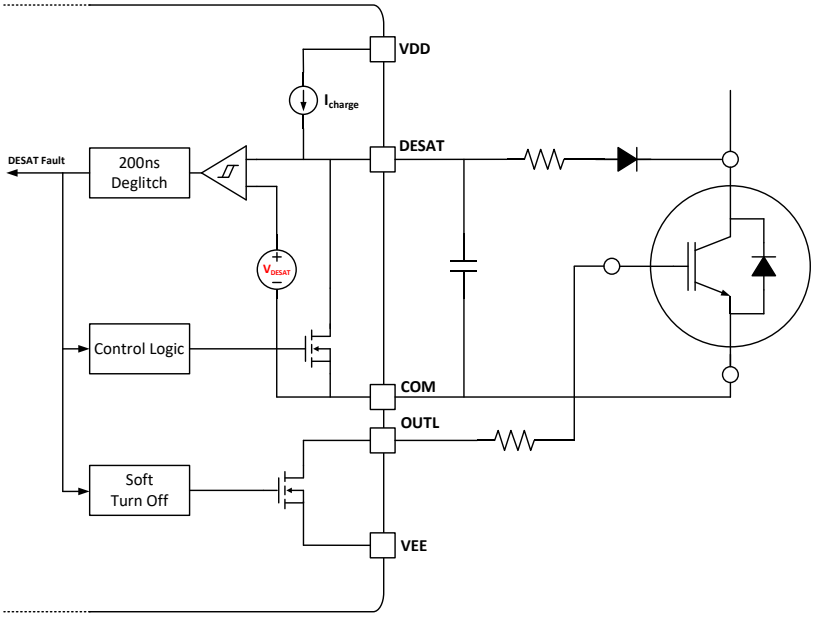


Figure 8-8 Soft turn-off

8.5.7. Active Short Circuit (ASC) Protection

When VCC supply power-down or external controller (DSP/MCU) does not work normally, the motor may lose system control and reverse charge the battery. Overvoltage can cause battery breakdown, even cause serious accidents. In this case, the active short circuit (ASC) control can provide protection for the system by forcing the output to high-level, turning-on the switch, and creating an active short circuit between each phase to protect the battery from damage.

If ASC_ pin receives a logic-high signal, the driver output will be placed in high-level regardless of the input IN+/IN_ status on the control-side. ASC_C input control has a higher priority than the IN+/IN_ input signal. VCC UVLO, $\overline{RST}$/EN and over-current(DESAT) protection have higher priority than ASC_C input control. See more detail in Figure 7-11 and Figure 7-12 about ASC_C protection logic. Figure 7-13 and Figure 7-14 shows the ASC_D control timing.

8.5.8. Shoot-through Protection (STP)

The CA-IS3215/6 isolated gate drivers have internal dead-time control circuit to prevent shoot-through current caused by high-side and low-side power transistors overlap, because this may lead to a potentially damaging short-circuit type condition in the typical applications. The CA-IS3215S_ has 800ns fixed dead-time(t_{DT}), and the CA-IS3216S_ has 140ns fixed dead-time. Connect INN pin to GND to disable STP function. If input's "dead-time" is longer than t_{DT}, the driver's dead-time is dependent on the input dead-time.

See Figure 8-9 shoot-through protection circuit. The dead-time is asserted by input (PWMA or PWMB) signal's falling edge. Only one output (OUTA or OUTB) can will be set high in a practical application. For example, if driver OUTA (or OUTB) is pulled

high, another driver's input PWMB (or PWMA) will be blocked. This feature is used to prevent shoot-through, and it doesn't affect the fixed dead-time setting for normal operation. Figure 8-10 shows various driver dead-time logic and operating conditions.

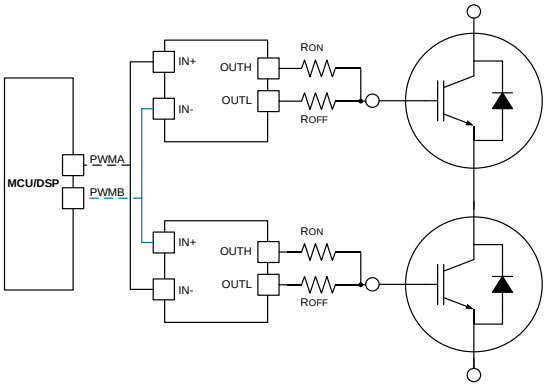


Figure 8-9 Shoot-through protection circuit

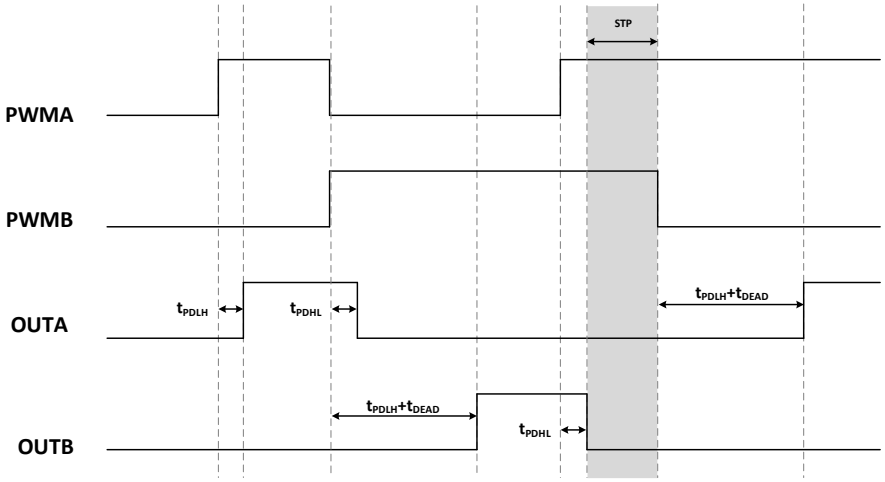


Figure 8-10 Shoot-through protection timing diagram

8.6. Fault Indication and Reset (FLT, RST/EN)

The FLT pin is an open-drain logic output that transitions active low (GND) when a fault condition is detected at DESAT pin. It will keep logic-low until a reset signal is received from RST/EN. The FLT can be used to report fault conditions to the controller (DSP or MCU). The CA-IS3215/6 gate-drivers has $t_{FLTMUTE}$ fixed fault mute time, within which the device ignores any reset signal.

RST/EN is reset and enable control input. It has a 55kΩ internal pulldown and disable the gate-driver at default state. In normal operation, pullup RST/EN externally and enable the gate-driver. This pin has two purposes:

1) Resets the desaturation condition indicator output at pin FLT. Place RST/EN to low for more than t_{RSTFIL} (800ns, maximum) after the mute time $t_{FLTMUTE}$ to assert FLT reset at the rising edge of RST/EN and reset DESAT fault indication latch at pin FLT .
2) Enable/Shutdown control for driver-side. Put RST/EN low for more than t_{INFIL} to disable the driver output and OUTL output pulls the gate of IGBT of SiC MOSFET to low-level to turn-off the external power transistors.

8.7. Device Functional Modes

Table 8-1 shows the CA-IS3215/6 devices functional modes.

Table 8-1 CA-IS3215/6 Inputs vs. Output Truth Table

INPUT								OUTPUT				
VCC	VDD	VEE	IN+	IN-	$\overline{RST}$/EN	ASC_C	ASC_D	RDY	$\overline{FLT}$	OUTH/ OUTL	CLAMPI	CLAMPE
PD	PU	PU	X	X	X	X	High	Low	HiZ	High	HiZ	Low
PD	PU	PU	X	X	X	X	Low	Low	HiZ	Low	Low	High
PU	PU	PU	X	X	X	X	High	HiZ	HiZ	High	HiZ	Low
PU	PU	PU	X	X	Low	X	Low	HiZ	HiZ	Low	Low	High
PU	PD	PU	X	X	X	X	X	Low	HiZ	Low	Low	High
PU	Open	PU	X	X	X	X	X	Low	HiZ	Low	HiZ	HiZ
PU	PU	Open	X	X	X	X	X	Low	HiZ	Low	Low	High
PU	PU	PU	X	X	High	High	X	HiZ	HiZ	High	HiZ	Low
PU	PU	PU	Low	X	High	Low	Low	HiZ	HiZ	Low	Low	High
PU	PU	PU	X	High	High	Low	Low	HiZ	HiZ	Low	Low	High
PU	PU	PU	High	Low	High	Low	Low	HiZ	HiZ	High	HiZ	Low

Notes:

1. X = don't care; HiZ = high-impedance.
2. PU = power up (VCC≥ 2.7V, VDD≥12V, VEE≤0V); PD = power down (VCC≤2.5V, VDD≤11V).

9. Application and Implementation

9.1. Typical Application

CA-IS3215/6 has the characteristics of strong driving ability, high isolation level, excellent CMTI, superior active protection and monitoring function, high reliability, etc., and has been widely used in traction inverters, on-board chargers, charging piles, motor drives, solar inverters, industrial power supplies and other fields in HEV/EV.

See Figure 9-1 the CA-IS3215/6 typical application circuits for IGBT driving.

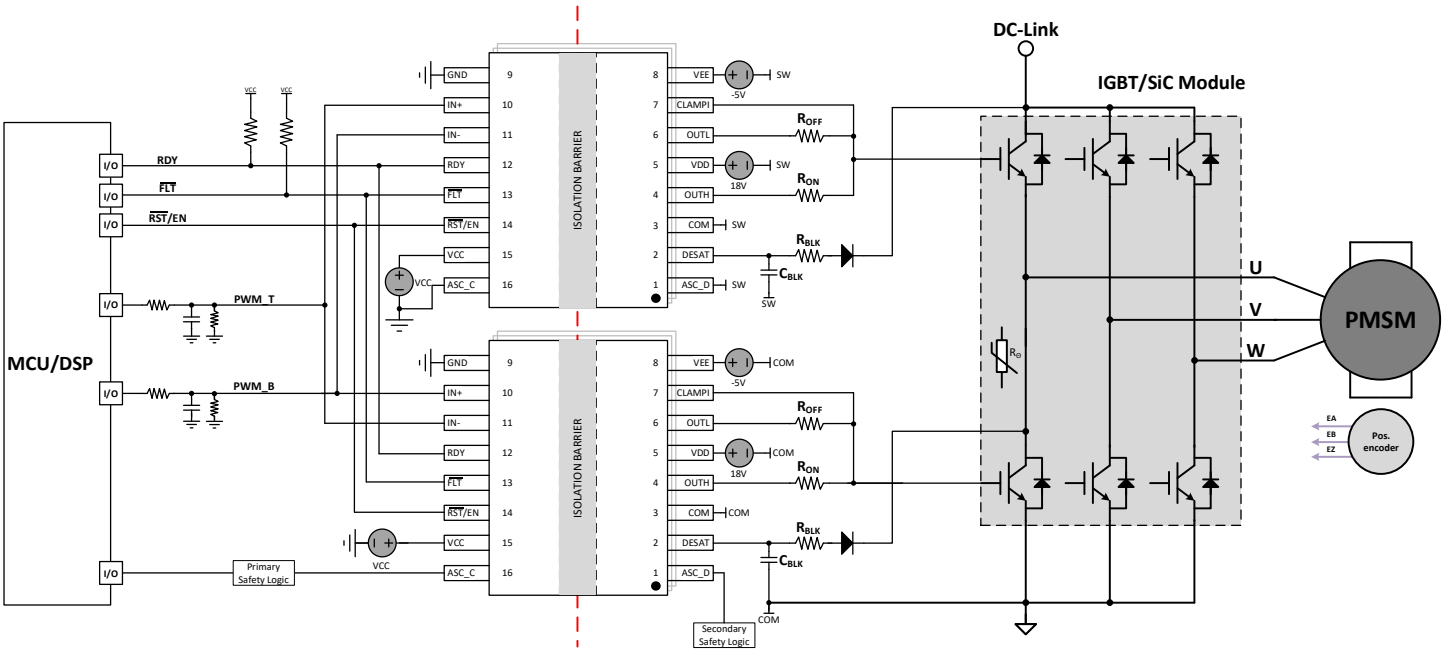


Figure 9-1 The CA-IS3215/6 typical application circuit

9.2. Input Filters

When the OUT switching, the peak source and sink current are provided by the VDD and VEE power supplies. To ensure a stable power supply and provide ±15A peak drive capability, a 10uF/50V decoupling capacitor is recommended for VDD to COM and VEE to COM. A 1μF decoupling capacitor is recommended between VCC and GND on the control side. At the same time, it is recommended to use an additional 0.1μF bypass capacitor per power supply to filter out high-frequency noise. The recommended capacitors must be low ESR and ESL to avoid high-frequency noise, and should be as close as possible to the VCC, VDD, and VEE pins to prevent parasitic coupling noise caused by the PCB layout.

9.3. Input Filters

The CA-IS3215/6 gate drivers feature differential PWM inputs (IN+ and IN_). The differential inputs reject input glitches and prevent false turn-on of the output. The internal filter can keep driver output in the previous state when a glitch or short pulse (<40ns, typical) is detected on either input(IN+, IN–, $\overline{\text{RST}}$/EN and ASC_C). The IN+, IN–, $\overline{\text{RST}}$/EN and ASC_C pins can not leave float if not used. For single-ended input configuration, apply PWM input at IN+ and connect IN_ to GND.

9.4. Interlock configuration

In the typical applications, the gate drivers are used to drive high-side and low-side power transistors. External controller (DSP/MCU) generates complementary PWM pulses during normal operation. However, the controller failures or software faults can cause both the high-side and low-side PWM signals from the DSP/MCU to latch high. Interlock configuration can be used to prevent the output from being high at same time even both high-side and low-side inputs are pulled high. As shown in Figure 9-2, the PWMA is used for high-side IN+ and low-side IN_ control, PWMB is used for low-side IN+ and high-side IN_ control. This architecture prevents both inputs from being "high" at the same time, preventing shoot through in the external power transistors.

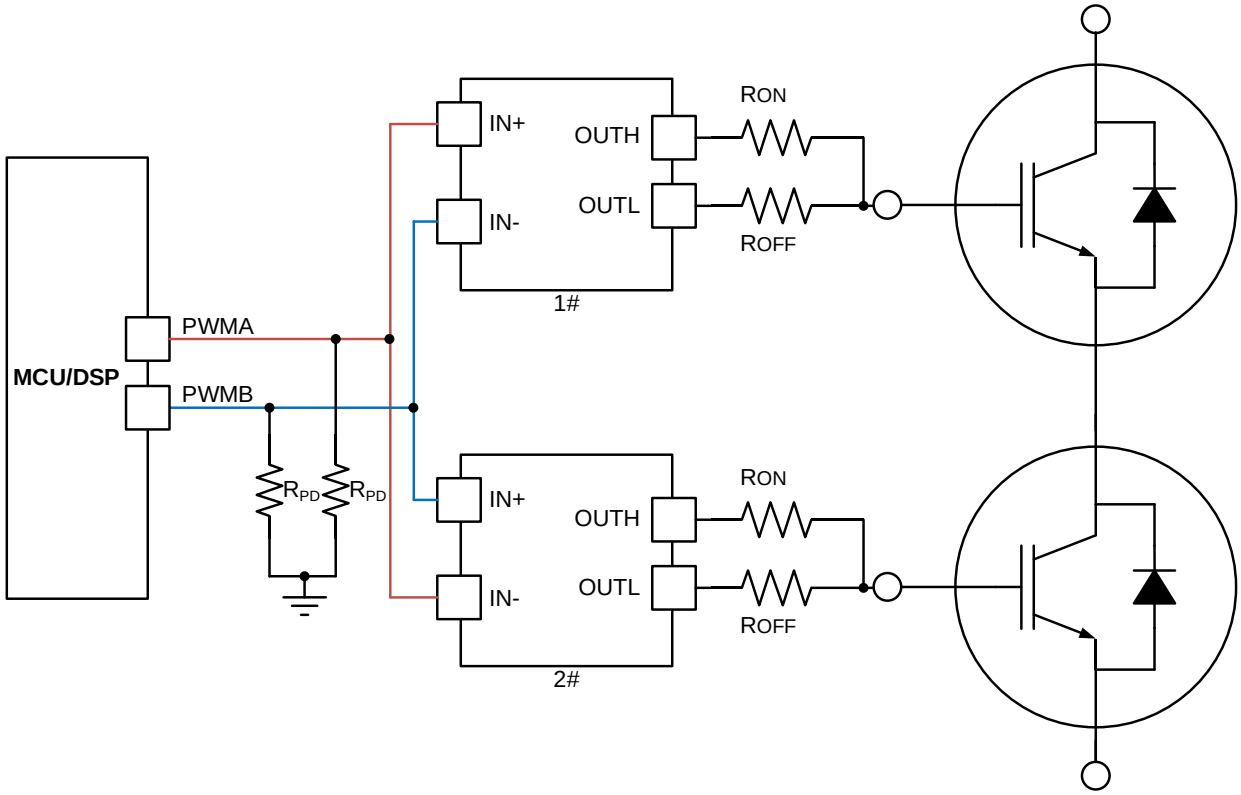


Figure 9-2 The CA-IS3215/6 half-bridge interlock configuration

9.5. $\overline{\text{FLT}}$, RDY pins

Both $\overline{\text{FLT}}$ and RDY pins are open-drain logic output. The $\overline{\text{RST}}$/EN has 57kΩ internal pulldown. For normal operation, pullup $\overline{\text{RST}}$/EN externally and enable the gate-driver. A 5kΩ pull-up resistor is recommended for $\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN inputs. A low pass filters (100pF to 300pF capacitor) can be added between the FLT, RDY and RST/EN pins and GND to improve the noise immunity due to the parasitic coupling and common mode noise.

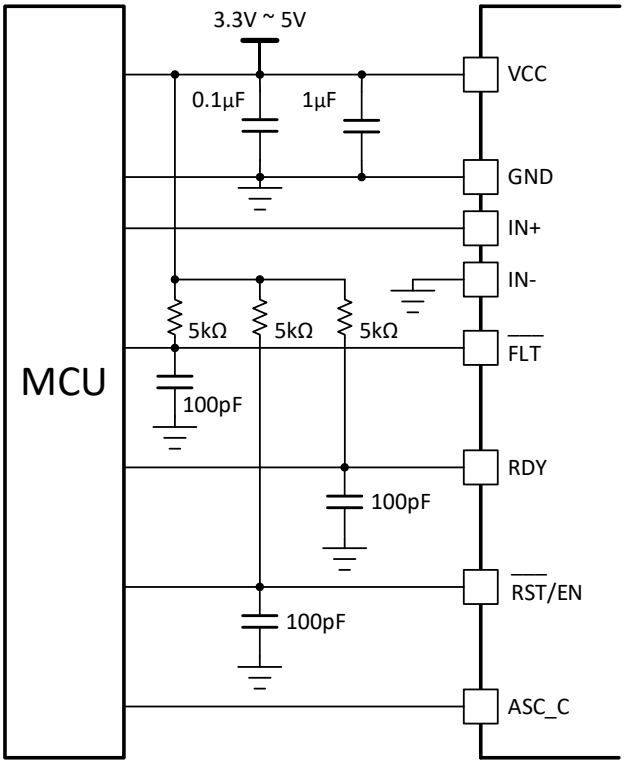


Figure 9-3 $\overline{\text{FLT}}$ and RDY pins connection

9.6. Auto-Reset Control $\overline{RST}$/EN

$\overline{RST}$/EN has two purposes: driver reset and enable/disable control input. The internal 55kΩ pulldown disables the driver in default status. To enable the gate-driver, $\overline{RST}$/EN pin must be pulled up externally. When DESAT is detected, both $\overline{FLT}$ pin and driver outputs are latched low and must be reset by the $\overline{RST}$/EN pin. Place $\overline{RST}$/EN to low for more than t_{RSTFIL} after the mute time $t_{FLTMUTE}$ to assert $\overline{FLT}$ reset and reset DESAT fault indication latch and driver output latch.

Connect IN+ or IN_ to $\overline{RST}$/EN as shown in Figure 9-4, the CA-IS3215/6 gate-driver will be configured as an auto-reset driver. This configuration can save a separate reset signal from external controller. In Figure 9-4, if apply the PWM to the noninverting input IN+, connect IN+ to $\overline{RST}$/EN pin directly; if apply the PWM to the inverting input IN–, then a NOT logic will be needed between the control output and $\overline{RST}$/EN pin. Using either configuration results in the driver being reset in every switching operation. The PWM off-time must be greater than t_{RSTFIL} to ensure reset the driver in cause of a DESAT fault.

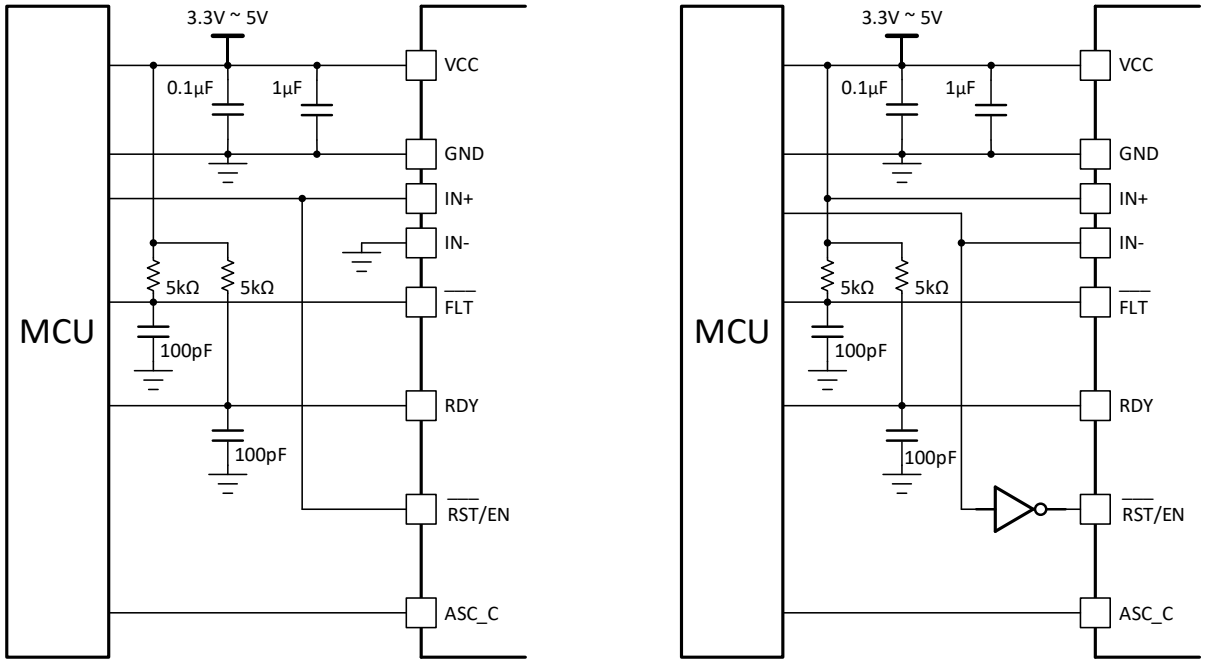


Figure 9-4 Auto-reset configuration

9.7. Gate Driver Resisters Selection

In the typical application circuits, there are two external gate driver resistors: R_{GON} and R_{GOFF}, see Figure 9-1, R_{GOFF} is the external turn-off resistance; R_{GON} is the external turn-on resistance. These two resistors are chosen to limit the current ringing caused by fast switching and parasitic inductances and capacitances, reduce EMI, also can be used to fine-tune gate drive strength and optimize the switching loss. The selection of gate drive resistor is mainly based on three factors: drive current, switch loss, rise and Fall time. The peak gate-current is calculated as follows:

I_{OUTH} peak source current:

$$I_{OUTH} = \min\left[15A, \frac{VDD - VEE}{\left(R_{NMOS}||R_{OUTH} + R_{GON} + R_{GFET_{int}}\right)}\right]$$

I_{OUTL} peak sink current:

$$I_{OUTL} = \min\left[15A, \frac{VDD - VEE}{\left(R_{OUTL} + R_{GOFF} + R_{GFET_{int}}\right)}\right]$$

Where:

- R_{NMOS} is about 0.23Ω; R_{OUTH} is about 1.6Ω.
- R_{GON} is the external turn-on resistance;
- R_{GOFF} is the external turn-off resistance;
- R_{OH_EFF} is internal resistance of pull-up structure, about 2×R_{OL} (0.7Ω);
- R_{OUTL} is internal pulldown resistance, about 0.23Ω;
- R_{GEFT_Int} is the gate resistance of the external power transistor, this number is available from power transistor data sheet.

9.8. Over-current and Short-circuit Protection

Figure 8-7 shows the desaturation detection circuit. The circuit consists of a resistor, a blanking capacitor, and a diode. We recommend to use a fast reverse recovery, high-voltage diode in this DESAT circuit. A resistor is in series with the high-voltage diode to limit the inrush current. In addition, a Schottky diode can be added from COM to DESAT to prevent driver damage caused by negative voltage; a Zener diode can be connected between COM and DESAT to prevent driver damage caused by positive voltage. When short circuit happens, the capacitor voltage is quickly charged to the threshold voltage of DESAT (V_{DESAT}) which triggers the gate-driver Soft turn-off. Fast response for the over-current and short-circuit fault ensure to initial a turn-off control for the SiC MOSFET or IGBT quickly.

The open-drain logic output $\overline{FLT}$ is active low (GND) when a fault condition is detected at DESAT pin. It can be used to report fault conditions to the controller (DSP or MCU). The $\overline{FLT}$ will keep logic-low once asserted until a reset signal is received from $\overline{RST}$/EN.

Connect DESAT pin to COM if desaturation detection is not used.

10. PCB Layout Guidelines

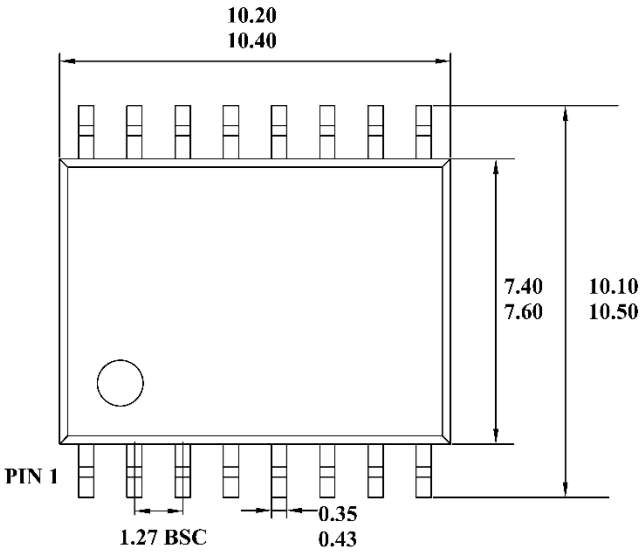
Due to high current levels and fast switching(high dv/dt and di/dt) that radiate noise in the CA-IS3215/6 design, proper PC board layout is essential. The PCB designer should follow some critical recommendations as below in order to get the best performance.

- To ensure the best performance and keep lower supply ripple, place the decoupling capacitors as close to the power-supply pins as possible. We recommend to use low ESR, low ESL MLCC capacitors.
- Driver outputs connection carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency-switching operation. This implies that the driver output loop areas should be minimized. Additionally, small current loop areas reduce radiated EMI. Place the external transistor as close to the gate driver as possible to decrease the trace inductance and avoid output ringing. The Kelvin method is recommended to connect COM to the source of SiC MOSFET or emitter of IGBT.
- If the gate driver is used for the low-side driving which the COM pin connected to the power supply bus negative, use a solid ground plane on driver-side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high-side driving which the COM pin is connected to the switch node, ground plane is not recommended.
- If ground plane is not used on driver-side, separate the return path of the DESAT and ASC_D ground loop from the gate loop ground which has high peak source and sink current.
- Keep the control input traces as short as possible. To maintain low signal-path inductance, avoid using vias. Have a solid ground plane on the control-side to shield the input signals.
- To ensure isolation performance between the control-side and driver-side, on the top layer and bottom layer keep the space under the CA-IS3215/6 device free from traces, vias, and pads to maintain maximum creepage distance.
- If the user does not use the VEE negative power supply, the VEE to COM pins must be connected at the shortest distance so that OUTL does not generate di/dt flow through the PCB parasitic inductance to generate a voltage drop during high-current shutdown, which may result in the VEE voltage being greater than COM, and triggering the chip protection mechanism.
- For CA-IS3215LNW and CA-IS3215ENW products, the VEE pin of PIN 1 should be connected to the VEE pin of PIN 8, and the PIN 1 pin should not be floating.

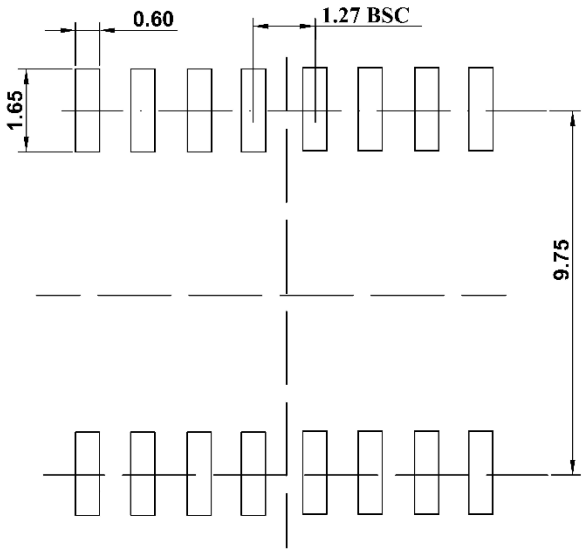
11. Package Information

16-Pin Wide Body SOIC Package

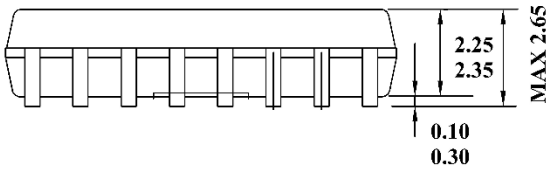
The following diagrams provide the package details and the recommended land pattern details for the CA-IS3215/6xxW-Q1 isolated gate driver in 16-pin wide body SOIC package. All values for the dimensions are shown in millimeters.



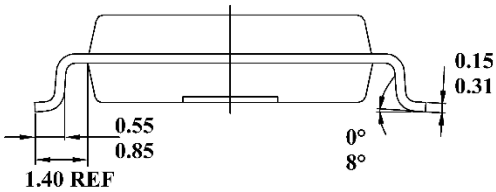
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature (reflow) Profile

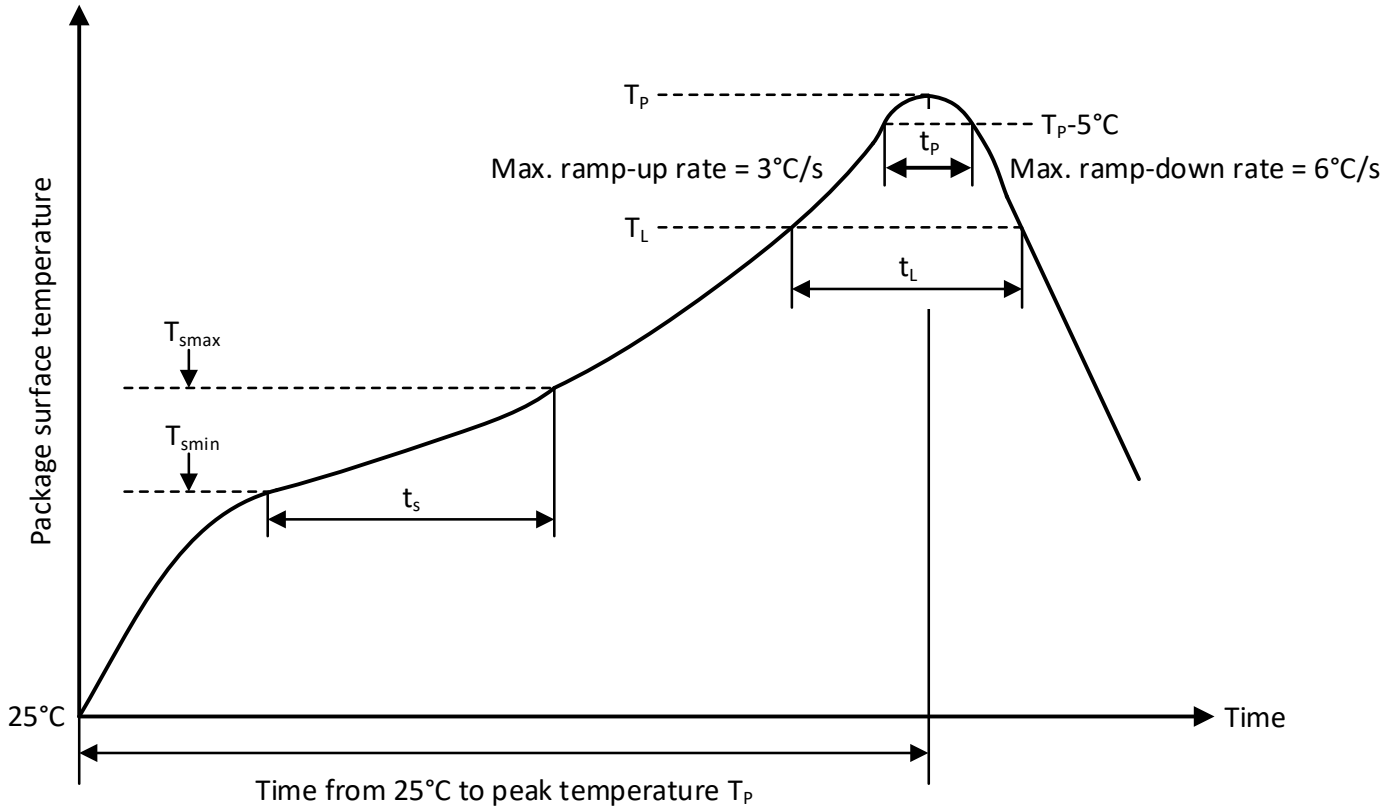


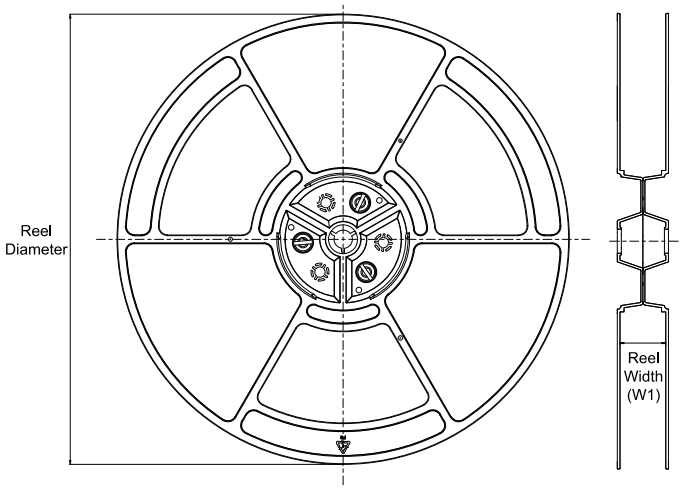
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

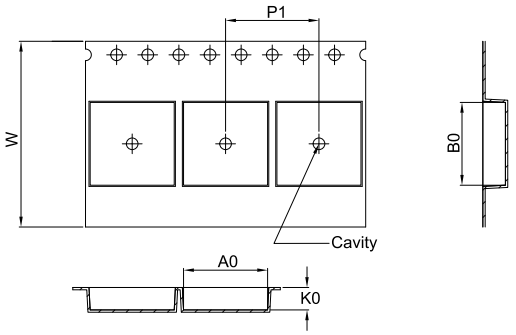
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217°C to Peak)	3°C /second max
Time of Preheat temp(from 150°C to 200°C	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0°C
Time within 5°C of actual peak temp	30 second
Ramp-down rate	6 °C /second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

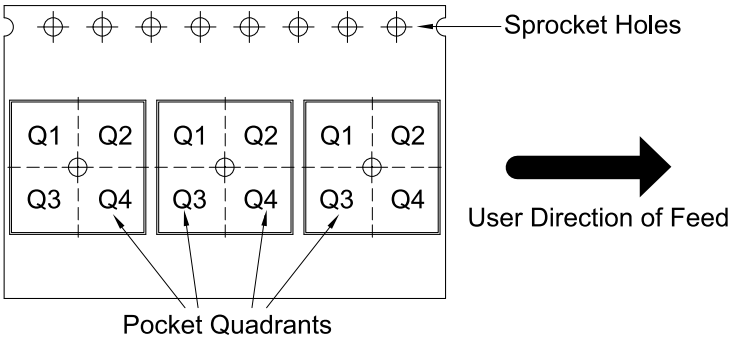


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3215NNW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3215LNW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3215ENW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3215VNW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3215NEW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3215SNW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3215SEW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3216NNW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3216NEW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3216SNW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3216SEW-Q1	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

14. Revision History

Revision Number	Description	Revised Date	Page Changed
Version1.0	1. Update the certificate information of VDE、UL、CQC	2024/04/16	1,11
Version1.1	1. Add heat information ($R_{\theta JC(top)}$ and $R_{\theta JB}$) 2. Updated isolation characteristics and authentication information 3. Updated Figure 7-1 and Figure 7-2 Propagation Delay Measurement. 4. Updated PCB design recommendations 5. Updated POD information	2025/05/19	8 9,10 17 43 44

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