CA-IF1169 High-speed CAN System Basis Chip with LDO and Watchdog

1. Features

- Meets the requirements of ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 physical layer standards
- ASIL-B compliant: designed with complete functional safety development process, supporting customer to achieve ASIL-B certification
- CAN FD Support: enables CAN FD data transmission up to 5 Mbit/s
- Support selective wake to wake-up specific partial networking nodes
- CAN bus pins short-circuit protection to ±42 V, ideal for 12V battery systems
- Autonomous bus biasing
- Integrated dual low-drop voltage regulators (LDO):
  - LDO 1 (V1): 3.3V and 5V output voltage option with up to 250mA output current capability. Supports current extension via an external PNP transistor for increased output capacity, to provide power supply for system microcontroller or other loads
  - LDO 2 (V2): 5V output voltage with up to 100mA output current capability, provide power supply for internal CAN transceiver and other loads.
- Advanced ECU power management
  - Ultra-low power consumption in sleep mode: 12.8μA (typical)
  - Remote wake-up via standard CAN wake-up pattern(WUP) or selective wake-up frame (WUF) according to ISO 11898-2:2016
  - Selective wake supports 50kbit/s, 100kbit/s, 125kbit/s, 250kbit/s, 500kbit/s and 1Mbit/s CAN bit-rate
  - Local wake-up via WAKE terminal, also local wake-up can be disabled to reduce power consumption
  - Wake-up sources identification
- Integrated protection and diagnosis increase system robustness
  - 16/24/32 bit SPI-compatible interface for device configuration, control and events diagnosis
  - Transmitter dominant timeout prevents lockup
  - Configurable watchdog timer
  - Cyclic wake-up in watchdog timeout mode
  - Overtemperature shutdown and alarm
  - Undervoltage protection on BAT supply terminal
  - LDO V1/LDO V2 overvoltage and undervoltage detection and protection
  - Cold start-up detection (PO and NMS bits)
  - Battery, WAKE and CAN bus pins protected against transients according to ISO 7637-3, test pulses 1, 2a, 3a and 3b
  - Advanced system and transceiver interrupt process
  - Integrated analog circuit initiate self-test (ABIST) and stuck monitoring on critical interfaces.
- Dedicated LIMP output to indicate system failure and guide the system into limp-home mode
- Multiple time programmable(MTP) non-Volatile(NV) memory:
  - Support multiple online debugging configuration and two-times programmability
  - Configurable power-up and reset behaviors and the system basis chip operating modes for different applications
- –40°C to 150°C junction temperature range
- Complies with the AEC-Q100 Grade 1 standard for automotive applications
- Available in DFN20 package (wettable flank)

2. Applications

- Body electronics
- Automotive lighting systems
- Advanced driver assistance systems (ADAS)
- Thermal management systems for new energy vehicles
- Automotive sensors
- In-car entertainment systems
- Automotive power train systems

3. General Description

The CA-IF1169 is a system basis chip(SBC) with integrated high-speed CAN(controller area network) transceiver and dual LDOs. The CAN transceiver complies with ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 standards for high-

speed CAN physical layer specifications, supporting up to 5 Mbit/s CAN FD communication. These devices feature up to ±42V extended fault protection on the data transmission lines in all operation modes. Also, the dominant timeout detection can prevent bus lockup caused by controller error or by a fault on the TXD input.

The CA-IF1169 SBC can operate in different modes: normal operation, reset mode, overtemperature protection mode, and standby/sleep modes for low current consumption. In the low-power standby and sleep modes, the CA-IF1169 supports remote wake-up (WUP) or selective wake-up frame(WUF) as defined by ISO 11898-2:2016, and local wake-up through the WAKE pin.

The CA-IF1169 integrates two low-drop voltage regulators (LDO V1 and LDO V2). LDO V1 provides 3.3V or 5V output voltage option with up to 250mA output current capability, see Table 5-1. Ordering Information. Also, its current capacity can be extended via an external PNP transistor, enabling it to power the system microcontroller or other on-board loads. LDO V2 provides 5V output voltage with up to 100mA output current to support the internal CAN transceiver and other loads supply. Internal LDO output option simplifies the interface with 3.3V or 5.0V CAN controllers. SPI-compatible interface is available for transceiver operation control and status information reading.

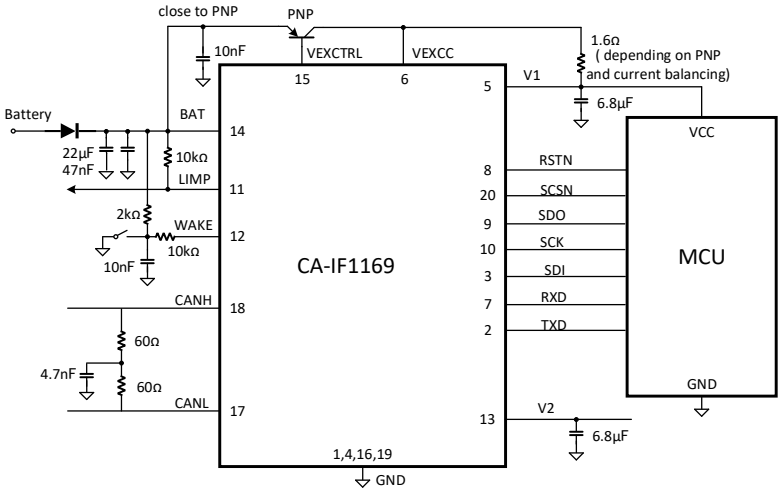
The CA-IF1169 follows a comprehensive functional safety development process with integrated analog circuit initiate self-test (ABIST), critical interface monitoring. The dedicated LIMP output pin for failure indication can be used to guide the system into limp-home mode. These devices comply with ISO 26262 ASIL-B standard and support customer to achieve ASIL-B certification for their end products.

The CA-IF1169 family of devices is available in 20-pin DFN package, operates over the -55°C to +150°C junction temperature range.

Device Information

Part number	Output voltage of V1	Watchdog	Package	Package size(NOM)
CA-IF1169WDT-Q1	5V	Autonomous / Timeout / Window	DFN20	3.5mm x 5.5mm
CA-IF1169VWDT-Q1	3.3V	Autonomous / Timeout / Window		
CA-IF1169FDT-Q1	5V	Autonomous / Timeout		
CA-IF1169VFDT-Q1	3.3V	Autonomous / Timeout		

4. Typical application block diagram



5. Ordering Information

Table 5-1. Ordering Information

Part Number	Features		Package size
	Recommended power supply	Partial awakening	DFN20
CA-IF1169FDT-Q1	5V V1 to MCU & 5V V2 to CAN	YES	3.5mm x 5.5mm
CA-IF1169VFDT-Q1	3.3V V1 to MCU & 5V V2 to CAN	YES	3.5mm x 5.5mm
CA-IF1169WDT-Q1	5V V1 to MCU & 5V V2 to CAN	YES	3.5mm x 5.5mm
CA-IF1169VWDT-Q1	3.3V V1 to MCU & 5V V2 to CAN	YES	3.5mm x 5.5mm

Contents

6. Revision History

Revision Number	Description	Page Changed
Ver.1.0	NA	2025.7.2

7. Pin Configuration and Functions

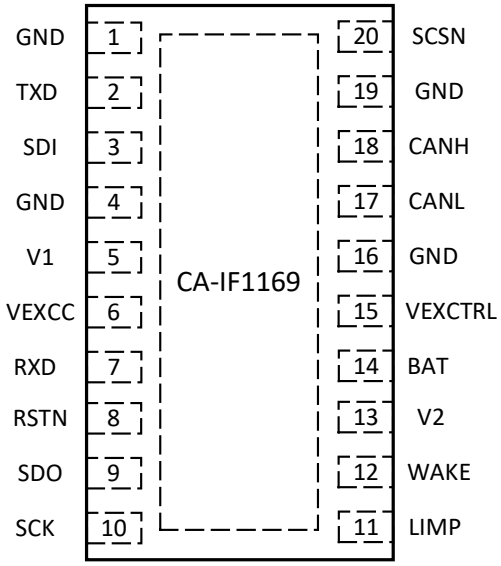


Figure 7-1. CA-IF1169 pin configuration

Table 7-1. CA-IF1169 pin configuration and description

Pin Name	Pin#	Type	Description
GND	1, 4, 16, 19	GND	Ground.
TXD	2	Digital input	Transmit Data Input. In normal operation, drive TXD high to set the driver in the recessive state; drive TXD low to set the driver in the dominant state. TXD is a CMOS/TTL compatible input from a CAN controller with an internal pull-up to V1.
SDI	3	Digital input	SPI Serial Data Input. Data is clocked into SDI on the rising edge of SCK.
V1	5	Power	5V or 3.3V power supply output.
VEXCC	6	Analog input	Current sense for external PNP transistor, connect VEXCC to the collector of the external PNP transistor.
RXD	7	Digital output	Receive Data Output. In normal operation, RXD is low for dominant bus state and high for recessive bus state. RXD is a CMOS/TTL compatible output from the bus lines CANH and CANL.
RSTN	8	Digital input /output	Reset input/output, active low.
SDO	9	Digital output	SPI Serial Data Output. Data is updated on the falling edge of SCK. When SCSN is high, SDO is high-impedance.
SCK	10	Digital input	SPI Serial Clock Input. SCK has internal pull-down.
LIMP	11	Analog output	Limp home output, active-low, open-drain output.
WAKE	12	High-voltage input	Local Wake-up Input. If enabled, either a low-to-high (rising edge) or a high-to-low (falling edge) transition will generate a local wake-up event. Pull WAKE to ground to avoid unwanted wake-up events if not used.
V2	13	Power	5V power supply output.
BAT	14	Power	Battery Supply Input. A bulk capacitance, typically 10μF, should be placed BAT supply with a 100nF capacitor place near the BAT terminal.
VEXCTRL	15	Analog output	Control pin of external PNP transistor, connect VEXCTRL to the base of the external PNP transistor.
CANL	17	Bus I/O	CAN bus line low.
CANH	18	Bus I/O	CAN bus line high.
SCSN	20	Digital input	SPI Chip-Select Input. Assert low to latch input states and enable the SPI interface.

8. Specifications

8.1. Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{BAT}	Battery supply voltage range	-0.3	42	V
$V_{(V1, V2)}$	LDO output voltage	-0.3	6	V
$V_{(VEXCC)}$	Collector of the external PNP transistor connection	-0.3	6	V
$V_{(LIMP, VEXCTRL)}$	LIMP, VEXCTRL voltage	-0.3	42	V
V_{BUS}	CAN bus I/O voltage range (CANH,CANL)	-42	42	V
$V_{(DIFF)}$	Max differential voltage between CANH and CANL	-42	42	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range (TXD, SDI, SCK, SCSN, RSTN)	-0.3	V_{V1}+0.3	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range (RXD, SDO)	-0.3	V_{V1}+0.3	V
$V_{(wake)}$	WAKE input voltage range	-0.3	42	V
$I_{O (LOGIC)}$	Logic output current (RXD)		4	mA
$I_{O (WAKE)}$	WAKE output current		3	mA
$I_{I (LIMP)}$	Limp mode current		20	mA
T_J	Virtual junction temperature range	-40	150	°C

Note:

1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

8.2. ESD Ratings

Parameters	TEST CONDITIONS		VALUE	UNIT
CA-IF1169-Q1				
HBM ESD	CAN bus terminals (CANH, CANL) to GND		±8000	V
	Other pins		±2000	
CDM ESD	All pins		±1500	V
System Level ESD	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2: unpowered contact discharge.	±6000	V
	BAT (with 100nF capacitor), WAKE (with 10nF capacitor and 10k resistor) to GND	IEC 61000-4-2: unpowered contact discharge.	±8000	V
ISO7637 transient according to GIFT-ICT CAN EMC test	CAN bus terminals (CANH, CANL) to GND VBAT, WAKE terminals to GND	Pulse 1	-100	V
		Pulse 2	+75	V
		Pulse 3a	-150	V
		Pulse 3b	+100	V
ISO7637-3 transient	CAN bus terminals (CANH, CANL) to GND VBAT, WAKE terminals to GND	Direct coupling 100nF capacitor "slow transient pulse" – powered.	±85	V

Note:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.

8.3. Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
V_{BAT}	Battery supply voltage range	4.5	28	V
I_{OH}(RXD)	RXD terminal high level output current	-2		mA
I_{OL}(RXD)	RXD terminal low level output current		2	mA
T_A	Ambient temperature	-40	125	°C

8.4. Thermal Information

Thermal Metric		CA-IF1169 DFN20	UNIT
$R_{\theta JA}$	IC junction to ambient	33.5	°C/W

8.5. Electrical Characteristics

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Battery power supply						
I_{BAT}	Battery Supply Current	Normal operation: MC=111, $V_{TXD} = V_{V1}$, CAN recessive		4	7.5	mA
		Normal operation: MC=111, V_{TXD} = 0V, CAN dominant		46	67	mA
		Sleep mode, MC=001, CWE=1; CAN bus offline mode		12.8	28	μA
		Standby mode, MC=100, CWE=1; CAN bus offline mode		56	91	μA
		V2 turn-on		8	32	μA
		CAN bus offline bias mode		460		μA
		CAN offline bias mode with active partial networking decoder		0.9		mA
		WAKE input current, WPRE = WPFE = 1		1.4	2.5	μA
$V_{th(det)pon}$	BAT power-on detection	Rising	4		4.9	V
$V_{th(det)poff}$	BAT power-off detection	Falling	2.8		3	V
$V_{BAT(OVR)}$	BAT over-voltage (OV) threshold	Rising	31	33	35	V
$V_{BAT(OVF)}$	BAT OVLO recovery voltage	Falling	29	31	33	V
Power supply output (V1)						
Vo	Output voltage	$Vo_{(V1)nom}$=5V, VBAT =5.5V to 28V, I_{V1}=-200mA to 0mA	4.9	5	5.1	V
		$Vo_{(V1)nom}$=5V, VBAT =5.65V to 28V, I_{V1}=-250mA to 0mA	4.9	5	5.1	V
		$Vo_{(V1)nom}$=5V, VBAT < $V_{th(det)poff}$ and rising, t ≤ $t_{startup}$, Tvj ≤ 125°C			5.5	V
		$Vo_{(V1)nom}$=3.3V, VBAT =3.834V to 28V, I_{V1}=-200mA to 0mA	3.234	3.3	3.366	V
		$Vo_{(V1)nom}$=3.3V, VBAT =3.984V to 28V, I_{V1}=-250mA to 0mA	3.234	3.3	3.366	V
$\triangle V_{ret(RAM)}$	RAM retention voltage difference	VBAT = 2 V ~ 3 V; IV1 = −2 mA			100	mV
		VBAT = 2 V ~ 3 V; IV1 = −200 μA			10	mV
$R_{ON(BAT-V1)}$	On-resistance between pin BAT and pin V1	5V output version, VBAT = 2.8 V ~ 5.65 V; IV1 = −250 mA			3.2	Ω
		3.3V output version, VBAT = 2.8 V ~ 3.90 V; IV1 = −250 mA			3.2	Ω
V_{uvd}	V1 undervoltage detection threshold	5V output version, Vuvd(nom) = 90 %	4.5		4.75	V
		5V output version, Vuvd(nom) = 80 %	4		4.25	V
		5V output version, Vuvd(nom) = 70 %	3.5		3.75	V
		5V output version, Vuvd(nom) = 60 %	3		3.25	V
		3.3V output version, Vuvd(nom) = 90 %	2.97		3.135	V
V_{uvr}	Under-voltage recovery threshold	5V output version	4.5		4.75	V
		3.3V output version	2.97		3.135	V
$V_{th(OVP)}$	Over-voltage detection and recovery threshold	5V output version	5.4		5.8	
		3.3V output version	3.45		3.7	V
I_{sink}	Sink current	VBAT = 5.65 V ~ 18 V	214			mA
$I_{O(sc)}$	Short-circuit output current		-500		-250	mA
$I_{DD(CAN)intV1}$	V1 supports CAN supply current[1]	Normal operation: MC=111, CAN active, dominant, V_{TXD}=0V, bus shorted, −3V < (VCANH = VCANL) < +18 V			95	mA

Note1：CA-IF1169VFDT/FDT/WDT/VWDF-Q1 all do not support powering the CAN module through V1. This parameter is only reserved for future versions of the part number that will support CAN power supply with V1.；

Electrical Characteristics (continued)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PNP base, pin VEXCTRL						
$I_{O(sc)}$	Short-circuit output current	VVEXCTRL ≥ 4.5 V; VBAT = 6 V to 28 V	4.2	6.2	7.5	mA
$I_{th(act)PNP}$	PNP turn-on threshold current	PDC=0			130	mA
		PDC=0; Tvj = 150 °C	60	83	100	mA
		PDC =1			80	mA
		PDC =1; Tvj = 150 °C	36	50	59	mA
$I_{th(deact)PNP}$	PNP turn-off threshold current	PDC =0			70	mA
		PDC =0; Tvj = 150 °C	26	44	59	mA
		PDC =1			18	mA
		PDC =1; Tvj = 150 °C	6	11	17	mA
$V_{th(Ictrl)PNP}$	PNP current control threshold voltage	Pin BAT rising edge	5.9		7.5	V
PNP collector						
$V_{th(act)Ilim}$	Current-limit enable threshold voltage	Measure the voltage on the resistor between pin VEXCC and pin V1; 2V ≤ V_{V1} ≤ 5.5 V; 6V < V_{BAT} < 28 V	300		450	mV
V2						
Vo	Output voltage	VBAT = 5.8 V ~ 28 V; IV2 = –100 mA ~ 0 mA	4.9	5	5.1	V
$V_{th(uvp)}$	Under-voltage protection threshold	detection and recovery threshold	4.5		4.75	V
$V_{th(ovp)}$	Over-voltage protection threshold	detection and recovery threshold	5.2		5.5	V
$R_{ON(BAT-V2)}$	On-resistance between pin BAT and pin V2	VBAT = 4.5 V ~ 5.8 V; IV2 = –100 mA ~ –5 mA			8.7	Ω
$I_{O(sc)}$	Short-circuit output current		-250		-100	mA
$I_{DD(CAN)intV2}$	V2 supports CAN supply current	Normal operation: MC=111, CAN active, dominant , V_{TXD}=0V, bus shorted, –3V < (VCANH = VCANL) < +18 V			95	mA
Limp-home output: LIMP						
Vo	Output voltage	ILIMP = 0.8 mA; LHC = 1; Tvj = –40 °C ~$T_{th(act)otp(max)}$			0.4	V
I_{LO}	Output leakage current	VLIMP = 0 V ~ 28 V; LHC = 0	-5		5	µA
Logic interface (SDI, SCK, SCSN inputs)						
$V_{th\ (sw\ )}$	Switching threshold voltage		0.25xV_{V1}		0.75xV_{V1}	V
Vth(sw)hys	Switching threshold voltage hysteresis		0.05xV_{V1}			V
$R_{pd(SCK)}$	SCK pull-down resistance		40	60	80	kΩ
$R_{pd(SCSN)}$	SCSN pull-up resistance		40	60	80	kΩ
$R_{pd(SDI)}$	SDI pull-down resistance	V_{SDI}<$V_{th(sw)}$	40	60	80	kΩ
$R_{pu(SDI)}$	SDI pull-up resistance	V_{SDI}>$V_{th(sw)}$	40	60	80	kΩ
C_i	Input capacitance[1]	V_i=V_{v1}		3	6	pF
Logic output (SDO output)						
V_{OH}	High-level output voltage	I_{oH}=-4mA,	V_{V1}-0.4			V
V_{OL}	Low-level output voltage	I_{oL}=+4mA,			0.4	V
$I_{LO(off)}$	Output leakage current @ off mode	V_{SCSN}=V_{V1}, Vo=0V to V_{V1}	-5		5	µA
C_O	Output capacitance[2]	SCSN = V_{V1}		3	6	pF
Note2: Not tested in production; guaranteed by design.						
Logic interface (TXD input)						
$V_{th\ (SW\ )}$	Switching threshold voltage		0.25xV_{V1}		0.75x V_{V1}	V
Vth(sw)hys	Switching threshold voltage hysteresis		0.05xV_{V1}			V
$R_{pu(TXD)}$	TXD pull-up resistance		40	60	80	kΩ

Electrical Characteristics (continued)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic interface (RXD output)						
V_{OH}	High-level output voltage	Io = -4mA	V_{V1}-0.4			V
V_{OL}	Low-level output voltage	Io = +4mA			0.4	V
$R_{pu(RXD)}$	RXD pull-up resistance	CAN offline mode	40	60	80	kΩ
WAKE interface (WAKE input)						
$V_{th(sw)r}$	High-level input voltage		2.8	3.5	4.1	V
$V_{th(sw)f}$	Low-level input voltage		2.4	3.1	3.75	V
$V_{hys(i)}$	Input threshold hysteresis		250	400	800	mV
I_i	Low-level input leakage current	Tvj = –40 °C to +85 °C			1.5	μA
CAN bus driver						
$V_{O(DOM)}$	Bus output voltage (dominant)	TXD=Low, RL=50 -65Ohm, CANH, see Figure 9-1	2.75	3.5	4.5	V
		TXD=Low, RL=50 -65Ohm, CANL, see Figure 9-1	0.5	1.5	2.25	V
$V_{O(DOM)}$	Bus output differential voltage (dominant)	TXD=Low, RL=45-70 Ohm, RCM open, see Figure 9-1	1.5		3	V
		TXD=Low, RL=2240 Ohm, RCM open, see Figure 9-1	1.5		5	V
$V_{O(REC)}$	Bus output voltage (recessive)	CAN active, TXD=High, no load, CANH/CANL, see Figure 9-1	2	0.5xV_{CAN}	3	V
		CAN offline bias/listen-only mode, TXD=High, no load, CANH/CANL, see Figure 9-1	2	2.5	3	V
		CAN offline mode, TXD=High, no load, CANH/CANL, see Figure 9-1	-0.1		0.1	V
$V_{OD(REC)}$	Bus output differential voltage (recessive)	CAN active/offline bias/listen-only mode, TXD=High, no load, CANH/CANL, see Figure 9-1	-50		50	mV
		CAN offline mode, TXD=High, no load, CANH/CANL, see Figure 9-1	-200		200	mV
$I_{OS(SS\_DOM)}$	Short-circuit current (dominant)	TXD=Low, CANL open, CANH from -15V to 27V, see **错误!未找到引用源。**	-90		6	mA
		TXD=Low, C ANH open, CANL from -15V to 27V, see **错误!未找到引用源。**	-6		90	mA
$I_{OS(SS\_REC)}$	Short-circuit current (recessive)	TXD=High, VBUS from -27V to 32V, see **错误!未找到引用源。**	-3		3	mA
V_{sym}	Transient symmetry (dominant or recessive)	RL=60 Ohm, C_{split}=4.7nF, RCM open, TXD=250kHz, 1MHz, 2.5MHz, V_{sym}=V_{CANH}+V_{CANL}	0.9xV_{CAN}		1.1xV_{CAN}	V
V_{sym_dc}	DC Output symmetry (dominant or recessive)	RL=60 Ohm, R_{CM} open, V_{sym_dc}=V_{CC}-V_{CANH}-V_{CANL}	-0.4		0.4	V

Electrical Characteristics (continued)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN receiver (TXD = High, CANH/CANL drive externally)						
V_{CM}	Common-mode input range	Normal mode/standby mode, RXD output valid, see Figure 9-2	-12		+12	V
V_{IT}	Input threshold voltage at active/listen-only modes	Vcm from -12V to 12V, see Figure 9-2	500		900	mV
$V_{IT(STB)}$	Input threshold voltage at offline mode	Vcm from -12V to 12V, see Figure 9-2	400		1150	mV
V_{DIFF_D}	Input differential threshold voltage at normal/listen-only modes (dominant)	Vcm from -12V to 12V, see Figure 9-2	0.9		9	V
V_{DIFF_R}	Input differential threshold voltage at normal/listen-only modes (recessive)	Vcm from -12V to 12V, see Figure 9-2	-4		0.5	V
$V_{DIFF\_D(STB)}$	Input differential threshold voltage at offline mode (dominant)	Vcm from -12V to 12V, see Figure 9-2	1.15		9	V
$V_{DIFF\_R(STB)}$	Input differential threshold voltage at offline mode (recessive)	Vcm from -12V to 12V, see Figure 9-2	-4		0.4	V
$V_{DIFF\_(HYST)}$	Differential input threshold hysteresis	Normal mode		100		mV
R_{IN}	CANH/CANL input resistance	TXD=High, STB=0V, Vcm from -30V to 30V	10	15	26	kΩ
R_{DIFF}	Differential input resistance	TXD=High, STB=0V, Vcm from -30V to 30V	20	30	52	kΩ
$R_{DIFF\ (M)}$	Input resistance matching	CANH=CANL=5V	-1		1	%
I_{LKG}	Input Leakage Current	V_{BAT} = 0V, VCAN=5V	-5		5	μA
C_{IN}	Input capacitance[2]	CANH or CANL to GND, TXD = high		30		pF
C_{IN_DIFF}	Differential input capacitance[3]	CANH to CANL, TXD = high		18		pF
IL	Leakage current	VBAT = VCAN = 0 V or VBAT = VCAN connect 47 kΩ resistor to GND; VCANH = VCANL = 5 V	-5		5	μA
Vuvd(CAN)	CAN under-voltage detection	BAT pin voltage V_{BAT} falling	4.2		4.55	V
		V_{CAN}	4.5		4.75	V
Vuvr(CAN)	CAN undervoltage recovery threshold	V_{BAT} rising	4.5		5	V
		V_{CAN}	4.5		4.75	V
IDD(CAN)	CAN supply current	CAN active; recessive ; VTXD = VV1	1	3.7	6	mA
		CAN active; dominant; VTXD = 0 V; no RL load	3	6	15	mA
Note 2,3: Not tested in production; guaranteed by design.						
Temperature protection						
$T_{th(act)otp}$	Thermal shutdown temperature		160	170	185	°C
$T_{th(rel)otp}$	Thermal shutdown release threshold temperature		125	135	145	°C
$T_{th(warn)otp}$	Overtemperature alarm threshold		125	135	145	°C
Reset output: pin RSTN						
VOL	Low-level output voltage	VV1 = 1.0 V~5.5V; pull-up resistance to $V_{V1} \geq$ 900 Ω	0		$0.2xV_{V1}$	V
Rpu	Pull-up resistance		40	60	80	kΩ
Vth(sw)	Switching threshold voltage		$0.25xV_{V1}$		$0.75xV_{V1}$	V
Vth(sw)hys	Switching threshold voltage hysteresis		$0.05xV_{V1}$			V
NV memory						
$n_{cyc(W)}$	Number of MTP write cycles	VBAT = 6 V ~ 28 V; Tvj = 0 °C ~ +125 °C	2			

8.6. Dynamic Characteristics

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN transceiver: CANH, CANL, TXD and RXD						
$t_{d(TXD-busdom)}$	TXD input to bus dominant output delay	RL=60 Ohm, CL=100pF, see Figure 9-1		35		ns
$t_{d(TXD-busrec)}$	TXD input to bus recessive output delay	RL=60 Ohm, CL=100pF, see Figure 9-1		35		ns
$t_{d(busdom-RXD)}$	Bus dominant to RXD output delay	CL=15pF, see Figure 9-2		65		ns
$t_{d(busrec-RXD)}$	Bus recessive to RXD output delay	CL=15pF, see Figure 9-2		55		ns
$t_{d(TXDL-RXDL)}$	TXD low to RXD low loop delay	$T_{bit(TXD)}$ = 200 ns, see Figure 9-3			255	ns
$t_{d(TXDH-RXDH)}$	TXD high to RXD high loop delay	$T_{bit(TXD)}$ = 200 ns, see Figure 9-3			255	ns
$t_{bit(bus)}$	Transmission recessive bit width	$t_{bit(TXD)}$ = 500 ns	435		530	ns
		$t_{bit(TXD)}$ = 500 ns	155		210	ns
$t_{bit(RXD)}$	Bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns	400		550	ns
		$t_{bit(TXD)}$ = 500 ns	120		220	ns
Δt_{rec}	Receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	-65		40	ns
		$t_{bit(TXD)}$ = 500 ns	-45		15	ns
$t_{wake(busdom)}$	Bus dominant wake-up time	First pulse (after first recessive) for wake-up on bus pins CANH/CANL; CAN offline mode	0.5		1.8	µs
		Second pulse for wake-up on bus pins CANH/CANL	0.5		1.8	µs
$t_{wake(busrec)}$	Bus recessive wake-up time	First pulse for wake-up on bus pins CANH/CANL;CAN offline mode	0.5		1.8	µs
		Second pulse (after first dominant) for wake-up on bus pins CANH/CANL	0.5		1.8	µs
$t_{to(wake)bus}$	Bus wake-up timeout	Between first and second dominant pulses; CAN offline mode	0.8		10	µs
$t_{to(dom)TXD}$	TXD dominant timeout	CAN active; VTXD = 0V	2		8	ms
$t_{to(silence)}$	Bus silence timeout	Start recessive time measurement in all CAN modes	0.95		1.17	s
$t_{d(busact-bias)}$	Propagation delay: from bus active to bias				200	µs
$t_{startup(CAN)}$	CAN start up time	CTS = 1; when switching to CAN active mode			220	µs
CAN Partial networking						
$n_{bit(idle)}$	Number of idle bits	Before receiving next SOF, CFDC=1	6		10	
$t_{fltr(bit)dom}$	Dominant bit filtering time	Arbitration data rate is less than 500 kbit/s, data bit-rate ≤ 2Mbps, CFDC=1,FD_FL=0	5		17.5	%
		Arbitration data rate is less than 500 kbit/s, data rate ≤ 5Mbps,CFDC=1,FD_FL=1	2.5		8.75	%
RXD interrupt or wake-up timing (valid only in CAN offline mode)						
$t_{d(event)}$	Event capture delay time	CAN offline mode	0.9		1.1	ms
$t_{rxd(stuck)}$	Stuck detecting filtering time			20		µs
t_{blank}	blanking time	Switch to CAN active/listen-only mode from CAN offline mode			25	µs

Dynamic Characteristics (continued)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT} Power supply						
$t_{BAT(OV)}$	BAT over-voltage detection filtering time		10	20	30	µs
Power supply: V1						
$t_{startup}$	Startup time	from V_{BAT} exceeding power-on detection threshold to V_{V1} exceeds 90% undervoltage threshold; C_{V1} = 4.7 µF		1	4.7	ms
$t_{d(uvd)}$	Under-voltage detection delay time	5V version, V_{V1} undervoltage detection delay	6		54	µs
		3.3V version, V_{V1} undervoltage detection delay	100		300	µs
		V1 undervoltage blanking time		1200		µs
$t_{d(uvd-RSTNL)}$	Delay time from undervoltage to RSTN low	V1 UVLO			63	µs
Power supply: V2						
$t_{d(uvd)}$	Undervoltage detection delay time	V_{V2} undervoltage detection delay time	6		32	µs
		V_{V2} undervoltage blanking time	1.5	2	2.5	ms
$t_{d(ovd)}$	Over-voltage detection delay time	V_{V2} overvoltage detection delay time	100		300	µs
Watchdog						
$t_{trig(wd)1}$	watchdog trigger time 1	Normal mode; watchdog window mode only	0.45xNWP		0.55xNWP	ms
$t_{trig(wd)2}$	watchdog trigger time 2	Normal/standby mode	0.9xNWP		1.1xNWP	ms
$t_{d(SCSNH-RSTNL)}$	Delay time from SCSN high to RSTN low	watchdog window mode, triggered before $t_{trig(wd)1}$			0.2	ms
RSTN						
$t_{w(rst)}$	Reset pulse width	Output pulse width: RLC = 00	20		25	ms
		Output pulse width: RLC = 01	10		12.5	ms
		Output pulse width: RLC = 10	3.6		5	ms
		Output pulse width: RLC = 11	1		1.5	ms
		Input pulse width:	18			µs
$t_{stuck(rst)}$	Pin RSTN stuck filtering time			100		µs
WAKE						
t_{wake}	Wake-up time		50			µs
LIMP						
$t_{d(limp)}$	Lime-home delay time		117		145	ms
$t_{stuck(limp)}$	Pin LIMP stuck filtering time			21		µs
Mode switching timing						
$t_{d(act)norm}$	Delay time to normal mode	MC=111, SBC switches to normal to CAN active			320	µs
NV memory						
$t_{d(MTPNV)}$	MTP NV memory delay time		0.9		1.1	s

Dynamic Characteristics (continued)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
$t_{cy(clk)}$	SCK clock period	Normal/standby mode	250			ns
$t_{SPILEAD}$	SCSN-fall-to-SCK-rise time	Normal/standby mode	50			ns
t_{SPILAG}	SCK-fall-to-SCSN-rise time	Normal/standby mode	50			ns
$t_{clk(H)}$	SCK pulse width_High	Normal/standby mode	100			ns
$t_{clk(L)}$	SCK pulse width_Low	Normal/standby mode	100			ns
$t_{su(D)}$	SDI input setup time	Normal/standby mode	50			ns
$t_{h(D)}$	SDI input hold time	Normal/standby mode	50			ns
$t_{v(Q)}$	Output data propagation delay	Pin SDO, Cl=20pF, normal/standby mode			50	ns
		Pin SDO, Cl=20pF, sleep mode			200	ns
$t_{d(SDI-SDO)}$	SDI to SDO propagation delay	SPI address and read-only bits, Cl=20pF			50	ns
$t_{WH(S)}$	SCSN pulse width_High	Pin SCSN, normal/standby mode	250			ns
$t_{d(SCKL-SCSNL)}$	SCK fall to SCSN fall delay time		50			ns

8.7. Typical Characteristics

Over recommended operating conditions, unless otherwise noted.

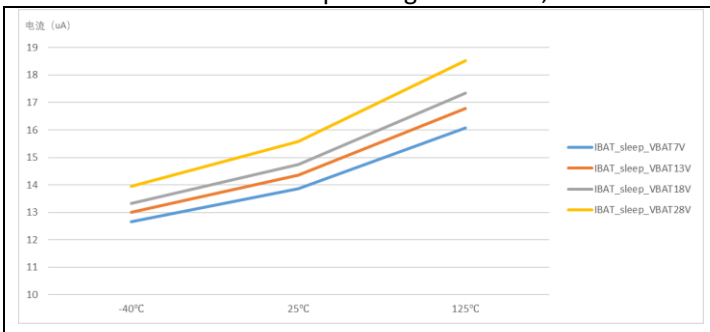


Figure 8-1. Supply current @ listen-only mode

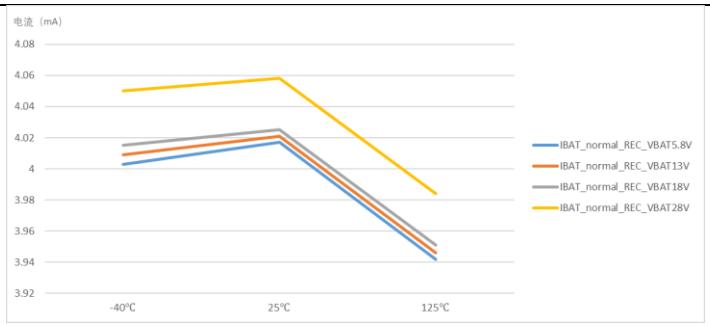


Figure 8-2. Supply current @ recessive state

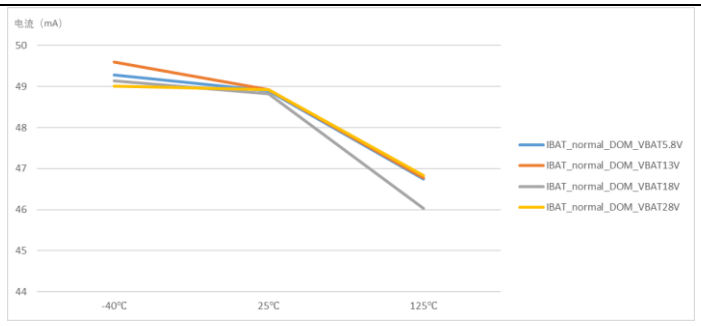


Figure 8-3. Supply current @ dominant state, R_L = 60Ω

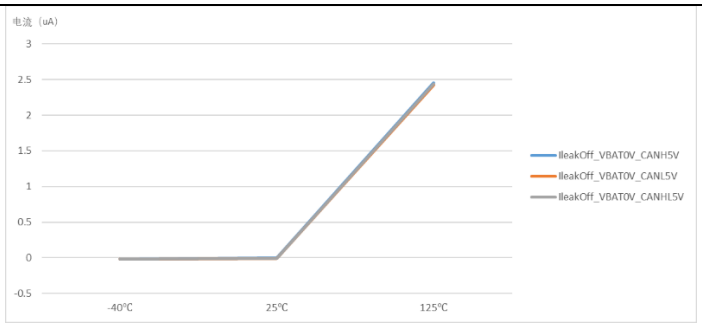


Figure 8-4. Bus Fault current

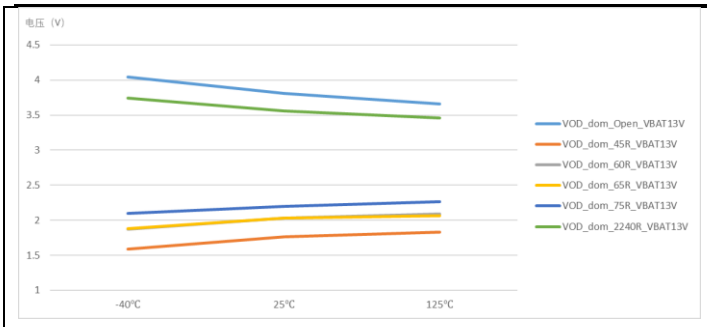


Figure 8-5. Bus output differential voltage (dominant) @ different load

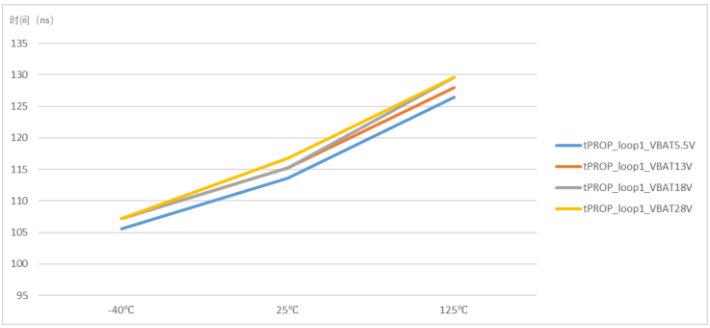


Figure 8-6. Loop delay from dominant to recessive

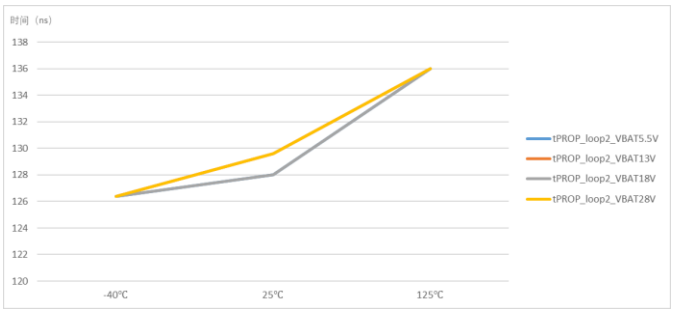


Figure 8-7. Loop delay from recessive to dominant

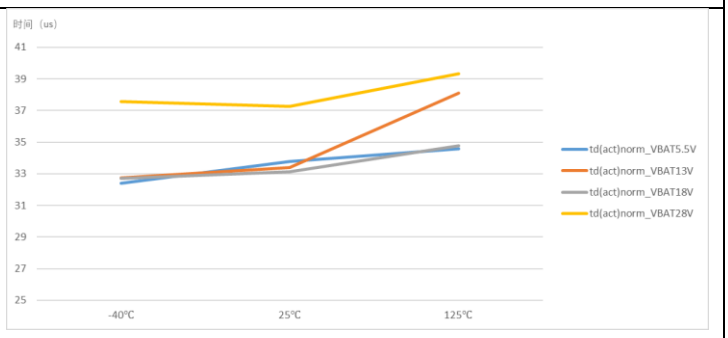


Figure 8-8. Mode switching time

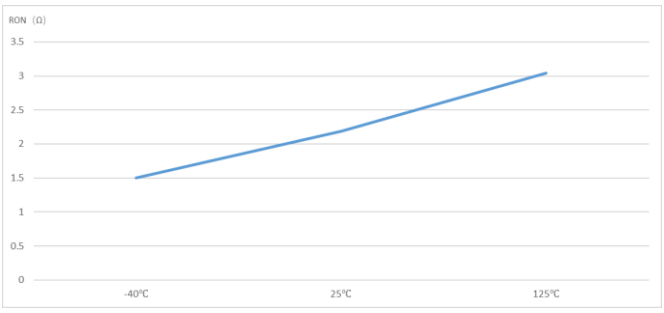


Figure 8-9. V1 Ron resistance vs. temperature

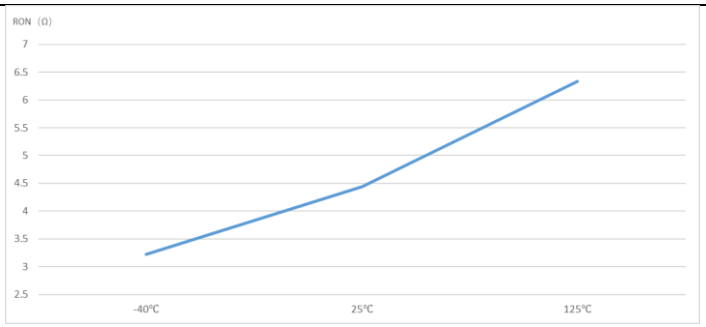


Figure 8-10. V2 Ron resistance vs. temperature

9. Parameter Measurement Information

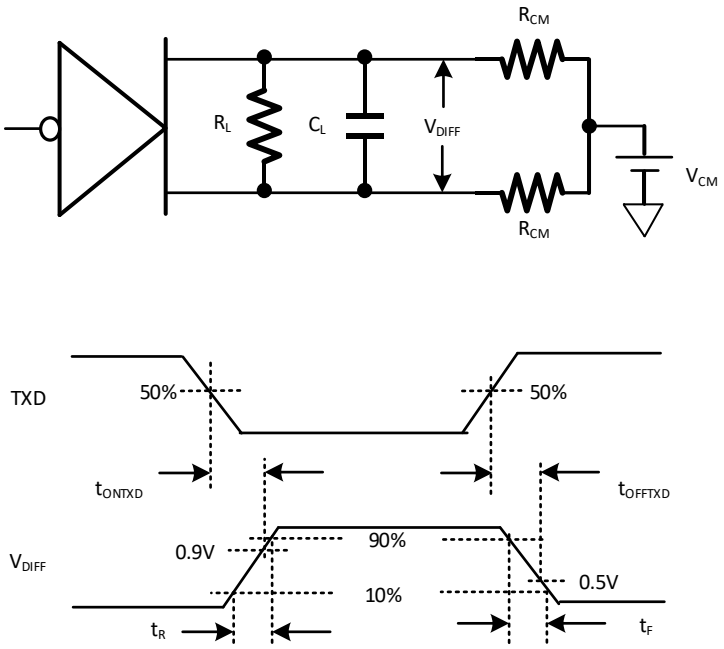


Figure 9-1. Transmitter test circuit and timing diagram

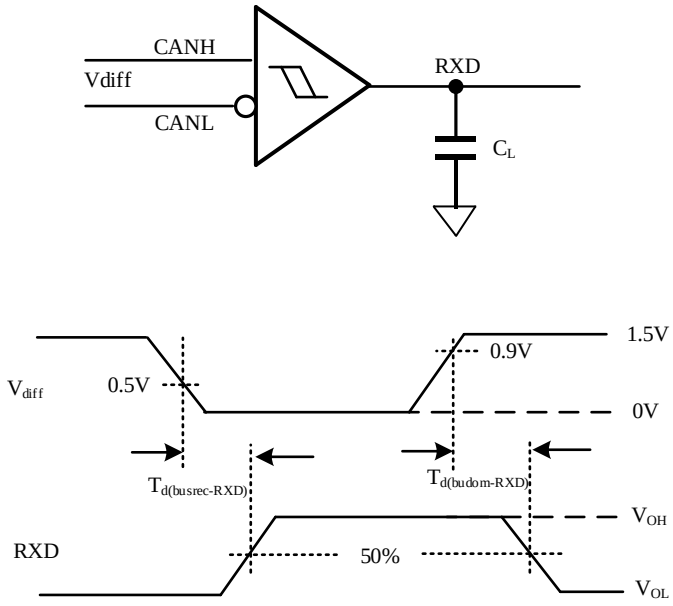


Figure 9-2. Receiver test circuit and timing diagram

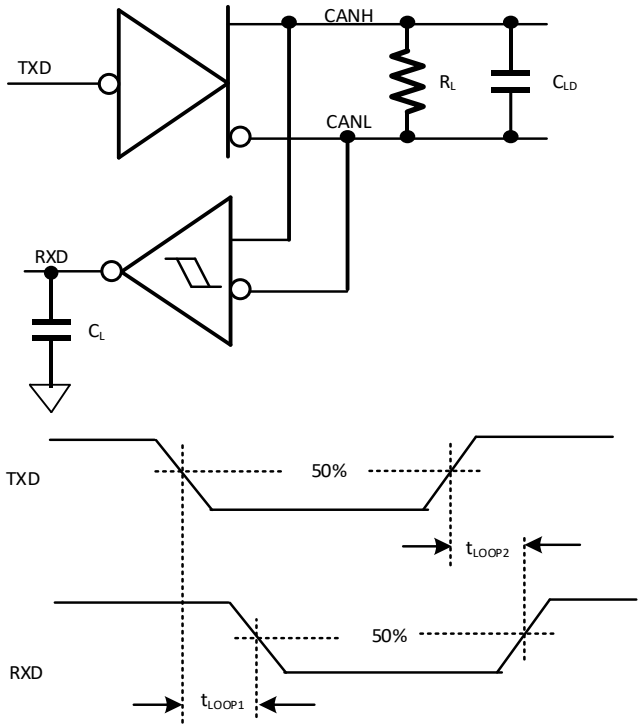


Figure 9-3. TXD to RXD loop delay

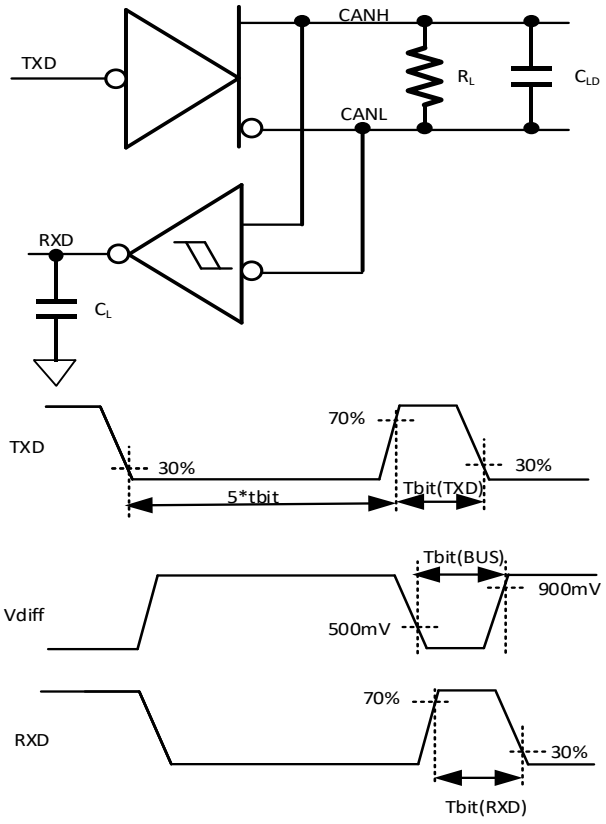


Figure 9-4. FD timing diagram

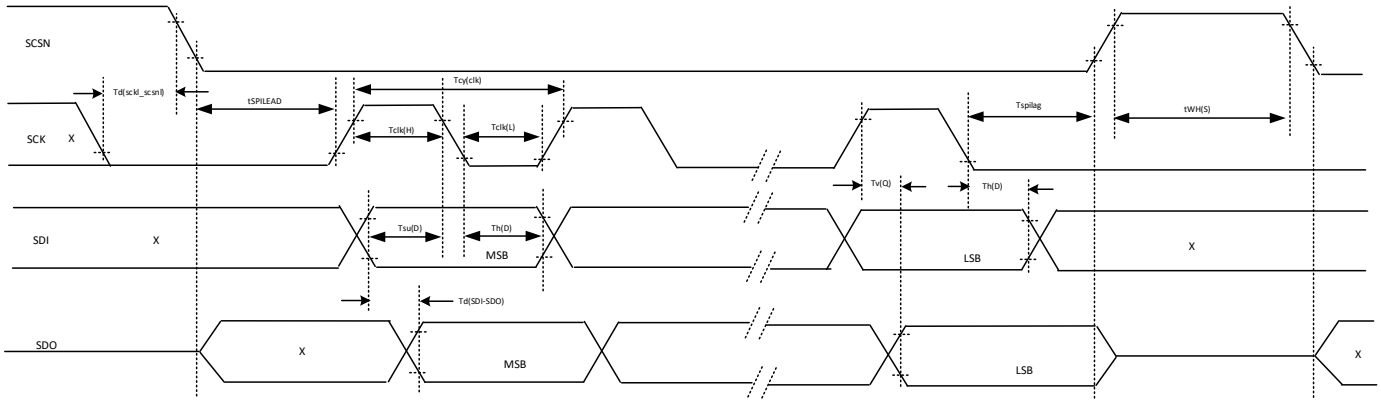


Figure 9-5. SPI timing diagram

10. Detailed Description

10.1. Overview

The CA-IF1169 is a system basis chip (SBC) with integrated high-speed CAN transceiver and dual LDOs. The CAN transceiver complies with ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 standards for high-speed CAN (Controller Area Network) physical layer specifications, supporting up to 5 Mbit/s CAN FD communication. These devices feature up to ±42V extended fault protection on the data transmission lines in all operation modes. The dual internal LDOs provide 3.3V or 5.0V @250mA (V1) and 5.0V @100mA (V2) outputs, respectively. The output current of LDO V1 can be extended via an external PNP transistor, enabling it to power the system microcontroller or other on-board loads; LDO V2 can be used to support the CAN transceiver and other on-board loads supply.

The CA-IF1169 features low-power standby and sleep modes, and supports selective wake-up. The selective wake-up support enables system to implement partial networking as defined by ISO 11898-2:2016 and operate with a reduced number of nodes in an active state while the remaining nodes are in a low-power sleep mode. The CA-IF1169 devices design follows a comprehensive functional safety development process to support customer achieving ASIL-B certification for their end products.

The functional block diagram of CA-IF1169 is shown in Figure 10-1. The CAN FD transceivers is fault protected up to ±42V, and devices communicate with external CAN controllers through a SPI interface and internal controller to configure the registers and control the CAN FD transceiver operation mode. Also, internal 3.3V or 5.0V LDO output option simplifies the interface with 3.3V to 5.0V CAN controllers.

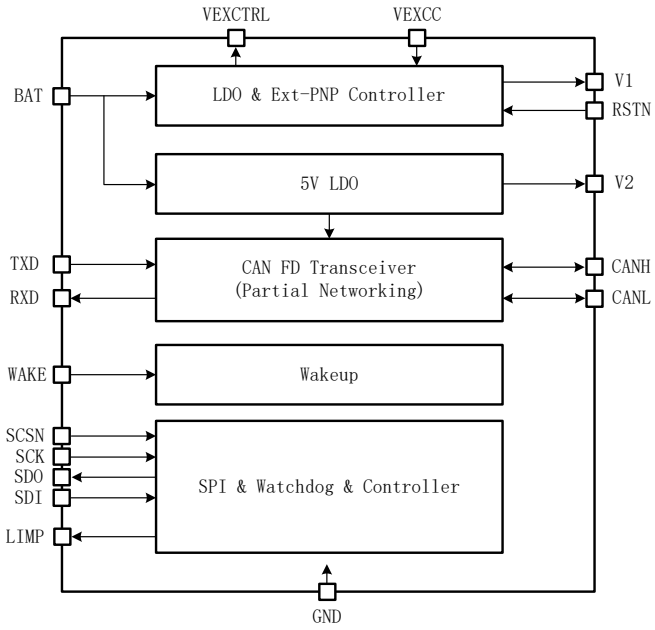
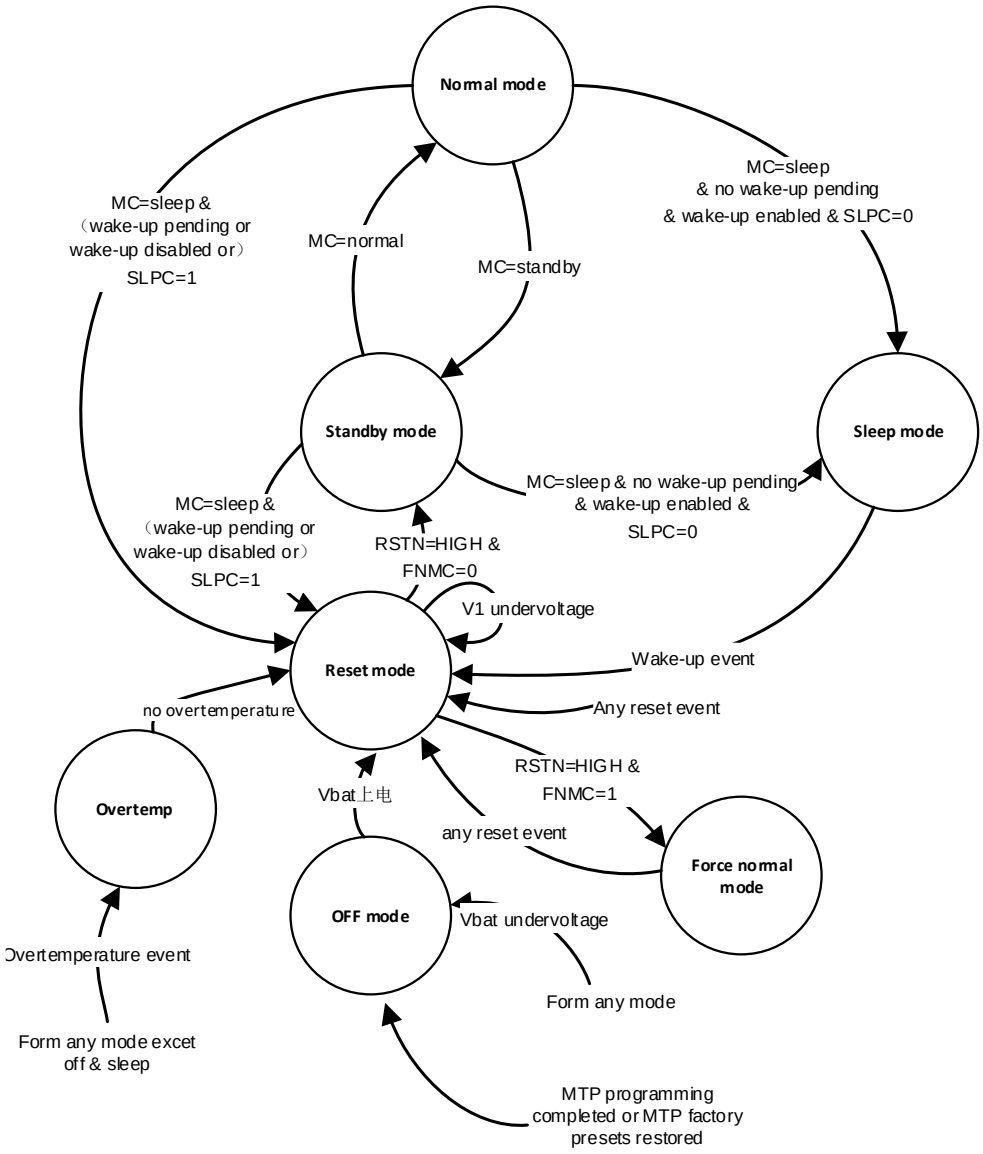


Figure 10-1. Functional block diagram

10.2. SBC Operating Modes and Control

The CA-IF1169 internal system controller manages the SBC register configurations and internal circuit operation, allowing the external microcontroller to collect and manage status information. The SBC state machine supports seven operating modes: normal mode, standby mode, sleep mode, overtemperature protection mode, off mode, reset mode, and forced normal mode, see Figure 10-2. System state diagram.



Note: MC means mode control bits.

Figure 10-2. System state diagram

10.2.1. Normal Mode

Normal mode is an active operation mode. The CAN FD transceiver is fully operational. LDO V1 is enabled to provide supply for microcontroller. Watchdog operates in window or timeout mode depending on the SPI register settings. Select normal mode operation from standby or sleep mode by setting MC = 111 (mode control register, 01h) through SPI command.

10.2.2. Standby Mode

Standby mode is a low-power SBC operating mode. Both CAN transmitter and receiver are disabled and no communication with the CAN bus in standby mode. The SPI and LDO V1 remain active. The watchdog and LDO V2/VEXT status are determined by SPI register setting.

In standby mode, the remote wake-up is enabled (CWE = 1, see Table 10-36), the bus pins are biased to GND when the bus is

inactive and the bus bias changes from ground to about 2.5 V while there is activity on the CAN bus and listening for a valid wake-up request. Once a wake-up request is detected, RXD will be placed at low-level that can be used as an interrupt for the microcontroller. The wakeup sources can be a standard wake-up pattern(WUP) or a selective wake-up frame (CPNC = PNCOK = 1, see Table 10-19. CAN transceiver control register (address = 0x20)

Table 10-19. CAN transceiver control register (address = 0x20)).

The CA-IF1169 switches to standby mode in case one of below conditions asserted,

- In off mode, the battery voltage increases and exceeds the BAT power-on detection threshold $V_{th(det)pon}$;
- Under overtemperature protection condition, the device temperature drops below thermal shutdown release threshold $t_{th(rel)otp}$;
- A wake-up request or an interrupt event is detected in sleep mode;
- During normal operation or in sleep mode, the CA-IF1169 receives MC=100 SPI command;

10.2.3. Sleep Mode and Protection

Sleep mode is the lowest-power operating mode. The difference between sleep and standby modes is that LDO V1 is off and temperature protection is disabled in sleep mode, while other features remain similar to standby mode. In sleep mode, the CAN bus, SPI interface and WAKE pin are continuously monitored for a valid wakeup signal, so that transceiver is able to be woken up by a message on the CAN bus, SPI interface or local wakeup event through WAKE pin. Whenever a local or remote wake-up, or interrupt event (except SPIF) occurs, the transceiver will enter standby mode automatically. LDO V2/VEXT status are determined by SPI register setting. The SPI is disabled after device enters sleep mode. Autonomous bus biasing is active. The watchdog status is determined by WMC bit setting and SBC operation mode, see Table 10-5 for more details.

During normal operation or standby mode, the CA-IF1169 switches to sleep mode through MC = 001 SPI command in case of there are no pending wake-up events and at least one wake-up source is enabled. If a wake up request is still pending or the SPI command disabled all of wake-up sources, the device will switch to reset mode and set RSS = 10100 to avoid system deadlock.

When the device is in sleep mode, the wake-up event capture function is critical because SBC can only exit sleep mode to respond a captured wake-up event. To avoid potential system deadlocks, SBC needs to distinguish the regular events and diagnostic events. Wake up events (remote or local) are recognized as regular events; Diagnostic events indicate fault or error conditions or status change. Before SBC goes to sleep mode, at least one regular wake-up event must be enabled. Any attempt to enter sleep mode will trigger a system reset if all regular wake-up events are disabled.

Another condition that must be met before SBC switches to sleep mode is that all event status bits must be cleared. If an event is in a pending state when SBC receives the sleep mode command (MC=001), it will switch to reset mode immediately. This condition applies to both routine events and diagnostic events.

As the LDO V1 is off in sleep mode, SBC can only exit sleep mode through wake-up events. For system operation safety, especially, for the applications where the host power supply can not be off, sleep mode can be permanently disabled by setting the sleep control bit to 1 in the SBC configuration register (SLPC=1, Table 10-3). In this case, writing MC = 001 through SPI command will not cause SBC to enter sleep mode, but will generate a SPI failure event instead.

10.2.4. Off Mode

When the voltage on BAT pin drops below power-off threshold $V_{th(det)poff}$ for longer than $t_{d(uvd)}$, the CA-IF1169 will be placed into off mod regardless of the current device state. Both CAN transmitter and receiver are disabled in off mode, leave the bus pins and RXD in high-impedance. All hardware is shutdown except the battery voltage detection feature. This is the default state when the device is first connected to battery supply. When the battery supply voltage rises above the power-on threshold $V_{th(det)pon}$, the CA-IF1169 starts an initialization procedure. After $t_{startup}$, the device enters reset mode.

10.2.5. Reset Mode

Reset mode is the state when the SBC executes a reset sequence. The RSTN pin is pulled low for a fixed time to ensure

the microcontroller start-up in a controlled manner. In reset mode, the CAN transceiver cannot transmit signals. The LDO V2 operation status is determined by V2C and V2SUC configuration. SPI and watchdog are disabled, while LDO V1 and overtemperature protection remain active.

The CA-IF1169 can transition into reset mode from any other mode after triggering a reset event, as detailed in Table 10-9. After exiting reset mode:

- If RSTN is high, the device enters standby mode;
- If FNMC = 1, the device enters forced normal mode;
- If overtemperature or shutdown conditions are met, the device transitions into overtemperature protection or off mode.

10.2.6. Overtemperature Protection Mode

Overtemperature protection mode prevents damage to the CA-IF1169 from excessive heat. Once the device junction temperature exceeds thermal shutdown threshold $T_{th(act)otp}$ (190°C, typ), the CA-IF1169 will be placed into overtemperature protection mode immediately, turn off the CAN transmitter thus blocking the TXD-to-bus transmission path. Also CAN receiver is disabled and can not detect wakeup events, but a pending wake-up event will still place RXD to low level, and RXD pin will keep low after the overtemperature condition cleared. In overtemperature protection mode, LDO V1, LDO V2/VEXT are switched off.

To prevent data losing due to overheating, the CA-IF1169 issues an alarm signal when the device junction temperature rises above the overtemperature warning threshold $T_{th(warn)otp}$ (140°C, typ). When the threshold $T_{th(warn)otp}$ is reached, the overtemperature alarm status bit OTWS is set and an overtemperature interrupt is triggered (OTW = 1) if OTWE = 1 (overtemperature alarm enable control bit, see
Table 10-34).

The CA-IF1169 exits overtemperature protection mode:

- When the junction temperature drops below the overtemperature release threshold $T_{th(rel)otp}$, the SBC transitions to standby mode via reset mode;
- If V_{BAT} voltage is too low ($V_{BAT} < V_{th(det)poff}$) , the device enters off mode.

10.2.7. Forced Normal Mode

Forced normal mode is used to simplify the SBC testing, prototyping and fault diagnosis. It can also be used for initial microcontroller flashing. In forced normal mode, the watchdog is disabled, and the LDO V1, LDO V2 and the CAN transceiver are activated.

Bit FNMC is factory preset (FNMC = 1), so the CA-IF1169 initially boots up in forced normal mode. This is equivalent to normal mode without the watchdog enabled.

Even in forced normal mode, a reset event will trigger the SBC into reset mode same as normal reset except the CAN transmitter will remain operational unless CAN bus supply (V_{CAN}) under-voltage occurs. When the device exits reset mode, the SBC returns to forced normal mode.

Registers accessible in forced normal mode include the main state machine register, watchdog status register, identification register, MTPNV status register, and registers stored in non-volatile memory. The NV memory area is fully accessible for writing as long as the CA-IF1169 is in forced normal mode.

10.2.8. Software Development Mode

Software development mode is not a dedicated SBC operation mode. This mode is provided just to simplify software design processes. When this mode is enabled, the watchdog starts in autonomous mode (WMC = 001) and remains inactive after a system reset, overriding the default values, see Table 10-6. The watchdog is always off in autonomous mode if software development mode is enabled (SDMC = 1; see Table 10-5).

In software development mode, software can be running without watchdog enabled. However, it is possible to enable or

disable the watchdog for testing and debugging purposes by selecting watchdog window or watchdog timeout mode via bits WMC while the SBC is in standby mode. The window mode is only activated when SBC switches to normal mode. The software development mode is enabled through SDMC bits in non-volatile memory. When the software development mode is activated, the CA-IF1169 SBC can be in any functional operation mode.

Table 10-1 shows the operation status for each functional block in the different operation modes.

Table 10-1. SBC operating status[1]

Functional Block	Operating Mode						
	Off	Forced normal	Standby	Normal	Sleep	Reset	Overtemperature Protection
LDO V1	Off	On	On	On	Off	On	Off
LDO V2	Off	On	Determined by bits V2C	Determined by bits V2C	Determined by bits V2C	Determined by bits V2C	Off
RSTN	Low	High	High	High	Low	Low	Low
SPI interface	Disabled	Limited register access	Active	Active	Disabled	Disabled	Disabled
Watchdog	Disabled	Disabled	Determined by bits WMC	Determined by bits WMC	Determined by bits WMC	Disabled	Disabled
CAN transceiver	Disabled	Active	Offline	Determined by CMC setup: active/offline/listen-only	Offline	Offline	Disabled
RXD output	High (V_1)	CAN bit stream	Low if a remote wake event occurred, otherwise output High(V_1).	CAN bit stream if CMC = 01/10/11, otherwise same as standby and sleep modes.	Low if a remote wake event occurred, otherwise output High (V_1).	Low if a remote wake event occurred, otherwise output High (V_1).	Low if a remote wake event occurred, otherwise output High (V_1).

Notes:
1. Hi-Z = high impedance, High = high-level, Low = low-level;

10.2.9. System Control Register

The external CAN controller can write the mode control register (address = 0x01) via SPI interface to setup system operating modes, see Table 10-2. The main status register(address = 0x03) can be accessed to monitor the overtemperature warning flag and whether the CA-IF1169 SBC has entered normal mode after power-on reset. It also indicates the source of latest events and RSS indicates the source of the most recent reset event, see

Table 10-3. SBC control register (address = 0x74h)

Bit	Symbol	Type	Value	Description
7:6	Reserved	R	-	
5:4	V1RTSUC	R/W		V1 undervoltage detection threshold after reset (defined by V1RTC):
			00	90% of nominal value at start-up (V1RTC = 00)
			01	80% of nominal value at start-up (V1RTC = 01)
			10	70% of nominal value at start-up (V1RTC = 10)
			11	60% of nominal value at start-up (V1RTC = 11)
3	FNMC	R/W	-	Forced normal mode control
			0	Forced normal mode disabled
			1	Forced normal mode enabled
2	SDMC	R/W		Software development mode control:
			0	Software development mode disabled
			1	Software development mode enabled
1	Reserved	R	-	
0	SLPC	R/W		Sleep mode control:
			0	Sleep mode commands accepted
			1	Sleep mode commands ignored

Table 10-4 for more detail. The SBC configuration control register is in non-volatile memory area, allowing designer to define the default SBC operation status at any battery start-up.

Table 10-2. Mode control register (address = 0x01)

Bit	Symbol	Type[1]	Value	Description
7:3	Reserved	R	-	
2:0	MC	R/W		Mode control
			001	Sleep mode
			100	Standby mode
			111	Normal mode

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 10-3. SBC control register (address = 0x74h)

Bit	Symbol	Type	Value	Description
7:6	Reserved	R	-	
5:4	V1RTSUC	R/W		V1 undervoltage detection threshold after reset (defined by V1RTC):
			00	90% of nominal value at start-up (V1RTC = 00)
			01	80% of nominal value at start-up (V1RTC = 01)
			10	70% of nominal value at start-up (V1RTC = 10)
			11	60% of nominal value at start-up (V1RTC = 11)
3	FNMC	R/W	-	Forced normal mode control
			0	Forced normal mode disabled
			1	Forced normal mode enabled
2	SDMC	R/W		Software development mode control:
			0	Software development mode disabled
			1	Software development mode enabled
1	Reserved	R	-	
0	SLPC	R/W		Sleep mode control:
			0	Sleep mode commands accepted
			1	Sleep mode commands ignored

Table 10-4. Main status register (address = 0x03)

Bit	Symbol	Type	Value	Description
7	Reserved	R		
6	OTWS	R		Overtemperature alarm status
			0	Junction temperature < $T_{th(warn)otp}$
			1	Junction temperature ≥ $T_{th(warn)otp}$
5	NMS	R		Normal operation status
			0	Device has entered normal mode after power-up.
			1	Device has powered up but didn't go to normal mode.
4:0	RSS	R	-	reset source status:
			00000	Power on
			00001	remote wake-up in sleep mode
			00100	Wake-up via pin WAKE in sleep mode
			01100	Watchdog timeout in sleep mode(timeout mode)
			01101	Diagnostic wake-up in Sleep mode
			01110	Watchdog triggered too early at window mode
			01111	Watchdog timeout at window mode or timeout mode with WDF = 1
			10000	Invalid watchdog mode control
			10001	RSTN triggered low externally
			10010	Exit over temperature protection mode
			10011	V1 UVLO
			10100	Received an invalid sleep mode command

			10110	Wake-up from sleep mode due to a frame detect error

10.3. Watchdog

10.3.1. Watchdog Operation and Configuration

The CA-IF1169 contains a programmable watchdog to improve system reliability by monitoring the system for software code execution errors. This watchdog features three configurable modes: window mode (available only in SBC normal operation mode), timeout mode and autonomous mode. The windowed watchdog can be triggered and reset the timer within a specific window of time. In timeout mode, the watchdog is active in all modes, and the watchdog can be triggered and reset the timer anytime within its timeout period. In autonomous mode, the watchdog is either disabled or operates in timeout mode, depending on the SBC operation modes. Table 10-5 shows the watchdog operation modes at different SBC operation status and configurations.

The watchdog mode is set through the WMC bit of the watchdog control register, see Table 10-6. The watchdog mode and timeout period can only be changed when the SBC is in standby mode. If the window mode is selected (WMC=100), the watchdog will not switch to timeout mode until the SBC enters normal mode. In normal mode, changing the watchdog mode or timeout period will cause the SBC to enter reset mode and the reset source status bit (RSS) is set to 10000 (see Table 10-4), and may also trigger SPI failure event.

The default watchdog timeout period is 128ms. It is configurable through the NWP bits and support eight timeout periods from 8ms to 4096ms. A watchdog trigger event resets the watchdog timer. Any valid write access to the watchdog control register can be a watchdog trigger event. If the watchdog mode or the watchdog timeout period is changed because of a write access, the new values will be effective immediately.

Table 10-5. Watchdog operation status

Watchdog operation/mode						
FNMC (forced normal mode)		0	0	0	0	1
SDMC (software development mode)		x	x	0	1	x
WMC (watchdog mode control)		100 (window)	010 (timeout)	001 (autonomous)	001 (autonomous)	N/A
SBC operation modes	Normal mode	Window mode	Timeout mode	Timeout mode	Off	Off
	Standby mode (RXD high)	Timeout mode	Timeout mode	Off	Off	Off
	Sleep mode (RXD low)	Timeout mode	Timeout mode	Timeout mode	Off	Off
	Sleep mode	Timeout mode	Timeout mode	Off	Off	Off
	Others	Off	Off	Off	Off	Off

Table 10-6. Watchdog control register (address = 0x00)

Bit	Symbol	Type	Value	Description
7:5	WMC	R/W	-	Watchdog mode control:
			001	Autonomous mode
			010	Timeout mode
			100	Window mode
4	Reserved	R	-	
3:0	NWP	R/W		Watchdog timeout period:
			1000	8ms
			0001	16 ms
			0010	32 ms
			1011	64 ms
			0100	128 ms
			1101	256 ms
			1110	1024 ms
			0111	4096 ms

Watchdog is a valuable safety feature. It is important to configure its operation correctly. The CA-IF1169 SBC provides two functions to prevent incorrect changes to the watchdog parameters:

- WMC and NWP redundant encoding: ensures single-bit errors don't misconfigure the watchdog (at least 2 bits must be changed to reconfigure WMC or NWP). If an invalid code is attempted to write into WMC or NWP (such as, 011 or 1001 respectively), the SPI operation will be ignored and a SPI failure event will be captured (if enabled).
- Reconfiguration protection: prevents improper changes during normal mode.

Two operating modes have significant impact on watchdog operation: forced normal mode and software development mode. These modes are enabled and disabled respectively through the FNMC and SDMC bits in the SBC control registers (see Table 10-3), which are located in the non-volatile memory area. Watchdog is disabled in forced normal mode; However, watchdog can be enabled or disabled for testing and software debugging in software development mode,.

Watchdog status information, forced normal mode status and whether the software development mode is enabled can be obtained from the watchdog status register, see Table 10-7

Table 10-7. Watchdog status register (address = 0x05)

Bit	Symbol	Type	Value	Description
7:4	Reserved	R	-	
3	FNMS	R		Forced normal mode status:
			0	SBC is not in forced normal mode
			1	SBC is in forced normal mode
2	SDMS	R	-	Software development mode status:
			0	SBC is not in software development mode
			1	SBC is in software development mode
1:0	WDS	R		Watchdog status:
			00	Watchdog disabled
			01	Watchdog is in first half of the nominal timeout period
			10	Watchdog is in seconded half of the nominal timeout period
			11	Reserved

10.3.2. Watchdog @ Window Mode

If WMC = 100 and SBC is in normal mode, the watchdog will be placed in window mode. The watchdog can only be triggered during the second half of the watchdog timeout period in window mode. If the watchdog timer exceeds the watchdog timeout period (watchdog timer overflows) or triggers during the first half of the watchdog period (before $t_{trig\,(wd)\,1}$), the CA-IF1169 SBC will perform a system reset. After the system reset, the reset sources, watchdog triggered too early or watchdog overflow, can be read through the reset source bits (RSS) in the main status register (see Table 10-4). If the watchdog is triggered in the second half of the watchdog timeout period (after $t_{trig\,(wd)\,1}$ and before $t_{trig\,(wd)\,2}$), the internal watchdog timer will be cleared and restarts counting.

10.3.3. Watchdog @ Timeout Mode

If WMC = 010 and SBC is in normal mode, standby mode or sleep mode, the watchdog will be placed into timeout mode; If WMC = 100 and SBC is in standby or sleep low-power mode, the watchdog will be placed into timeout mode as well. If the autonomous mode (WMC = 001) is selected and one of the watchdog timeout mode conditions listed in Table 10-8 is met, the watchdog will also be placed in timeout mode.

The watchdog timer can be reset at any time in timeout mode. If the watchdog timer exceeds the watchdog timeout period, a watchdog failure(WDF) event will be captured. If WDF is pending already when watchdog timer overflows, the CA-IF1169 SBC will perform a system reset. In timeout mode, the watchdog can be used to wake-up microcontroller periodically when the SBC is in standby or sleep mode. When SBC is in sleep mode and watchdog timeout mode is selected, WDF setting will generate a wake-up event after the nominal watchdog period (NWP). At this point, RXD is forced to low level and LDO V1 is on. The application software can clear the WDF bit and trigger the watchdog timer before watchdog overflows again.

For the versions of CA-IF1169VFDT and CA-IF1169FDT, the CAN transceiver of the SBC can be split into two parts: the driver (TXD-CAN) and the receiver (CAN-RXD). When the watchdog of the SBC is configured in timeout mode, it is necessary to first normally configure the watchdog period (NWP) to perform periodic dog-feeding operations, and then start the CAN driver. The receiver part works normally. When no dog-feeding operation is performed, the fault event caused by the watchdog overflow requires the driver part of the CAN transceiver to be turned off first, while the receiver part is not affected.

10.3.4. Watchdog @ Autonomous Mode

If WMC = 001, watchdog autonomous mode is selected. In this mode, watchdog will be placed in timeout mode or off as shown in Table 10-8.

Table 10-8. Watchdog status @ autonomous mode

CA-IF1169 SBC operation modes	Watchdog status	
	SDMC = 0	SDMC = 1
Normal mode	Timeout mode	Off
Standby mode; RXD high	Off	Off
Sleep mode	Off	Off
Other modes	Off	Off
Standby mode; RXD low	Timeout mode	Off

When selecting autonomous mode, if SBC is in normal mode or standby mode (RXD is low), the watchdog will be in timeout mode in case of the software development mode has been disabled (SDMC=0), otherwise the watchdog will be turned off.

In autonomous mode, the watchdog will turn off when the SBC is in standby (RXD high) or sleep mode. If a wake-up event is captured, pin RXD is forced to low level to issue an event alarm signal, and the watchdog restarts automatically with timeout mode. If the SBC is in sleep mode when the wake-up event is captured, it will switch to standby mode.

10.4. System Reset

10.4.1. Reset Sources

The CA-IF1169 SBC monitors the LDO V1 voltage and other reset sources continuously. When a system reset occurs, SBC switches to reset mode and generates a low-level pulse on pin RSTN. The CA-IF1169 can detect and identify up to 13 different reset sources.

The following events will assert the CA-IF1169 to enter reset mode.

- During normal operation or under standby mode, the LDO V1 voltage falls below the programmable reset threshold. The V1 reset voltage detection threshold is defined by V1RTC bits, see Table 10-15;
- End of a MTPNV programming cycle from off mode;
- External pull-down on the pin RSTN;
- Watchdog overflow in window mode;
- Watchdog triggered too early in window mode (before $t_{trig(wd)1}$);
- Watchdog timer overflow in timeout mode with WD F= 1 (watchdog failure pending);
- Attempt to change the watchdog control register during normal operation;
- SBC exits off mode;
- Local wake-up or CAN bus remote wake-up in sleep mode;
- Diagnostic wake-up in sleep mode;
- SBC exits overtemperature protection mode;
- An illegal sleep mode command received;
- SBC wake-up from sleep mode due to a frame detection error.

The reset trigger source information can be obtained by reading the main status register (RSS, Table 10-4).

10.4.2. RSTN

Pin RSTN is a bidirectional, open drain, low-side driver with integrated pull-up resistor, as shown in Figure 10-3. This configuration allows the operator or external logic circuit (such as microcontrollers) to initiate a system reset through RSTN input. The input reset pulse width must be at least $t_{w\ (rst)}$ to ensure a correct detection of external reset events.

Pin RSTN also generates reset output. Once a reset resource assert a system reset, pin RSTN will remain asserted at least $t_{w(rst)}$. The duration of the output reset pulse $t_{w(rst)}$ is dependent on the reset sources and RLC configuration in the startup control register, see Table 10-9. The CA-IF1169 SBC can recognize cold-start and hot-start reset sources. If the reset event occurs simultaneously with LDO V1 undervoltage event (power on reset, sleep mode reset, over temperature reset, V1 undervoltage before entering or during reset mode), the SBC will perform a cold-start. The setting of the RLC bit determines the output reset pulse width for cold start.

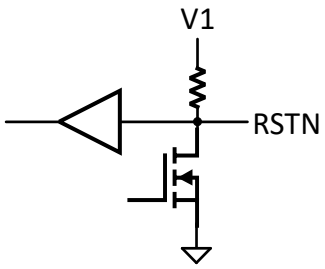


Figure 10-3. Pin RSTN circuit

If any other reset events occur without LDO V1 undervoltage, such as external reset, watchdog timeout, attempting to change watchdog settings during normal operation, an illegal sleep mode command, the SBC will perform a hot-start. The reset output pulse width $t_{w(rst)}$ is determined by the shortest reset length (RLC=11, Table 10-9) for hot-start.

Table 10-9. Startup control register (address = 0x73)

Bit	Symbol	Type	Value	Description
7:6	Reserved	R	-	
5:4	RLC	R/W		RSTN output pulse width:
			00	tw(rst) = 20 ms ~ 25 ms
			01	tw(rst) = 10 ms ~ 12.5 ms
			10	tw(rst) = 3.6 ms ~ 5 ms
			11	tw(rst) = 1 ms ~ 1.5 ms
3	V2SUC	R/W	-	V2 enable control:
			0	V2C/VEXTC bits set to 00 after power-on reset
			1	V2C/VEXTC bits set to 01 after power-on reset
2:0	Reserved	R	-	

10.4.3. Reset Counter

The CA-IF1169 has a reset counter to detect serious failure events. Every time the SBC enters reset mode, the reset counter is incremented by 1 (RCC = RCC+1, see Table 10-10). For normal operation, the application software should reset the counter (RCC=00) periodically to ensure that the regular reset events do not cause reset counter overflow. For example, as the SBC enables LDO V1 powered-up to respond a wake-up event, it always switches to reset mode after exiting sleep mode. As a result, the RCC incremented after each sleep mode. Application software must monitor the RCC and update this value as needed to ensure that multiple sleep mode cycles do not cause reset counter overflow.

If the CA-IF1169 SBC enters reset mode and RCC = 3, the SBC will assume a serious failure has occurred and set the limp-home control bit LHC in the fail-safe register. This forces pin LIMP to low level and clears the reset counter to zero: RCC = 0. The LHC bit can also be configured through SPI interface. If LHC is reset to 0 by application software or a power-on reset when SBC exits off mode, the LIMP pin will be placed floating again.

The application software can preset the counter through SPI interface to define the allowed number of reset events before enabling a limp-home operation. If RCC is initialized to 3, for example, the next reset event will trigger a limp-home function immediately. The default counter setting is RCC = 00 after system power-on reset.

In forced normal mode, both limp-home function and reset counter are disabled, and will not trigger limp-home.

10.5. Fail-safe and Functional Safety Design

The CA-IF1169 follows a comprehensive functional safety development process with integrated analog circuit initiate self-test (ABIST) and critical interface monitoring. The dedicated LIMP output pin for failure indication can be used to guide the system into limp-home. The high-speed CAN transceiver features overvoltage fault protection, over-current protection, under-voltage lockout during all modes of operation. Also, the local and remote bus failures detection can prevent device damage or CAN bus stuck. The device status indicator flags allow the microcontroller to determine the status of the device and the system. This benefits the troubleshooting in a CAN bus system and improves equipment operating efficiencies.

10.5.1. LIMP Output

The dedicated limp-home pin (LIMP) is used to enable limp-home mode when a serious ECU failure occurred. Figure 10-4 shows the LIMP external connections, it's an active-low, open drain output. The CA-IF1169 SBC detects SBC overheating events, watchdog service loss, pin RSTN or V1 short circuit, and user initiated or external reset events etc. failure conditions and configure the LIMP output status. Pin LIMP can also be forced to low level by setting the LHC bit in the fail-safe control register, see Table 10-10.

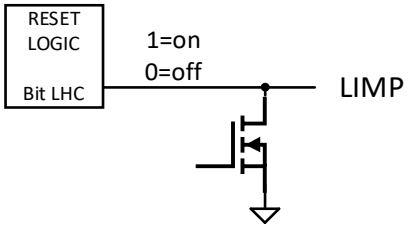


Figure 10-4. LIMP pin connection

When the reset counter overflow (RCC = 3), the CA-IF1169 SBC treats this as a serious failure and sets the limp-home control bit (LHC = 1), forces pin LIMP low. In addition to the reset counter (RCC) overflow, the following events can also cause LHC to set and trigger limp-home immediately:

- The duration of overheating exceeds $t_{d\ (limp)}$;
- SBC remains in reset mode for more than $t_{d\ (limp)}$ (e.g. due to RSTN pin clamped or LDO V1 output voltage remains undervoltage continuously).

In forced normal mode, both limp-home function and reset counter are disabled and will not trigger limp-home mode, see Figure 10-5. Limp-home state diagram for more details.

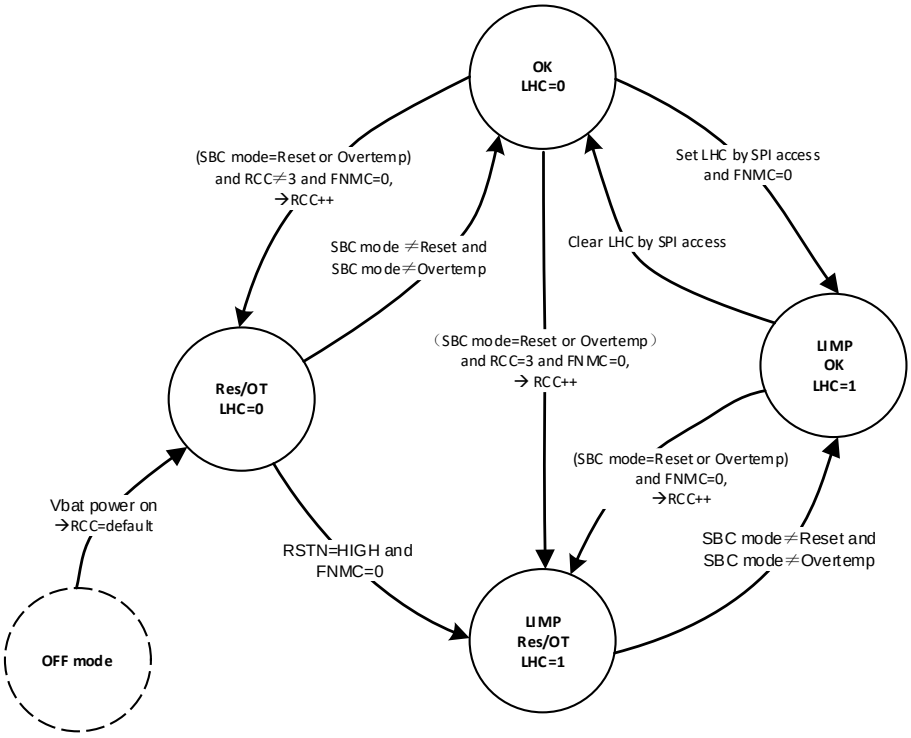


Figure 10-5. Limp-home state diagram

Table 10-10 shows the device fail-safe register, which includes reset counter and limp-home control conditions.

Table 10-10. Fail-safe register (address = 0x02)

Bit	Symbol	Type	Value	Description
7:3	Reserved	R	-	
2	LHC	R/W	-	Pin LIMP status control:
			0	Pin LIMP floating
			1	Pin LIMP is forced low
1:0	RCC	R/W		Reset counter control:
			0	If FNMC = 0, the reset counter is incremented by 1 each time the SBC enters reset mode; RCC overflows from 11 to 00; power-on default value is 00.

10.5.2. Transmitter-Dominant Timeout

The CA-IF1169 devices feature a transmitter-dominant timeout ($t_{o(dom)TXD}$) detection that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus to a recessive state. After a dominant timeout fault, the transmitter is re-enabled and dominant timeout timer is reset when receiving a rising edge at TXD input. The transmitter-dominant timeout limits the minimum possible data rate of CA-IF1169 CAN transceiver to 4.4kbps.

A CAN failure interrupt is generated (CF = 1), if CFE = 1; In addition, the status of the transmitter dominant timeout can be read (CFS bit) from the transceiver status register and CTS bit is set to 0.

10.5.3. Overvoltage Fault Protection

The CA-IF1169 devices has an internal ±42V overvoltage protection circuit on the transmitter output and receiver input to protect the devices from accidental shorts between a local power supply and the data lines of the transceivers. This level of

protection is present whether the transceiver is powered or un-powered. Also, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly.

10.5.4. Current-Limit

The CA-IF1169 protects the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. Also, the device has transmitter dominant timeout detection which prevents permanently having the higher short circuit current of dominant state in case of a system fault.

10.5.5. Floating Terminals

The CA-IF1169 devices have internal pull-up or pull-down on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to LDO V1 to force a recessive input level if the terminal floats.

10.5.6. Undervoltage Lockout

The CA-IF1169 has undervoltage detection on BAT supply terminal, CAN transceiver supply voltage and the internal regulator V1 (LDO V1) output that place the device into low-power mode or protected mode once an undervoltage event occurred. As the battery provides supply for internal circuit and regulators, the device must be protected against negative supply voltages. See Figure 11-1 typical application circuit, an external series diode is used to prevent reverse currents from flowing into the device if the battery or ground connection is lost.

When the voltage on BAT pin drops below power-off threshold $V_{th(det)poff}$ for longer than $t_{d(uvd)}$, the device switches to off mode. Battery supply losing at pin BAT will not affect CAN bus communication between other nodes or external microcontroller operation because no reverse currents flow from the bus. Once V_{BAT} under voltage condition is cleared and the battery supply returned to valid level, above the power-on threshold $V_{th(det)pon}$, the CA-IF1169 SBC starts an initialization procedure, then switches to reset mode after $t_{startup}$. Power-on event status bit PO in the system event status register (
Table 10-31) is set to 1 to indicate the SBC has powered up and exited off mode.

The LDO V1 undervoltage threshold is determined by V1RTC bits in the regulator control register (Table 10-15) for 5V output parts or fixed at 90% of nominal voltage for 3.3V output parts. The default value of LDO V1 power-on reset threshold is defined in the SBC configuration control register(V1RTSUC, Table 10-3). A system reset is generated if the voltage on LDO V1 output drops below the selected undervoltage threshold.

When CMC = 01 and CAN transceiver's supply voltage drops below $V_{UVD(CAN)}$, a CAN failure interrupt will be generated (CF = 1) if CAN failure detection is enabled (CFE = 1) and the supply voltage status bit VCS is set.

10.5.7. Functional Safety Design

The CA-IF1169 device design complies with functional safety development requirements. It features power supply monitoring, critical interface stuck monitoring, and power on self-test (ABIST). See Table 10-11 to Table 10-14 for more details. These devices comply with ISO 26262 ASIL-B standard, also support customer to achieve ASIL-B certification for end products.

Table 10-11. Power supply status register (address = 0x1D)

Bit	Symbol	Type	Value	Description
7	Reserved	R	-	
6	VBAT_OVS	R		BAT overvoltage status:
			0	Lower than threshold
			1	Higher than threshold
5	V2OCS	R		V2 output overcurrent status:

			0	Lower than threshold
			1	Higher than threshold
4	V1OCS	R		V1 output overcurrent status:
			0	Lower than threshold
			1	Higher than threshold
3	V1OVS	R		V1 output overvoltage status:
			0	Lower than threshold
			1	Higher than threshold
2	RSTN_STUCK1_S	R		RSTN stuck status:
			0	No stuck
			1	RSTN stuck
1	LIMP_STUCK_S	R		LIMP stuck status:
			0	No stuck
			1	LIMP stuck
0	RXD_STUCK_S	R		RXD stuck status:
			0	No stuck
			1	RXD stuck

Table 10-12. Power supply monitoring enable control register (address = 0x4D)

Bit	Symbol	Type	Value	Description
7	Reserved	R/W	-	
6	VBAT_OVE	R/W		BAT overvoltage test enable control:
			0	Disable
			1	Enable
5	V2OCE	R/W		V2 output overcurrent test enable control:
			0	Disable
			1	Enable
4	V1OCE	R/W		V1 output overcurrent test enable control:
			0	Disable
			1	Enable
3	V1OVE	R/W		V1 output overvoltage test enable control:
			0	Disable
			1	Enable
2	RSTN_STUCK1_EN	R/W		RSTN stuck test enable control:
			0	Disable
			1	Enable
1	LIMP_STUCK_EN	R/W		LIMP stuck test enable control:
			0	Disable
			1	Enable
0	RXD_STUCK_EN	R/W		RXD stuck test enable control:
			0	Disable
			1	Enable

Table 10-13. Power supply monitoring event register (address = 0x65)

Bit	Symbol	Type	Value	Description
7	Reserved	R	-	
6	VBAT_OV	R/W		BAT overvoltage test:
			0	Lower than threshold
			1	Higher than threshold
5	V2OC	R/W		V2 output overcurrent test:
			0	Lower than threshold

			1	Higher than threshold
4	V1OC	R/W		V1 output overcurrent test:
			0	Lower than threshold
			1	Higher than threshold
3	V1OV	R/W		V1 output overvoltage test:
			0	Lower than threshold
			1	Above the threshold
2	RSTN_STUCK1	R/W		RSTN stuck test:
			0	No stuck
			1	RSTN stuck
1	LIMP_STUCK	R/W		LIMP stuck test
			0	No stuck
			1	LIMP stuck
0	RXD_STUCK	R/W		RXD stuck test:
			0	No stuck
			1	RXD stuck

Table 10-14. Power-on self-detection register (address = 0x66)

Bit	Symbol	Type	Value	Description
7:4	Reserved	R	-	
3	V1_UVRST_ABIST	R/W		V1 undervoltage self-test during reset
			0	Pass self-test
			1	Doesn't pass self-test
2	V1_UV_ABIST	R/W		V1 undervoltage detection circuit:
			0	Pass self-test
			1	Doesn't pass self-test
1	V2_UV_ABIST	R/W		V2 undervoltage detection circuit
			0	Pass self-test
			1	Doesn't pass self-test
0	V2_OV_ABIST	R/W		V2 overvoltage detection circuit:
			0	Pass self-test
			1	Doesn't pass self-test

10.6. Internal Voltage Regulator

The CA-IF1169 integrates two voltage regulators (LDO V1 and LDO V2). These regulators are supplied from the battery via pin BAT. An external series diode can be connected between the battery and pin BAT to prevent reverse currents from flowing into the device if the battery or ground connection is lost, see Figure 10-6.

10.6.1. LDO V1

LDO V1 provides 3.3V or 5V output voltage option with up to 250mA output current capability, see Table 5-1. Ordering Information and Figure for the typical external connection of LDO V1. If V_{BAT} voltage falls below the undervoltage detection threshold ($V_{th(det)poff}$), the SBC switches to off mode. For 5V output parts ,the microcontroller supply voltage (LDO V1) remains active until V_{BAT} drops below 2V to ensure the microcontroller memory remains active as long as possible for RAM retention. This feature is not available for 3.3V output parts.

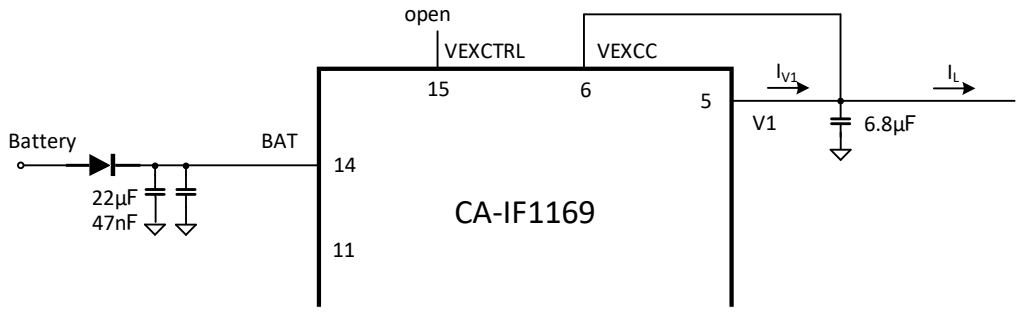


Figure 10-6. LDO V1 external circuit connection

LDO V1 can provide up to 250mA output current @ 5.0V or 3.3V. Its current capacity can be extended via an external PNP transistor, enabling it to power the system microcontroller or other on-board loads, see Figure 10-7. Also, the external PNP transistor is added to share power dissipation with SBC when operating at higher ambient temperature or very high supply current, to avoid device over heating.

In this configuration, power consumption is distributed between SBC (I_{V1}) and PNP transistor (I_{PNP}). When the load current reaches PNP transistor conduction threshold $I_{th(act)PNP}$, the PNP transistor turns on. The power consumption distribution is adjustable based on the PDC bit setting in the regulator control register.

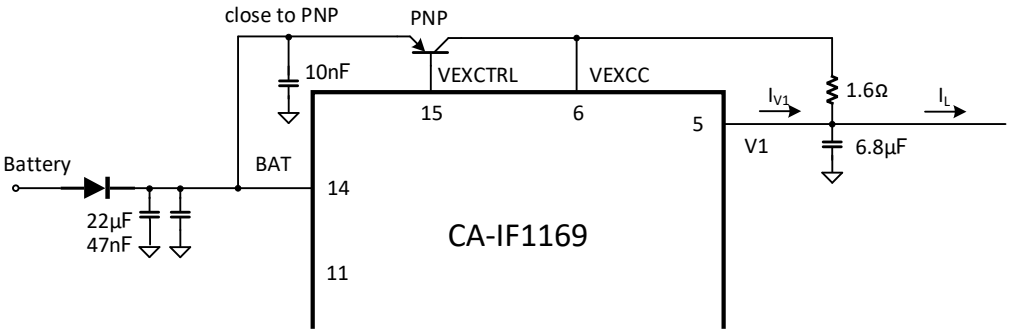


Figure 10-7. LDO V1 circuit connection with external PNP transistor

In order to achieve short-circuit protection, a current-sense resistor is connected in series between pin V1 and VEXCC. This resistor limits the current flow through external PNP transistor. If the voltage drop between pin VEXCC and pin V1 reaches $V_{th(act)Ilim}$ (PNP current-limit threshold voltage), the transistor current will not increase further. Usually, we recommend to select a PNP transistor with current gain factor (β) between 50 and 500.

The CA-IF1169 SBC monitors LDO V1 output voltage. If the regulator output voltage drops below the selected undervoltage threshold, a system reset is triggered. The LDO V1 undervoltage threshold is 60%, 70%, 80%, or 90% of V1 nominal output voltage determined V1RTC in Table 10-15 (5V output), or fixed at 90% of V1 nominal output (3.3V output). The default value of LDO V1 power-on reset threshold is defined in the SBC configuration control register (V1RTSUC, Table 10-3). The configuration of SBC control registers is located in non-volatile memory, allowing users to define the default power-on reset thresholds as needed.

If 60%, 70% or 80% threshold is selected in the regulator control register, the CA-IF1169 can generate an undervoltage warning (V1U event) when LDO V1 output voltage drops below 90% of nominal voltage and V1U event detection is enabled by V1UE = 1, to indicate that the V1 output voltage exceeds the nominal power supply range. The status of LDO V1 output, whether above or below the 90% undervoltage threshold, can be queried through bit V1S in the regulator status register (

Table 10-16).

10.6.2. LDO V2

The LDO V2 provides 5V output voltage with up to 100mA output current to support the internal CAN transceiver and other internal loads supply. As the CAN transceiver consumes a portion of available current from LDO V2, also LDO V2 does not have shorted to batter or negative supply protection, this regulator output is only used for internal circuit supply.

The application software controls LDO V2 on/off status through SPI interface (V2C bit) as shown in Table 10-15, to provide power supply for internal CAN transceiver. LDO V2 supply is not required to support remote wake-up detection via CAN bus. The power-on default value of V2C defined by the V2SUC bit in non-volatile memory, see Table 10-9. The status of LDO V2 can be queried from the regulator status register.

Table 10-15. Regulator control register (address = 10h)

Bit	Symbol	Type	Value	Description
7	Reserved	R	-	
6	PDC	R/W		Power distribution control:
			0	V1 threshold current for activating the external PNP transistor, load current rising; $I_{th(act)PNP}$ higher value; V1 threshold current for deactivating the external PNP transistor, load current falling; $I_{th(deact)PNP}$ higher value.
			1	V1 threshold current for activating the external PNP transistor, load current rising; $I_{th(act)PNP}$ lower value; V1 threshold current for deactivating the external PNP transistor, load current falling; $I_{th(deact)PNP}$ lower value.
5:4	Reserved	R	-	
3:2	V2C	R/W	-	V2 configuration:
			00	V2 turn-off in all operation modes
			01	V2 turn-on in normal mode
			10	V2 turn-on in normal/standby/reset modes
			11	V2 turn-on in normal/standby/sleep/reset modes
1:0	V1RTC[1]	R/W		V1 power-on reset threshold:
			00	90% of V1 nominal value
			01	80% of V1 nominal value
			10	70% of V1 nominal value
			11	60% of V1 nominal value

[1] Only 5V version; the default value is determined by the value of V1RTSUC during the startup phase. The 3.3V version is fixed at 00, and the readback is also fixed at 00.

Table 10-16. Regulator status register (address = 0x1B)

Bit	Symbol	Type	Value	Description
7	Reserved	R	-	
2:1	V2S	R	-	V2 status:
			00	V2 output is normal
			01	V2 output drops below undervoltage threshold
			10	V2 output voltage above overvoltage threshold
			11	V2 is off
1:0	V1S	R		V1 status:
			0	V1 output voltage above 90% undervoltage threshold
			1	V1 output voltage below 90% undervoltage threshold

10.7. High-speed CAN Transceiver

The CA-IF1169 high-speed CAN transceiver support low-power operation mode, as well as wake-up capability over CAN

bus, or via the WAKE pin, SPI command. Also, the features CAN FD-passive by a dedicated implementation of the partial networking protocol.

10.7.1. Receiver

The receiver of CA-IF1169 supports normal bi-directional communication and the bus line wakeup event detection. In normal operation and the transceiver is active, the receiver reads the differential input from the bus line (CANH and CANL) and transfers this data as a single-ended output RXD to the CAN controller. The internal comparator senses the difference voltage V_{DIFF} = (V_{CANH}-V_{CANL}), with respect to an internal threshold of 0.7V. If V_{DIFF} > 0.9V, a logic-low is present on RXD; If V_{DIFF} < 0.5V, a logic-high is present. Table 10-17 shows the receiver truth table.

Table 10-17. Receiver truth table

DEVICE MODE	$V_{ID} = V_{CANH}-V_{CANL}$	BUS STATE	RXD
Active/listen-only CMC=01/10/11	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
	$V_{ID} \leq 0.5V$	Recessive	High
	Open ($V_{ID} \approx 0V$)	Open	High
Standby Sleep	$V_{ID} > 1.15V$	Dominant	Low if a remote wake event occurred, otherwise output High.
	$0.4V < V_{ID} < 1.15V$	Indeterminate	
	$V_{ID} \leq 0.4V$	Recessive	
	Open ($V_{ID} \approx 0V$)	Open	

As mentioned in SBC Operating Modes and Control section, the CA-IF1169 can be configured into low-power operation modes: standby mode and sleep mode. In standby and sleep modes, both CAN transmitter and receiver are disabled and bidirectional CAN communication is not possible, but the CAN bus, SPI interface and WAKE pin are continuously monitored for a valid wakeup signal. RXD is logic high until a valid wakeup signal is received.

10.7.2. Transmitter

In normal operation, if the transceiver is active, the transmitter converts a single-ended input signal (TXD) from the local CAN controller to differential outputs for the bus lines CANH and CANL. The truth table for the transmitter is provided in Table 10-18. The CA-IF1169 protects the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown temperature. In standby and sleep modes, the transmitter is disabled and put the bus in high-impedance with internal weak pull-down to ground.

Table 10-18. Transmitter truth table (when not connected to the bus)

DEVICE MODE	TXD INPUT	TXD LOW TIME	OUTPUT		BUS STATE
			CANH	CANL	
Normal CMC=01 or 10	Low	$< t_{o(dom)TXD}$	High	Low	Dominant
	Low	$> t_{o(dom)TXD}$	$V_1/2$	$V_1/2$	Recessive
	High or Open	X	V_12	$V_1/2$	Recessive
Listen-only CMC = 11	X	X	High-Z	High-Z	Biased to 2.5V
Standby	X	X	High-Z	High-Z	Weakly biased to GND
Sleep	X	X	High-Z	High-Z	Weakly biased to GND

Note: X = Don't care

10.7.3. CAN Operating Modes

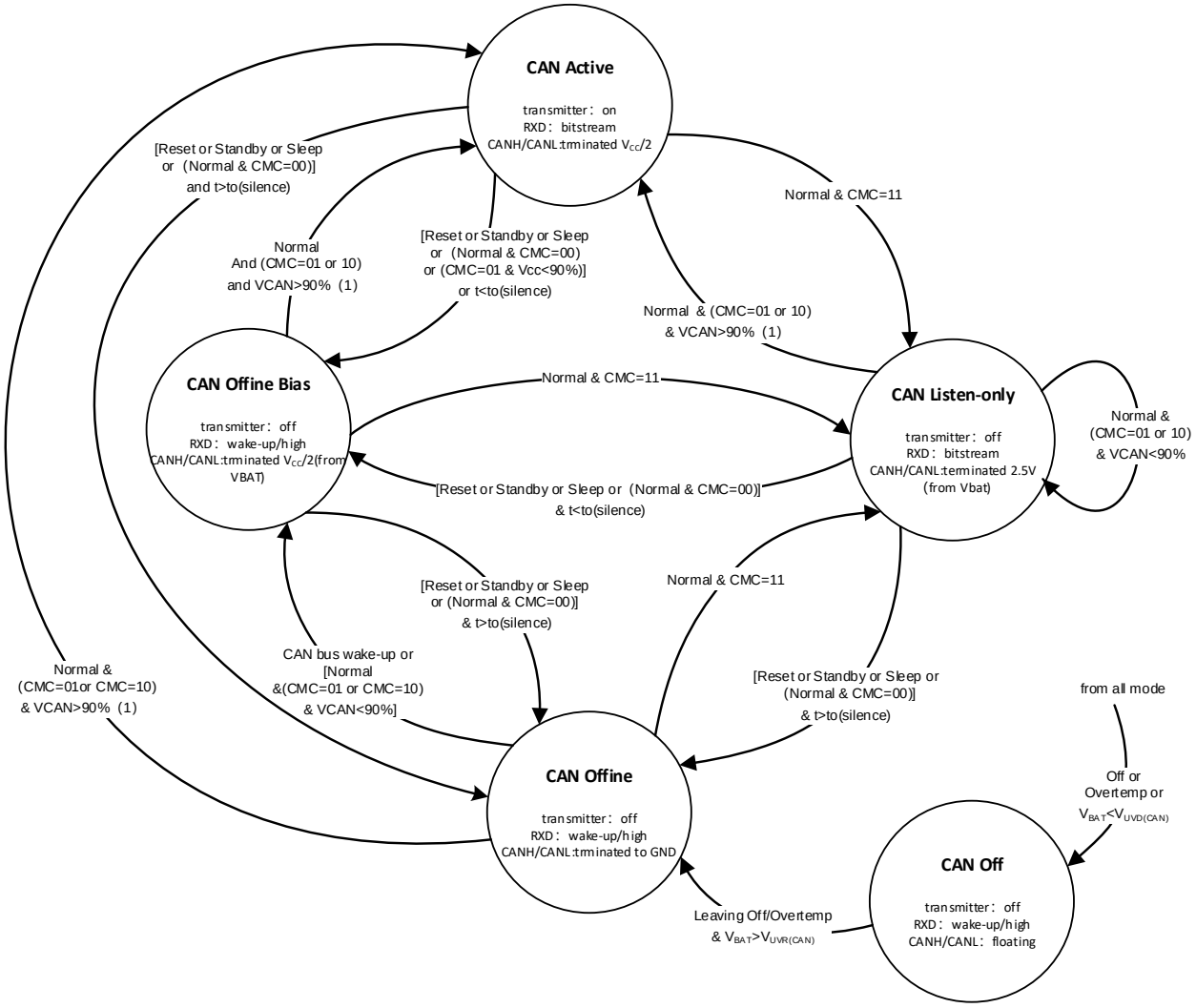
The high-speed CAN transceiver of CA-IF1169 can operate in four modes: active mode, listen-only mode, offline mode, offline bias mode. The transceiver operating mode is determined by the bus status and internal state machine controller, see Figure 10-8. CAN transceiver state diagram. The integrated high-speed CAN transceiver is designed to support up to 1Mbit/s data transmission autonomous biasing and selective wake-up features which compatible with ISO 11898-2:2016 standard definition, also ensure reliable communication in CAN FD networks with up to 5Mbps data rate.

The internal regulators (LDO) provide power supply for CAN transceiver. Autonomous bus biasing is used to minimize RF emissions. The CA-IF1169 biases the CAN bus (CANH/CANL) to 2.5V when the transceiver is in active mode or listen-only mode (CMC=01/10/11); If there is activity on the bus, or if other nodes are communicating, the CAN bus will stay biased to 2.5V (CAN offline bias mode); If there is no activity on the bus for $t > t_{to(silence)}$, the CAN bus will be biased to ground (CAN offline mode). Autonomous biasing ensures that the CAN bus is correctly biased to avoid blocking normal communication between other CAN nodes. The autonomous CAN bias voltage is derived from battery supply directly.

CAN Active Mode

In active mode, the CAN transceiver supports bidirectional bus communication and CAN bus is biased to $V_1/2$ @ recessive state, the CAN bias voltage is derived from LDO V2 supply. In normal operation, if CMC = 01 or 10, the CAN transceiver enters active mode. The LDO V1 UVLO detection is enabled when CMC = 01 and put CAN transceiver into offline/offline bias mode once the V_1 supply voltage drops below UVLO threshold $V_{UVD(CAN)}$; The LDO V1 UVLO detection is disabled when CMC = 10, the CAN transceiver will remain active until the a system reset is generated because of LDO V1 voltage drops below its reset threshold selected by V1RTC configuration, then the transceiver enters offline/offline bias mode.

In normal operation (MC = 111), select CAN transceiver active mode by setting CMC = 10 and V1 voltage is above power-on reset threshold or CMC = 01 and V2 voltage > $V_{UVD(CAN)}$. If the TXD remains in the dominant state (low level), CAN transceiver will switch to listen-only or remain listen-only mode until TXD goes to high-level. This allows other nodes to communicate to prevent bus lockup caused by controller error or by a fault on the TXD input. Reading the CAN transceiver status bit (CTS, see Table 10-20), CAN controller can determine whether the CAN transceiver is ready for data transmission.



Note that: CAN transceiver can not enter active mode when TXD is pulled to GND.

Figure 10-8. CAN transceiver state diagram

CAN Listen-only Mode

Select CAN listen-only mode from normal operation by setting CMC = 11 through SPI interface. In listen-only mode, CAN transmitter is disabled and receiver keeps normal operation, CAN bus is biased at 2.5V if bus active. Also, CAN transceiver will stay at listen-only mode when the TXD remains low-level state, or LDO V1 output voltage is lower than 90% of V1 nominal value when CMC = 01 or 10.

CAN Offline Mode/Offline Bias Mod

The only difference between CAN offline bias mode and CAN offline mode is that CAN bus is biased at 2.5V in offline bias mode and CAN bus is weakly biased to GND in offline mode. In CAN offline mode, the transceiver monitors the CAN bus for a wake-up event if CAN wake-up detection is enabled (CWE = 1). CAN offline bias mode activated automatically when activity is detected on bus while the transceiver is in CAN offline mode. The transceiver will return to CAN offline mode if the CAN bus is silent for longer than $t_{to(silence)}$.

The CAN transceiver switches to offline mode from active or listen-only mode if the CA-IF1169 SBC switches to reset or standby/sleep mode, or the device is in normal mode but CMC = 00. The CAN transceiver will enter offline bias mode first or offline mode directly based on whether the bus is active or has been inactive at least $t_{to(silence)}$; If CAN bus is active, transceiver

switches to offline bias mode first, then goes to CAN offline mode once the bus has been silent for $t_{to(silence)}$.

The CAN transceiver switches to offline/offline bias mode from active mode if CMC = 01 or 10 and the LDO V1 output voltage drops below 90% of V1 nominal value or V1 power-on reset threshold.

The CAN transceiver switches to CAN offline mode from CAN offline bias mode if no activity is detected on bus for t > $t_{to(silence)}$ or when device switches from off/overtemperature protection mode to reset mode. In CAN offline mode, if wake-up detection is enabled (CWE = 1), CAN receiver will monitor CAN bus status and wait for a wake-up event. Once a standard wake-up pattern(WUP) is detected on the CAN bus, the CAN transceiver switches from CAN offline mode to CAN offline bias mode. This autonomous CAN biasing ensures CANH and CANL are always biased to a correct level and allow other nodes on the bus to communicate correctly. The battery supply provides supply voltage for the autonomous CAN bias circuit.

CAN Off Mode

When the CA-IF1169 SBC switches to off mode or overtemperature protection mode, or when the supply voltage drops below CAN bus UVLO detection threshold $V_{UVD(CAN)}$, both CAN transmitter and receiver are fully disabled and leave the bus float. This mode prevents reverse currents flowing from CAN bus when battery supply power-off. When CAN supply voltage rises above the undervoltage recovery threshold $V_{uvr(CAN)}$, the CAN transceiver will switch to offline mode from off mode or overtemperature protection mode.

10.7.4. CAN Transceiver Control Register and Status Register

Table 10-19. CAN transceiver control register (address = 0x20)

Bit	Symbol	Type[1]	Value	Description
7	Reserved	R	-	
6	CFDC	R/W		CAN FD tolerance
			0	Disable CAN FD tolerance
			1	Enable CAN FD tolerance
5	PNCOK	R/W		CAN partial networking configuration
			0	Partial networking register configuration error (standard wake-up pattern only)
			1	Partial networking registers configured correct
4	CPNC	R/W		Selective wake-up configuration
			0	Disable the selective wake-up
			1	Enable the selective wake-up
3:2	Reserved	R	-	
1:0	CMC	R/W		CAN transceiver operating mode selection
			00	Offline mode
			01	Active mode (normal operation); VCC UVLO detection is enabled.
			10	Active mode (normal operation); VCC UVLO detection is disabled.
			11	Silent mode

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 10-20. CAN transceiver status register (address = 0x22)

Bit	Symbol	Type[2]	Value	Description
7	CTS	R		CAN transceiver status
			0	not in active mode
			1	active mode
6	CPNERR	R		CAN partial networking error status
			0	no CAN partial networking error (PNFDE=0 and PNCOK=1)

			1	Detected CAN partial networking error (PNFDE=1 or PNCOK=0), device can be woken via standard wake-up signal only.
5	CPNS	R		CAN partial networking configuration status
			0	CAN partial networking configuration error (PNCOK=0)
			1	CAN partial networking configuration is correct (PNCOK=1)
4	COSCS	R		CAN oscillator status
			0	CAN partial networking oscillator running at incorrect frequency
			1	CAN partial networking oscillator running at correct frequency
3	CBSS	R		CAN bus is silent
			0	CAN bus is active
			1	CAN bus remains inactive longer than $t_{to(silence)}$
2	Reserved	R		
1	VCS [1]	R		VCC supply voltage status
			0	$V_{CC} > V_{uvd(vcc)}$
			1	$V_{CC} < V_{uvd(vcc)}$
0	CFS	R		CAN bus failure
			0	no transmitter dominant timeout
			1	Detected transmitter dominant timeout, disable CAN transmitter

Notes:
1. Active only when CMC = 01 and device is in normal mode;
2. R: Read only; R/W: Read and Write; X: Don't care.

10.8. Wake-up Events

10.8.1. Regular Wake-up Events

Advanced power management and wake-up capability make the CA-IF1169 ideal for the battery power applications. The CA-IF1169 has two regular ways to exit sleep mode:

- Standard remote wake-up **(**CWE = 1)**:** remote CAN wake-up is enabled (CWE = 1), also CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0);
- Local wake-up: state change on WAKE terminal.

Standard Remote Wake-up

If standard remote wake-up detection is enabled (CWE = 1), also selective wake-up is disabled (CPNC = 0 or PNCOK = 0), CAN receiver will monitor CAN bus status and wait for a wake-up pattern(WUP) in offline mode. To improve system operation reliability and prevent false wake-up, the CA-IF1169 receiver features wakeup timeout detection and filtered CAN bus status wakeup detection according to the ISO 11898-2:2016 standard. This means, for a valid dominant and recessive status to be considered, the bus must be kept in that state for more than the t_{wake}. For a standard remote wake-up event to successfully occur, a dominant bus level greater than t_{wake} must be detected and received by the receive channel first to initiate a wake-up event detection; Then the monitor will wait for a valid recessive state (a recessive phase of at least t_{wake}) from CAN bus. Once a valid recessive pulse is received, the bus monitor is waiting for the 2nd valid dominant state, other bus traffic does not reset the bus monitor. Once the receive channel detects a successful wake-up event (a series of valid dominant - recessive - dominant pulses) within the timeout value $t \le t_{to(wake)bus}$, RXD pulls low, the wake-up bit CW in the transceiver event status register(

Table 10-32) is set, see Figure 10-9 for more detail about standard weak-up. If a valid wake-up pattern is received in sleep mode, LDO V1 turns on to provide power supply for microcontroller and SBC goes to standby mode after a system reset.

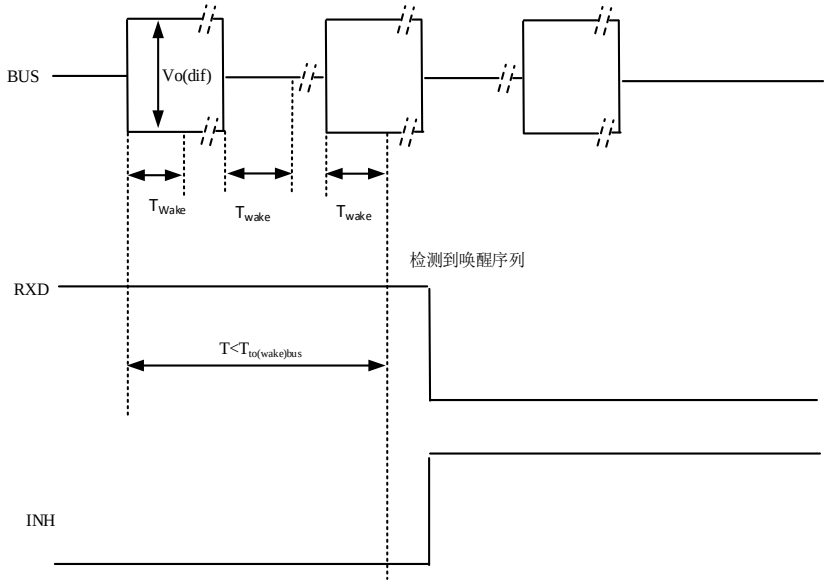


Figure 10-9. Standard remote wake-up

Local Wake-Up

A valid local wake-up request is generated either a low to high rising edge (WPRE = 1), or a high to low falling edge (WPFE = 1) transition on WAKE terminal. The WAKE is a high voltage input terminal. The local wakeup request is active in normal, standby and sleep modes. For the unused local wakeup design, it is recommended to connect pin WAKE to GND to prevent EMI issues. While in normal mode, the CA-IF1169 is able to monitor the status of pin WAKE by reading WPVS bit, see Table 10-21. Otherwise, WPVS is only valid when local wake-up is enabled (WPRE = 1 and/or WPFE = 1).

Table 10-21. WAKE status register (address = 0x4B)

Bit	Symbol	Type[1]	Value	Description
7:2	Reserved	R	-	
1	WPVS	R		WAKE pin status
			0	WAKE voltage below switching threshold ($V_{th(sw)}$)
			1	WAKE voltage above switching threshold ($V_{th(sw)}$)
0	Reserved	R	-	
Note: R: Read only; R/W: Read and Write; X: Don't care.				

10.8.2. Selective Wake-up

The SBC CAN supports selective wake-up according to ISO 11898-2:2016 that can be used to enable the nodes as needed only in a CAN networking. When selective wake is enabled, only the specific or desired wake-up frame (WUF) can wake the device, unless there is some type of error threshold that is hit (such as a decoding error). The selective WUF is based on the CAN frame defined in ISO 11898-1:2015 standard, consisting of identifier field (ID), data length code (DLC), data field and CRC (cyclic redundancy check) code with CRC delimiter. The CA-IF1169 has selective wake control registers to setup the device to detect a programmed match using either the CAN ID, or the CAN ID plus the data frame including data masking. The CAN ID can be a standard (11-bit) format or extended (29-bit) format that is selected by IDE bit in the frame control register (2Fh), see Table 10-26.

A valid WUF identifier is stored in the partial networking ID registers (Table 10-24). The ID mask register (Table 10-25) defines a group of valid identifiers to be detected by individual CAN node, where "1" means 'do not care' the corresponding identifier bit. For example, a standard frame shown in Figure 10-10, the 11-bit identifier is defined as 0x1A0 reserved in ID registers 0x29 and 0x2A. The three least significant bits of the ID mask are set to 1, which means that the corresponding

identifier bits 2 to 0 are 'do not care'. This means any of eight different identifiers from 0x1A0 to 0x1A7 will be recognized as valid wake in the received WUF.

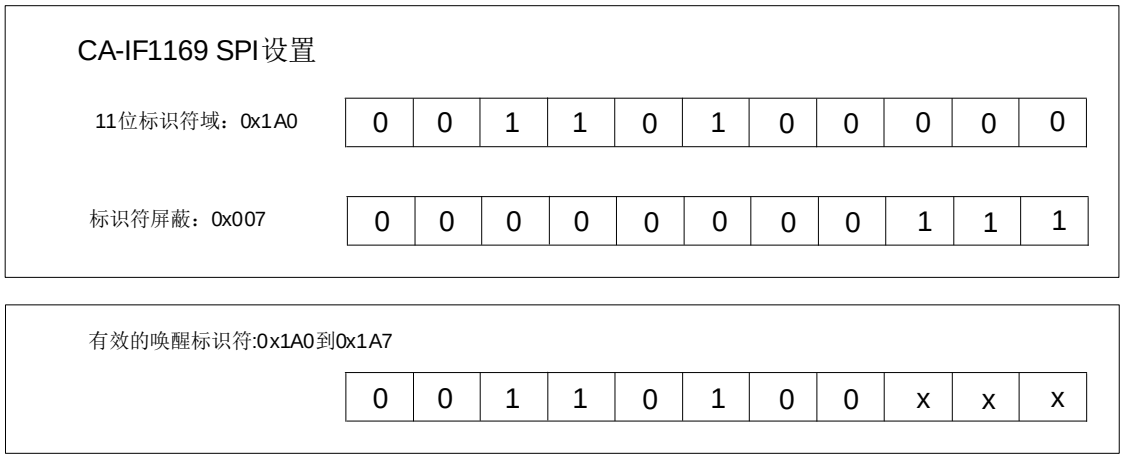


Figure 10-10. Identifier field detection in a selective WUF

The data field defines which CAN nodes to be woken up. The CA-IF1169 compares the incoming data field with the data mask bits (Table 10-27). A single wake-up message can wake-up multiple nodes simultaneously. The data length code (DLC) in the frame control register (Table 10-26) defines the number of data bytes in WUF data field, 0 to 8 bytes. If DLC ≠ 0000, for a successful wake-up, at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register (68h to 6Fh, Table 10-27) must also be set to 1. Each pair of matched "1" indicates a group of nodes to be woken-up, since the data field length is up to 8 byes, there are up to 64 groups of nodes can be defined. If DLC ≠ 0000 and all data mask bits are set to 0, the device cannot be woken up by CAN bus, note that all data mask bits are default "1". If DLC = 0000, a CAN node will wake up if the WUF contains a valid ID and the received data length code is 0000, regardless of the values stored in the data mask. If a WUF contains a valid ID but the DLC in the WUF and the DLC in the frame control register are not matched, the data field will be ignored and there are no CAN nodes wake-up occurred.

Figure 10-11 shows an example for valid WUF data field detection, DLC = 1, the data field is a single byte; This means that device will compare the incoming data filed of WUF with data mask 7 (DM7 in the data mask registers 6Fh). In this example, DM7 = 10101000 and up to three groups of nodes could be woken up (group 1, 3 and 5) if the respective bits in the data frame are also set to 1. In Figure 10-11, the received message could wake up four groups of nodes potentially: groups 2, 3, 4 and 5; As there are two matched bits found (groups 3 and 5) when the message data bits are compared with DM7, group 3 and group 5 can be woken-up.

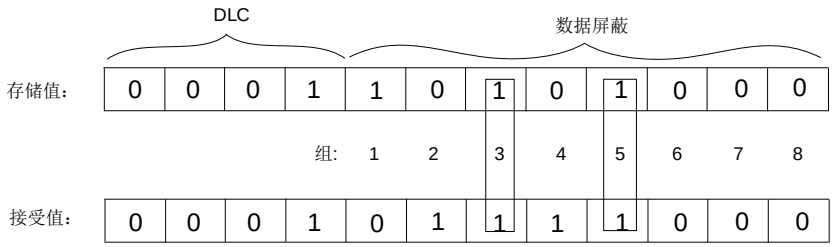


Figure 10-11. Data field detection in a selective wake-up frame

DLC and data filed are optional in wake-up filtering. If PNDM = 0, the data length code and data field will be ignored in the wake-up message evaluation; If PNDM = 1(default), the data field will be included in wake-up message evaluation.

If PNDM = 0, when the following conditions are met, the received frame shall be a valid wake-up frame and CAN wake-up flag (CW) will be set to 1 (CW = 1):

- The identifier field of received WUF is exactly matching the configured pattern in the ID register after filtering, and
- A CRC field has been received, including a recessive CRC delimiter, and no error is detected prior to the acknowledgment(ACK) slot.

If PNDM = 1, a valid wake-up frame is captured and CAN wake-up flag (CW) will be set to 1 when:

- The identifier field of received WUF is exactly matching the configured pattern in the ID register after filtering, and
- the DLC of received CAN data frame is exactly matching the configured DLC, and
- If DLC ≠ 0000, the data field of received frame has at least one bit set in a bit position which corresponds to a set bit in the configured data mask, AND
- A CRC field has been received, including a recessive CRC delimiter, and no error is detected prior to the ACK slot.

The CA-IF1169 has a frame error counter. This error counter determines the CAN frame errors detected by the device. The initial counter value is zero, if the device receives a CAN message with errors (like stuffing error, CRC error or CRC delimiter error) prior to ACK slot, the internal error counter is incremented by 1. If a received CAN message without any errors prior to ACK slot, the counter is decremented by 1 in case of the counter is not zero. Any message received after the CRC delimiter or before the next start of frame (SOF) will be ignored by partial networking and has no impact on the frame error counter. The default value for the frame error counter threshold is 31, so the frame overflow flag PNFDE is set once the counter value > 31, a frame detect error is captured (PNFDE = 1) and the device wakes up. The counter will be reset to zero when CAN transceiver switches to offline mode or partial networking is enabled again. Every time when the error counter is decremented or incremented, device will wait for $n_{bit(idle)}$ recessive bits before considering a dominant bit as a SOF, see Figure 10-12.

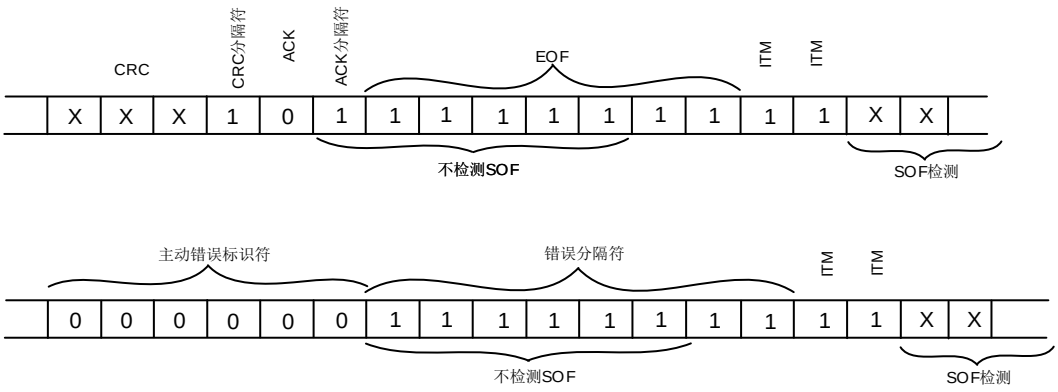


Figure 10-12. SOF detection after Classic CAN frames and error scenarios

If PNCOK is set by the application software, partial networking is assumed to be configured correctly. The CA-IF1169 will clear PNCOK after a write access to any of CAN partial networking configuration registers, see the CAN Partial Networking Configuration Registers. When the CAN transceiver is in offline mode and CAN remote wake-up is enabled (CWE = 1), but selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), any valid wake-up pattern (WUP) will trigger a wake-up event. If the CAN transceiver is not in offline mode (CMC ≠ 00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus will be ignored. If both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver will monitor the bus for a dedicated CAN wake-up frames.

The CA-IF1169 supports 50kbps, 100kbps, 125kbps, 250kbps, 500kbps and 1 Mbps bit-rate configured via CDR bits in the data rate control register (

Table 10-23) during selective wake-up detection.

10.9. CAN Partial Networking (CA-IF1169FDT-Q1/CA-IF1169VFDT-Q1 only)

Partial networking was developed based on the ISO 11898-2:2016 standard. It offers a solution to save power in CAN 2.0 and CAN FD networks by allowing bus communication but sleeping nodes only wake on a specific CAN message or frame. With this additional feature of partial networking, the CA-IF1169 is ideal for the CAN FD and standard CAN 2.0 mixed networks and benefits the network to only enable needed nodes while the rest are in a low power sleep mode without generating bus errors. This is especially important in an automotive setting communications.

As mentioned in Selective Wake-up section, when both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the high-speed transceiver will monitor the bus for a dedicated CAN wake-up frame(WUF).

10.9.1. CAN FD Frame Tolerance

The ISO 11898-2:2016 standard includes the physical layer for high-speed CAN, CAN FD and partial networking. To avoid complicated data decoding operation, partial networking uses high-speed CAN for waking up evaluation. After CAN FD was introduced into the automotive market, all CAN controllers are required to comply with the new standard (FD-active) or at least to tolerate CAN FD communication (FD-passive).

The SBC can be configured to recognize CAN FD frames as valid frames. When CFDC = 1 (Table 10-19), the CA-IF1169 decrements error counter every time the control field of a CAN FD frame is received; When CFDC = 0, the CA-IF1169 treats CAN FD frames as error frames and increments the error counter, this will accumulate the error counter that can overflow and set PNFDE bit, cause a wake-up. As the CAN-FD frame format is different from high-speed CAN frame format, CAN FD frames will never be recognized as valid wake-up frame even if PNDM = 0 (Table 10-26) and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the CA-IF1169 ignores the remaining part of CAN-FD frame by waiting for the next bus idle ($n_{bit(idle)}$ recessive bits).

There are two bit-filter options available to support different combinations of arbitration and data bit-rates:

- Dominant bit-filter 1 ($t_{filtr(bit)dom1}$): data bit-rate ≤ 4 x arbitration-rate, support a maximum data bit-rate of 2 Mbit/s and a maximum arbitration speed of 500 kbit/s;
- Dominant bit-filter 2 ($t_{filtr(bit)dom2}$): data bit-rate ≤ 10 x arbitration-rate or 5 Mbps whichever is lower shall be supported.

Dominant signal filtering time can be configured in the CAN transceiver data-rate register, FD_FL bit, see

Table 10-22 .

10.9.2. CAN Partial Networking Configuration Registers

Table 10-22. Data-rate configuration register (address = 25h)

Bit	Symbol	Type	Value	Description
7	FD_FL	R/w	0	data bit-rate ≤ 4 x arbitration-rate
			1	data bit-rate ≤ 10 x arbitration-rate, or ≤ 5 Mbps
6：0	Reserved	R		

Table 10-23. Data rate control register (address = 0x26)

Bit	Symbol	Type	Value	Description
7:3	Reserved	R	-	
2:0	CDR	R/W		CAN data-rate selection
			000	50 kbps

			001	100 kbps
			010	125 kbps
			011	250 kbps
			100	Reserved
			101	500 kbps
			110	Reserved
			111	1000 kbps

Table 10-24. Partial networking ID register (address = 0x27– 0x2A)

Address	Bit	Symbol	Type[1]	Value	Description
27h	7:0	ID7:ID0	R/W		extended frame format: ID7 to ID0
28h	7:0	ID15:ID08	R/W		extended frame format: ID15 to ID8
29h	7:2	ID23:ID18	R/W		extended frame format: ID23 to ID18 standard frame format: ID5 to ID0
	1:0	ID17:ID16	R/W		extended frame format: ID17 to ID16
2Ah	7:5	Reserved	R	-	
	4:0	ID28:ID24	R/W		extended frame format: ID28 to ID24 standard frame format: ID10 to ID6
Note: R = Read only; R/W = Read and Write; X= Don't care.					

Table 10-25. Partial networking ID mask register (address = 0x2Bh – 0x2E):

Address	Bit	Symbol	Type	Value	Description
2Bh	7:0	M7:M0	R/W		extended frame format: mask for ID bits 7 to 0
2Ch	7:0	M15:M8	R/W		extended frame format: mask for ID bits 15 to 8
2Dh	7:2	M23:M18	R/W		extended frame format: mask for ID bits 23 to 18 standard frame format: mask for ID bits 5 to 0
	1:0	M17:M16	R/W		extended frame format: mask for ID bits 17 to 16
2Eh	7:5	Reserved	R	-	
	4:0	M28:M24	R/W		extended frame format: mask for ID bits 28 to 24 standard frame format: mask for ID bits 10 to 6
Note: R=Read only; R/W= Read and Write; X= Don't care.					

Table 10-26. Frame control register (address = 0x2F)

Bit	Symbol	Type[1]	Value	Description
7	IDE	R/W		partial networking identifier format
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W		mask for partial networking data
			0	ignore data length code and data field at wake-up
			1	detect data length code and data field at wake-up
5:4	Reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame
			0000	0 bytes
			0001	1 bytes
			0010	2 bytes
			0011	3 bytes
			0100	4 bytes
			0101	5 bytes
			0110	6 bytes
			0111	7 bytes
			1000	8 bytes
			1001 to 1111	8 bytes

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 10-27. Data mask registers [2] (address = 0x68 – 0x6F)

Address	Bit	Symbol	Type[1]	Value	Description
68h	7:0	DM0	R/W		Data mask 0 configuration
69h	7:0	DM1	R/W		Data mask 1 configuration
6Ah	7:0	DM2	R/W		Data mask 2 configuration
6Bh	7:0	DM3	R/W		Data mask 3 configuration
6Ch	7:0	DM4	R/W		Data mask 4 configuration
6Dh	7:0	DM5	R/W		Data mask 5 configuration
6Eh	7:0	DM6	R/W		Data mask 6 configuration
6Fh	7:0	DM7	R/W		Data mask 7 configuration

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.
2. All data mask bits are set to 1 by power-on reset default.

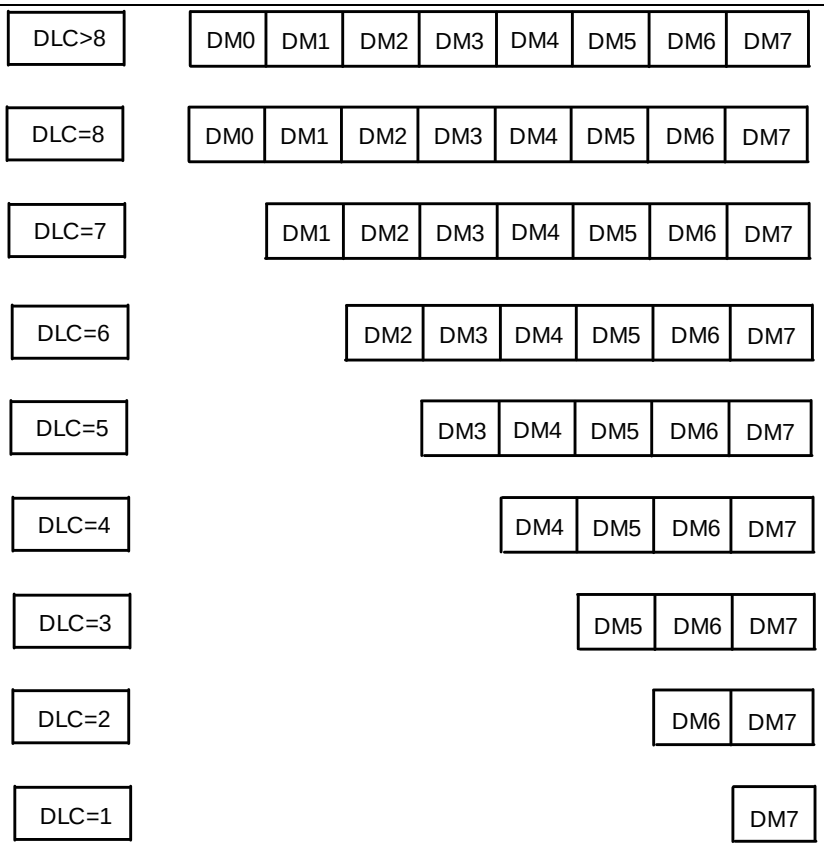


Figure 10-13. Data mask register configuration

10.10. Interrupt and Wake-up Event Diagnosis

10.10.1. Interrupt Sources Detection

RXD can be used as an interrupt for the external microcontroller when a wake-up event occurred or an interrupt source triggered. The CA-IF1169 provides wake-up and interrupt event diagnosis. This kind information is stored in the event status registers, see Table 10-30 to Table 10-33. The power-on (PO) and partial networking frame detection error (PNFDE) interrupt sources are always be enabled, other interrupt sources are maskable, wake-up detection can be enabled/disabled in the event capture enable registers. The relevant event status bit is set when an event occurred (if enabled). The microcontroller can monitor events/interrupt sources by reading the event status registers through SPI interface. A global event status register (Table 10-30 错误!未找到引用源。) is provided to speed-up software polling routines and determine the type of event captured (internal controller, transceiver or wake-up interrupts), then access the relevant register as needed. Once an interrupt source has been identified, the status flag should be cleared by writing 1 to the relevant register bit, writing 0 will have no effect. A number of status bits can be cleared with a single write operation(writing 1) to all relevant bits. However, we recommend to clear the status bits that were set only when the status registers were last read. This ensures that events triggered just before the write operation.

If the CA-IF1169 is in standby mode or CAN transceiver is in offline mode, pin RXD is forced low to indicate that a wake-up or interrupt event has been detected; If the CA-IF1169 is in sleep mode when an event (except SPIF interrupt) occurred, the device switches to standby mode. When the device is in standby mode or sleep mode, any enabled wake-up event detected will trigger a wake-up. If CAN transceiver is in active or silent mode, both the standard remote wake-up and WUF can not trigger CW interrupt and CW will not be set, a local wake-up on pin WAKE will trigger a wake-up and set CW to 1.

Table 10-28. Regular wake-up events

Symbol	Event	POR(default status)	Description
CW	Standard CAN bus wake-up	disabled	The CA-IF1169 detected a CAN bus wake-up event while the transceiver in offline mode.
WPR	Local wake-up: rising edge	disabled	The CA-IF1169 detected a low to high rising edge on WAKE terminal.
WPF	Local wake-up: falling edge	disabled	The CA-IF1169 detected a high to low falling edge on WAKE terminal.

After power-on reset, PO is set to 1 and place pin RXD to low. RXD terminal is released only after PO bit cleared. Therefore, only when the PO is cleared, the CA-IF1169 device can enter sleep mode. Otherwise, sending MC = 001 command through SPI will only place the device into standby mode, not sleep mode. CAN bus silent (CBS bit) is detected only when CBSE = 1 while bus active; If there is no activity on CAN bus for $t_{to(silence)}$, CBS bit is set. CBS doesn't trigger interrupt when the transceiver first enters silent mode after power-on reset. After CAN bus is active, CAN bus silent will trigger interrupt when CBS bit is set. CAN bus failure flag (CF) is used for the transmitter dominant timeout indication and LDO V1 UVLO event (CMC = 01) indication. Once a transmitter dominant timeout or LDO V1 UVLO condition is detected, CAN bus failure flag (CF) is set to 1. The CA-IF1169 enters sleep mode only after this bit is cleared to zero. In sleep mode, the device can detect SPI failure, but doesn't trigger wake-up. When the device junction temperature > $T_{th(warn)otp}$ (in normal mode only), if enabled by OTWE, OTE will be set to 1. After this bit is cleared to zero, if the junction temperature is still above $T_{th(warn)otp}$, OTW will be set again. See Table 10-29 for more details about the interrupt sources.

Table 10-29. Interrupt sources

Symbol	Event	POR (default status)	Description
PO	Power-on	always enabled	Transceiver exited offline mode after battery supply applied.
OTW	Overtemperature alarm	disabled	Junction temperature > $T_{th(warn)otp}$ (detected in normal mode only)
SPIF	SPI fault	disabled	SPI clock count error, illegal MC code or attempt to write the locked register.
PNFDE	PN frame detection error	always enabled	partial networking frame detection error
CBS	CAN bus silent	disabled	CAN bus remains inactive at least $t_{to(silence)}$ (detected in normal mode and CBSE = 1 only).
CF	CAN bus fault	disabled	One of the following CAN failure detected (not in sleep mode): --Transmitter dominant timeout; -- V_{CAN} UVLO event (CMC=01).

10.10.2. Interrupt and Wake-up Delay

When the CAN transceiver is in offline mode, if interrupt resources trigger or wake-up events occur frequently, this may cause significant impact on the software processing, because pin RXD will be driven to low level repeatedly and do not have enough time to get response from external microcontroller each time when an interrupt/wake-up is generated. To solve this potential problem, the CA-IF1169 integrates an interrupt/wake-up delay timer to limit the disturbance to the software. When one of event capture status bits is cleared, pin RXD is released, the timer is reset and start counting. If further events occur while the timer is counting, the relevant status bits will be set to 1. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes low again to indicate the microcontroller. In this way, the microcontroller is interrupted only once to process a number of captured events, thus to avoid software processing conflicts. If all active event capture bits have been cleared when the timer expires after $t_{d(event)}$, pin RXD remains high level. The event capture registers can be read at any time.

10.10.3. Event Status Register

Table 10-30 to

Table **10-37** show the CA-IF1169 events status and events capture status. Note that, after an event source has been identified, the status flag should be cleared by writing 1 to the correspond status bit.

Table 10-30. Global event status register (address = 0x60)

Bit	Symbol	Type [1]	Value	Description
7:5	Reserved	R	-	
4	FSE	R		Functional safety event
			0	No functional safety event captured
			1	functional safety event pending in 0x65
3	WPE	R		WAKE local wake-up event
			0	no local wake-up on WAKE captured
			1	WAKE local wake-up event pending at address 0x64
2	TRXE	R	-	transceiver event
			0	no transceiver event captured
			1	transceiver event pending at address 0x63
1	Reserved	R	-	
0	SYSE	R		system event
			0	no system event
			1	system event pending at address 0x61

Table 10-31. System event status register (address = 0x61)

Bit	Symbol	Type	Value	Description
7:5	Reserved	R	-	
4	PO [1]	R/W		power-on indication
			0	power off
			1	device left off mode after battery power-on
3	Reserved	R	-	
2	OTW	R/W		Overtemperature alarm
			0	junction temperature < $T_{th(warn)otp}$
			1	junction temperature ≥ $T_{th(warn)otp}$
1	SPIF	R/W		SPI failure indication
			0	no SPI failure
			1	detected SPI failure
0	Reserved	R	-	

Note:
1. PO is cleared when device is forced to sleep mode due to UVLO event. This information could be lost because of UVLO event. Bit NMS, which is set to 0 when device returns to normal operation mode after power-on, this can compensates for PO losing.

Table 10-32. Transceiver event status register (address = 0x63)

Bit	Symbol	Type	Value	Description
7:6	Reserved	R	-	
5	PNFDE	R/W		partial networking frame detection error
			0	no error detected
			1	detected partial networking frame error
4	CBS	R/W		CAN bus status
			0	CAN bus active
			1	CAN bus inactive for > $t_{to(silence)}$
3:2	Reserved	R	-	
1	CF [1]	R/W		CAN bus fault
			0	no bus fault
			1	detected bus fault
0	CW	R/W		CAN bus wake-up
			0	no wake-up event
			1	detected CAN wake-up event

Note:
1. CF is only enabled when CAN transceiver is in active mode. This bit is triggered if transmitter dominant timeout or VCC UVLO event is detected (when CMC = 01).

Table 10-33. WAKE wake-up event status register (address = 0x64)

Bit	Symbol	Type [1]	Value	Description
7:2	Reserved	R	-	
1	WPR	R/W		WAKE pin rising edge
			0	No rising edge wake-up on WAKE pin
			1	Detected rising edge wake-up on WAKE pin
0	WPF	R/W	-	WAKE pin falling edge
			0	No falling edge wake-up on WAKE pin
			1	Detected falling edge wake-up on WAKE pin

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

Table 10-34. System event enable control register (address = 0x04)

Bit	Symbol	Type	Value	Description
7:3	Reserved	R	-	
2	OTWE	R/W		Over-temperature alarm enable control
			0	disable over-temperature alarm
			1	enable over-temperature alarm
1	SPIFE	R/W	-	SPI failure detection enable control
			0	disable SPI failure detection
			1	enable SPI failure detection
0	Reserved	R	-	

Table 10-35. Regulator event enable control register (address = 0x1C)

Bit	Symbol	Type	Value	Description
7:3	Reserved	R	-	
2	V2OE	R/W		V2 overvoltage detection enable control
			0	V2 overvoltage detection disabled
			1	V2 overvoltage detection enabled
1	V2UE	R/W	-	V2 undervoltage detection enable control
			0	V2 undervoltage detection disabled
			1	V2 under voltage detection enabled
0	V1UE	R/W	-	V1 undervoltage detection enable control
			0	V1 undervoltage detection disabled
			1	V1 under voltage detection enabled

Table 10-36. Transceiver event capture enable control register (address = 0x23)

Bit	Symbol	Type	Value	Description
7:5	Reserved	R	-	
4	CBSE	R/W		CAN bus silent detection enable control
			0	enable CAN bus silent detection
			1	disable CAN bus silent detection
3:2	Reserved	R	-	
1	CFE	R/W		CAN bus failure detection enable control
			0	disable CAN bus failure detection
			1	enable CAN bus failure detection
0	CWE	R/W		CAN bus wake-up detection enable control
			0	disable CAN bus wake-up detection

			1	enable CAN bus wake-up detection

Table 10-37. WAKE pin local wake-up enable register (address = 0x4C)

Bit	Symbol	Type [1]	Value	Description
7:2	Reserved	R	-	
1	WPRE	R/W		WAKE rising edge wake-up enable control
			0	Disable rising edge wake-up detection
			1	Enable rising edge wake-up detection
0	WPFE	R/W		WAKE falling edge wake-up enable control
			0	Disable falling edge wake-up
			1	Enable falling edge wake-up

Note:
1. R: Read only; R/W: Read and Write; X: Don't care.

10.11. SPI Interface

The CA-IF1169 has a SPI compatible interface used to read event or interrupt information, read diagnostic data, and configure all of the registers. Each configuration register can be read back to ensure proper configuration. The CA-IF1169 communicates with microcontroller through the SPI-compatible 4-wire serial interface:

- Three inputs: clock input (SCK), chip select (SCSN), and data input (SDI)
- One output: data output SDO

The CA-IF1169 is the slave device in a SPI communication with the microcontroller being the master. The SCSN input is used to initiate and terminate a data transfer. SCK is used to synchronize data movement between the master (microcontroller) and the slave device. SCSN must be low to clock data into or out of the device, and SDI must be stable when sampled on the rising edge of SCK. SDO is stable on the rising edge of SCK. The device ignores all activity on SCK and SDI except when SCSN is low, see Figure 9-5. SPI timing diagram and Dynamic Characteristics to find more details about SPI timing characteristics.

The CA-IF1169 supports 16-bit, 24-bit and 32-bit SPI read/write operation. For the 16-bit read/write operation, SPI communication packet is composed of two serial bytes. The first byte specifies the 7 bits address of the CA-IF1169 internal SPI register to be accessed (read or write) and 1 bit read/write control bit(LSB). The second byte in the packet consists of either the data to be written into the addressed CA-IF1169 SPI register (using SDI), or the data read from the addressed CA-IF1169 SPI register (using SDO). If read/write control bit is "0", the device performs write operation and the designated internal SPI register will be updated with the supplied write data (second data byte); if read/write control bit is "1", the device performs read operation and ignores SDI input data. During SPI data read or data write operation, the contents of the addressed register will be returned via pin SDO.

In 24-bit or 32-bit read/write operation, the register address is automatically incremented, as shown in Figure 10-14. During a SPI data read or write operation, the contents of the addressed register will be clocked out from SDO. If the write address provided does not correspond to a physical available internal register, no internal register update will occur in the SPI write operation and the SPI input data is discarded, also do not assert SPI fault event. During SPI write operation, the device counts the number of SCK pulses. If it is not a multiple of 8 (16, 24 or 32), the SPI input data is discarded and SPI failure event is captured, SPI failure flag bit SPIF is set. In SPI read operation, if more than 32 bits data are clocked into the CA-IF1169 via SDI, the data stream on SDI will be returned via SDO from bit 33 onwards.

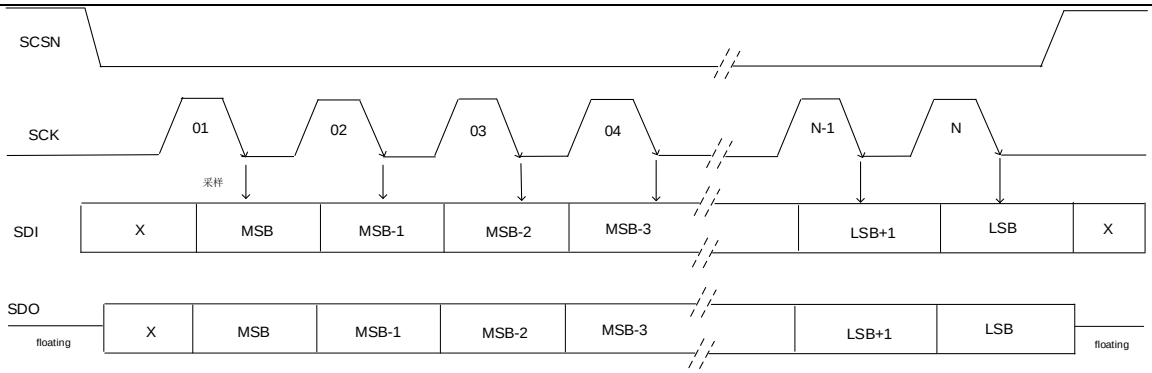


Figure 10-14. SPI communication protocol

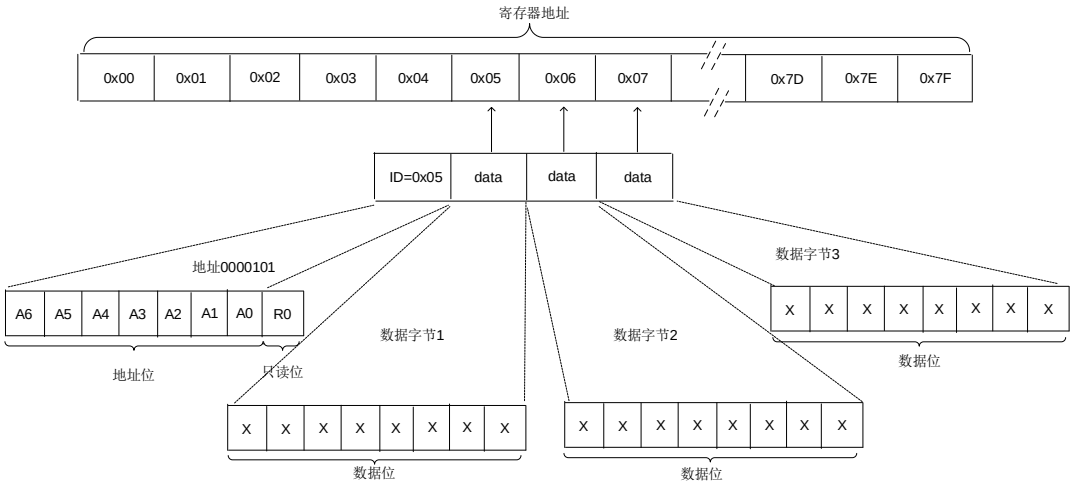


Figure 10-15. SPI write operation

10.12. Register Map and Configuration

10.12.1. Device ID

The CA-IF1169 series of devices includes four parts: CA-IF1169DT-Q1, CA-IF1169VDT-Q1, CA-IF1169FDT-Q1, and CA-IF1169VFDT-Q1 which features different internal regulator output voltages and with or without partial networking support, see Table 5-1. Ordering Information for more detail. The CA-IF1169 includes a read-only register (address = 0x7E) to reserve the CA-IF1169 digital identification code, see Table 10-38 .

Table 10-38. Device ID register (address = 0x7E)

Bit	Symbol	Type	Value	Description
7:0	IDS[7:0]	R		Part number:
			CFh	CA-IF1169WDT-Q1
			C9h	CA-IF1169VWDT-Q1
			E9h	CA-IF1169VFDT-Q1
			EFh	CA-IF1169FDT-Q1

10.12.2. Lock Control Register

The CA-IF1169 provides a write-protected register to protect against unintended modifications. This only protects locked bits from being modified via the SPI and doesn't prevent the device updating status registers, see Table 10-40.

Table 10-39. Lock control register [1] (address = 0x0A)

Bit	Symbol	Type	Value	Description
7	Reserved	R	-	
6	LK6C	R/W		0x68 to 0x6F partial networking data byte registers lock control
			0	Enable SPI write
			1	Disable SPI write
5	LK5C	R/W		0x50 to 0x5F lock control
			0	Enable SPI write
			1	Disable SPI write
4	LK4C	R/W		0x40 to 0x4F WAKE configuration registers lock control
			0	Enable SPI write
			1	Disable SPI write
3	LK3C	R/W		0x30 to 0x3F registers lock control
			0	Enable SPI write
			1	Disable SPI write
2	LK2C	R/W		0x20 to 0x2F transceiver and partial networking registers lock control
			0	Enable SPI write
			1	Disable SPI write
1	LK1C	R/W		0x10 to 0x1F registers lock control
			0	Enable SPI write
			1	Disable SPI write
0	LK0C	R/W		0x06 to 0x09 registers lock control
			0	Enable SPI write
			1	Disable SPI write

Notes:
1. The CA-IF1169 protects the locked bits from being modified through SPI interface only.

10.12.3. Register Map

The CA-IF1169 includes 128 addressable registers with addresses from 0x00 to 0x7F. Table shows the register summary and provides descriptions for each bit.

Table 10-40. System control registers summary

Address	Register	Bit							
System control registers									
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Watchdog mode control	WMC			Reserved	NWP			
0x01	Mode control	Reserved					MC		
0x02	Functional safety	Reserved					LHC	RCC	
0x03	Main status	FSMS	OTWS	NMS	Reserved				
0x04	System event enable	Reserved					OTWE	SPIFE	Reserved
0x06	General-purpose register 0	GPM[7:0]							
0x07	General-purpose register 1	GPM[15:8]							
0x08	General-purpose register 2	GPM[23:16]							
0x09	General-purpose register 3	GPM[31:24]							
0x0A	Lock control	Reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C
Regulator registers									
0x10	Regulator control	Reserved	PDC	Reserved		V2C		V1RTC	
0x1B	Regulator status	Reserved					V2S		V1S
0x1C	Regulator events	Reserved					V2OE	V2UE	V1UE
0x1D	Functional safety status	Reserved	VBAT_OVS	V2OCS	V1OCS	V1OVS	RSTN_STUCK1_S	LIMP_STUCK_S	RXD_STUCK_S
0x4D	Functional safety events control	Reserved	VBAT_OVE	V2OCE	V1OCE	V1OE	RSTN_STUCK1_EN	LIMP_STUCK_EN	RXD_STUCK_EN
Transceiver control and partial networking registers									
0x20	CAN control	Reserved	CFDC	PNCOK	CPNC	Reserved		CMC	
0x22	CAN transceiver status	CTS	CPNERR	CPNS	COSCS	CBSS	Reserved	VCS	CFS
0x23	Transceiver event enable	Reserved			CBSE	Reserved		CFE	CWE
0x25	FD filtering bit-rate select	FD_FL	Reserved						
0x26	Data rate	Reserved					CDR		
0x27	Identifier 0	ID[7:0]							
0x28	Identifier 1	ID[15:8]							
0x29	Identifier 2	ID[23:16]							
0x2A	Identifier 3	Reserved			ID[28:24]				
0x2B	Mask 0	M[7:0]							
0x2C	Mask 1	M[15:8]							
0x2D	Mask 2	M[23:16]							
0x2E	Mask 3	Reserved			M[28:24]				
0x2F	Frame control	IDE	PNDM	Reserved		DLC			
0x68	Data mask 0	DM0[7:0]							
0x69	Data mask 1	DM1[7:0]							
0x6A	Data mask 2	DM2[7:0]							
0x6B	Data mask 3	DM3[7:0]							
0x6C	Data mask 4	DM4[7:0]							
0x6D	Data mask 5	DM5[7:0]							
0x6E	Data mask 6	DM6[7:0]							
0x6F	Data mask 7	DM7[7:0]							
WAKE control and status registers									
0x4B	Pin WAKE status	Reserved						WPVS	Reserved
0x4C	Local wake-up enable	Reserved						WPRE	WPFE
Event Capture registers									
0x60	Event capture status	Reserved			FSE	WPE	TRXE	SUPE	SYSE
0x61	System event status				PO	Reserved	OTW	SPIF	WDF
0x62	Regulator event status	Reserved					V2O	V2U	V1U
0x63	Transceiver event status	Reserved		PNFDE	CBS	Reserved		CF	CW
0x64	Pin WAKE status	Reserved						WPR	WPF
0X65	Functional safety event status	Reserved	VBAT_OV	V2C	V1C	V1O	RSTN_STUCK1	LIMP_STUCK	RXD_STUCK
0x66	ABIST status	Reserved				V1_UVRST_ABIST	V1_UV_ABIST	V2_UV_ABIST	V2_OV_ABIST
NV memory									
0x70	NV register status	Reserved		WRCNTS[3]	WRCNTS[2]	WRCNTS[1]	WRCNTS[0]	ECCS	NVMPS
0x73	Start-up control	Reserved		RLC		V2SUC	Reserved		
0x74	SBC configuration control	Reserved			V1RTSUC[1]	V1RTSUC[0]	FNMC	SDMC	Reserved

0x75	CRC	CRCC[7]	CRCC[6]	CRCC[5]	CRCC[4]	CRCC[3]	CRCC[2]	CRCC[1]	CRCC[0]
Identifier registers									
0x7E	Identifier	IDS[7:0]							

Note that, the CA-IF1169 has 4 bytes of memory for general-purpose registers used to store user information. The general purpose registers can be accessed via the SPI at address 0x06 to 0x09.

10.12.4. Non volatile Memory Programming

The CA-IF1169 CAN SBC devices are delivered with factory preset of SBC operation mode in the forced normal mode (FNMC=1 and NVMPS=1): the watchdog is disabled, dual voltage regulators are turned on, and the CAN transceiver is in active mode. The factory programmed setting are located in nonvolatile (NV) memory (73h to 74h), see Table 10-40. User can change the factory preset to meet different application requirements and setup the SBC to operate in different power-on reset states. However, the NV memory can be reprogrammed a maximum of 2 times ($n_{cyc(W)}$). The NVMPS bit in the NV memory status register (Table 10-41) indicates whether the non-volatile units can be reprogrammed. This register also contains a write counter, WRCNTS, which incremented by 1 every time a NV memory is reprogrammed. The maximum value of WRCNTS is “2” and there is no overflow assert; The counter also increments during factory reset. This counter is for customer reference only and reprogramming will not be rejected when the maximum value is reached.

The programming of NV memory is performed in two steps. First, write the user configuration data into addresses 73h and 74h; Second, confirm the reprogramming setting by writing correct CRC(cyclic redundancy checks) value into the non-volatile memory CRCC control register (see Table 10-42). Once the CRC value is verified, SBC starts reprogramming the NV memory. If the CRC value is incorrect, reprogramming will be aborted. The non-volatile memory cannot be read out during reprogramming. After the NV memory programming cycle is completed and user configuration has been successfully reprogrammed, a new system power-on reset is generated. Then the NV memory will be protected and will not be overwritten. When the battery supply is applied pin BAT and power-on again, the SBC will operate according to the updated setting. The error correction code status bit ECCS (Table 10-41) is set to indicate that the CRC check mechanism in SBC has detected and a single bit fault in NV memory has been corrected. If more than one bit failure is detected, the SBC will not restart after reprogramming the NV memory.

The factory preset value can be restored if the following steps are performed and the RSTN, CAN bus status are kept for at least $t_{d(MTPNV)}$ during battery supply power-up:

a) VBAT powered-off;
b) Pin RSTN is forced low;
c) Pull-up CANH to V_{BAT};
d) Pull-down CANL to Low;
e) V_{BAT} is powered on (above 7.5V) and the durations of steps b), c) and d) are maintained for not less than td (MTPNV)
f) First, release the low level of RSTN, then release the high level of CANH and CANL, and keep the VBAT level.

After the factory preset has been restored, the SBC performs a system power-on reset and enters forced normal mode. Since the CAN-bus is clamped dominant, pin RXD is placed at low-level. Pin RXD is forced high during the factory preset restore process ($t_{d(MTPNV)}$). A falling edge on RXD caused by setting bit PO =1 after power-on indicates that the factory preset process has been completed. Note that the write counter, WRCNTS, is incremented by 1 every time the factory presets are restored.

Table 10-41. NV memory status register (address = 0x70)

Bit	Symbol	Type	Value	Description
7:6	Reserved	R	-	-
5:2	WRCNTS	R	-	Write counter status:
			XXXX	The number of NV memory reprogrammed times
1	ECCS	R		Error correction code status:
			0	no bit failure detected
			1	bit failure detected and corrected in NV memory
0	NVMPS	R		NV memory programming status:

			0	memory cannot be overwritten
			1	NV memory is ready for reprogramming

A 8-bit CRC (cyclic redundancy checks) is stored in the NV CRC control register (CRCC, Table 10-42). This CRC is used for error detection when reprogramming the NV memory. The CRC is generated according to the standardized CRC-polynomial function: $X^8 + X^5 + X^3 + X^2 + X + 1$. The result of this operation must be bitwise inverted. The CRC is computed using the 2-bytes data stored in 73h and 74h as shown in Figure 10-16.

Table 10-42. NV memory CRC control register (address = 0x75)

Bit	Symbol	Type	Value	Description
7:0	CRCC	R/W	-	CRC control:
			-	CRC control data

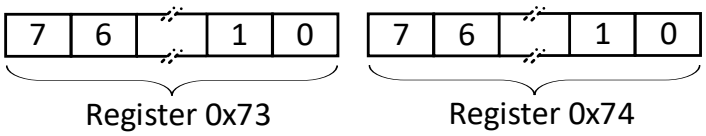


Figure 10-16. Data representation for CRC calculation

The following parameters can be used to calculate the CRC value:

Table 10-43. Parameters for CRC coding

Parameters	Value
CRC result width	8 bits
Polynomial	2Fh
Initial value	FFh
Input data reflected	no
Result data reflected	no
XOR value	FFh

Alternatively, the following algorithm can be used:

```
data = 0   // unsigned byte
crc = FFh
for i = 0 to 1
      data = content_of_address(73h + i) EXOR crc
      for j = 0 to 7
            if data ≥ 128
                  data = data * 2  // shift left by 1
                  data = data EXOR 2Fh
            else
                  data = data * 2 // shift left by 1
      next j
      crc = data
next i
crc = crc EXOR FFh
```

10.12.5. Register Configuration

Table 10-44 shows the register configuration status in different mode changes. Some register bits may change state

automatically when the CA-IF1169 switches from one operating mode to another, especially when the device switches to off mode because of the battery voltage is too low, or switches to sleep mode because of an UVLO event. If the CA-IF1169 changes operation mode during SPI communication, data transmission will be ignored.

Table 10-44. Register configuration @ different modes

Symbol	Off (POR)[1]	Standby	Normal	Sleep	Overtemperature Protection	Sleep_UVLO[2]
CBS	0	no change	no change	no change	no change	0
CBSE	0	no change	no change	no change	no change	no change
CBSS	1	actual state	actual state	actual state	actual state	actual state
CDR	101	no change	no change	no change	no change	no change
CF	0	no change	no change	no change	no change	0
CFDC	0	no change	no change	no change	no change	no change
CFE	0	no change	no change	no change	no change	no change
CFS	0	actual state	actual state	actual state	actual state	actual state
CMC	01	no change	no change	no change	no change	no change
COSCS	0	actual state	actual state	actual state	actual state	actual state
CPNC	0	no change	no change	no change	no change	0
CPNERR	1	actual state	actual state	actual state	actual state	actual state
CPNS	0	actual state	actual state	actual state	actual state	actual state
CTS	0	0	actual state	0	0	0
CW	0	no change	no change	no change	no change	0
CWE	0	no change	no change	no change	no change	1
DMn	11111111	no change	no change	no change	no change	no change
DLC	0000	no change	no change	no change	no change	no change
ECCS	actual state	actual state	actual state	actual state	actual state	actual state
FD_FL	0	no change	no change	no change	no change	no change
FNMC	0	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
FNMS	0	actual state	actual state	actual state	actual state	actual state
GPMn	00000000	no change	no change	no change	no change	no change
IDn	00000000	no change	no change	no change	no change	no change
IDE	0	no change	no change	no change	no change	no change
IDS	01110100	no change	no change	no change	no change	no change
LHC	0	no change	no change	no change	If t > td(limp), otherwise remain unchanged	If RCC = 3 or t > td(limp), otherwise it remains unchanged.
LKnC	0	no change	no change	no change	no change	no change
MC	100	100	111	001	don’t care	001
NMS	1	no change	0	no change	no change	no change
NVMPS	actual state	actual state	actual state	actual state	actual state	actual state
NWP	0100	no change	no change	no change	0100	0100
OTW	0	no change	no change	no change	no change	0
OTWE	0	no change	no change	no change	no change	no change
OTWS	0	actual state	actual state	actual state	actual state	actual state
PDC	0	no change	no change	no change	no change	no change
PNCOK	0	no change	no change	no change	no change	0
PNDM	1	no change	no change	no change	no change	no change
PNFDE	0	no change	no change	no change	no change	0
PO	1	no change	no change	no change	no change	0
RCC	00	no change	no change	no change	no change	RCC++
RLC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
RSS	00000	no change	no change	no change	10010	Reset source
SDMC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SDMS	0	actual state	actual state	actual state	actual state	actual state

SLPC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SPIF	0	no change	no change	no change	no change	no change
SPIFE	0	no change	no change	no change	no change	no change
SUPE	0	no change	no change	no change	no change	no change
SYSE	1	no change	no change	no change	no change	no change
TRXE	0	no change	no change	no change	no change	no change
V1RTC	V1RTSUC	no change	no change	no change	no change	no change
V1RTSUC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
V1S	0	actual state	actual state	actual state	actual state	actual state
V1UE	0	no change	no change	no change	no change	no change
V1U	0	no change	no change	no change	no change	no change
VCS	0	actual state	actual state	actual state	actual state	actual state
V2C	V2SUC	no change	no change	no change	no change	no change
V2O	0	no change	no change	no change	no change	no change
V2OE	0	no change	no change	no change	no change	no change
V2S	00	actual state	actual state	actual state	actual state	actual state
V2SUC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
V2U	0	no change	no change	no change	no change	no change
V2UE	0	no change	no change	no change	no change	no change
WDF	0	no change	no change	no change	no change	no change
WDS	0	actual state	actual state	actual state	actual state	actual state
WMC	If SDMC = 1, then it is 001; otherwise, it is 010.	no change	no change	no change	no change	If SDMC = 1, then it is 001; otherwise, it is 010.
WPE	0	no change	no change	no change	no change	no change
WPF	0	no change	no change	no change	no change	no change
WPR	0	no change	no change	no change	no change	no change
WPFE	0	no change	no change	no change	no change	no change
WPRE	0	no change	no change	no change	no change	no change
WPVS	0	no change	no change	no change	no change	no change
WRCNTS	actual state	actual state	actual state	actual state	actual state	actual state

11. Application Information

The CA-IF1169 CAN SBC is typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. 错误!未找到引用源。 shows the typical application circuit for the CA-IF1169. An external series diode is used to prevent reverse currents from flowing into the device if the battery or ground connection is lost. In 错误!未找到引用源。, internal LDO V1 is connected with MCU logic power supply input and provides a logic-compatible between the microcontroller logic I/O and the SBC RXD, TXD and SPI interface.

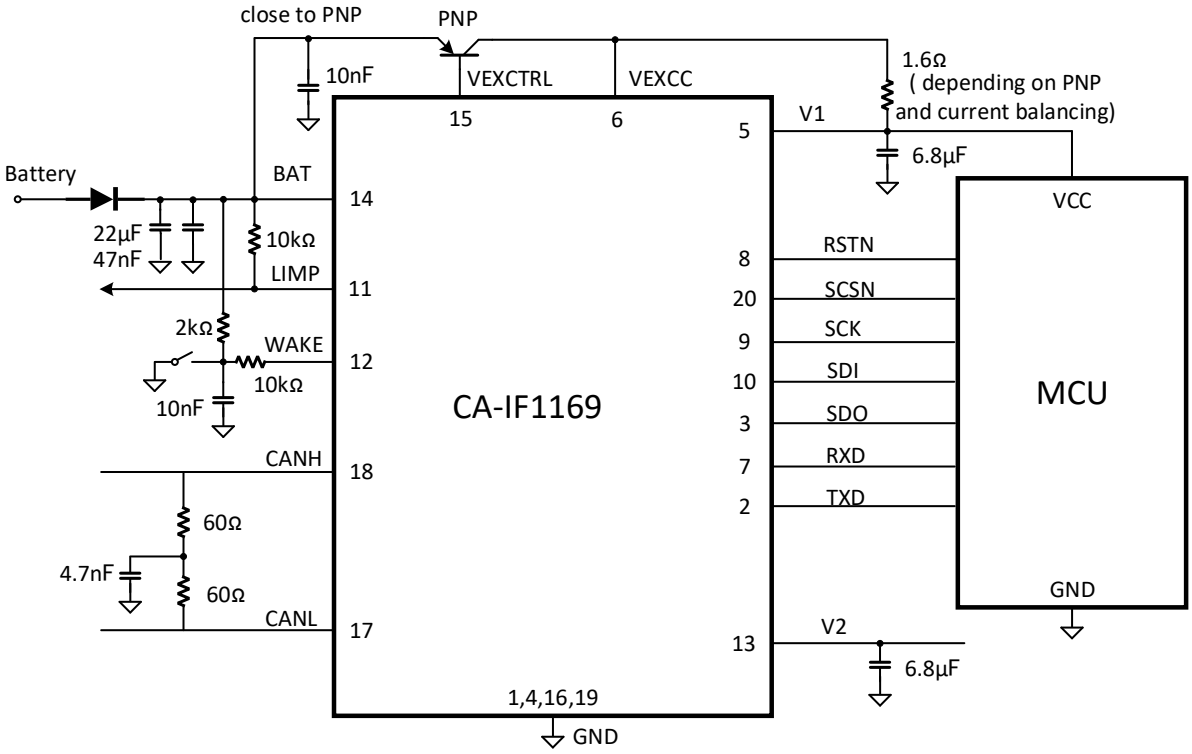


Figure 11-1. CA-IF1169 typical application circuit

12. Package Information

DFN20 Package Outline

The following figure illustrates the size drawing and recommended pad size of DFN20 package. All dimensions are in millimeters.

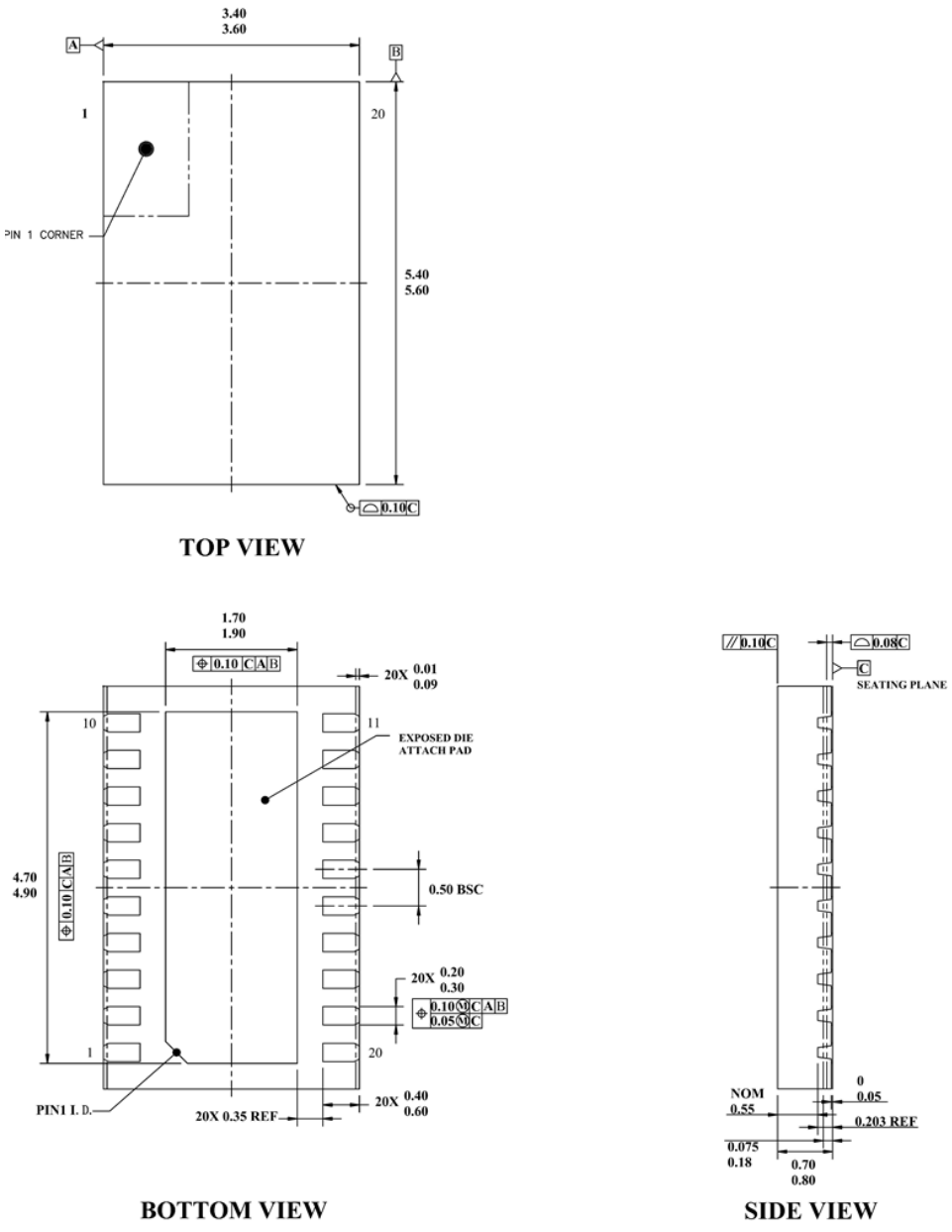


Figure 12-1. DFN20 package outline

13. Soldering Temperature (reflow) Profile

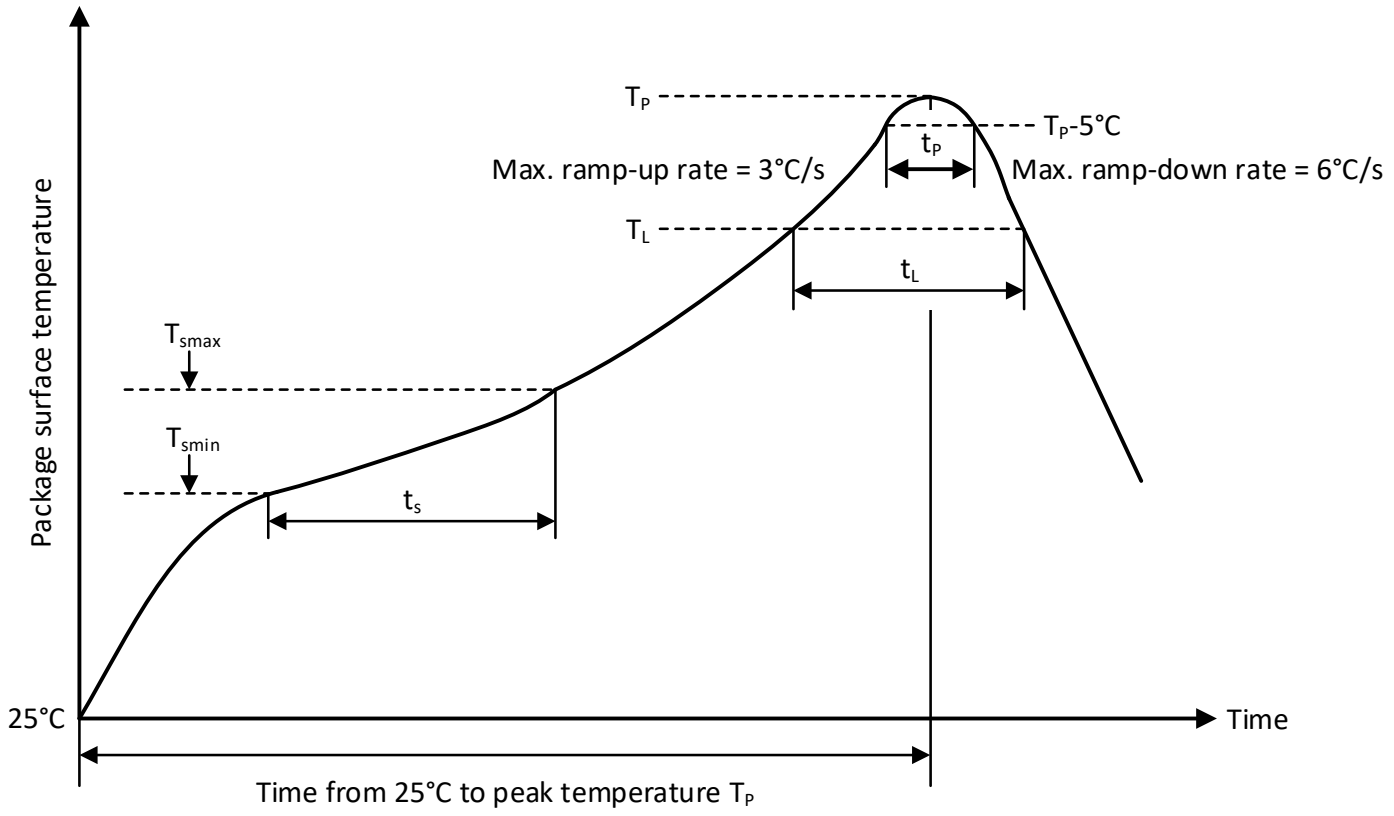


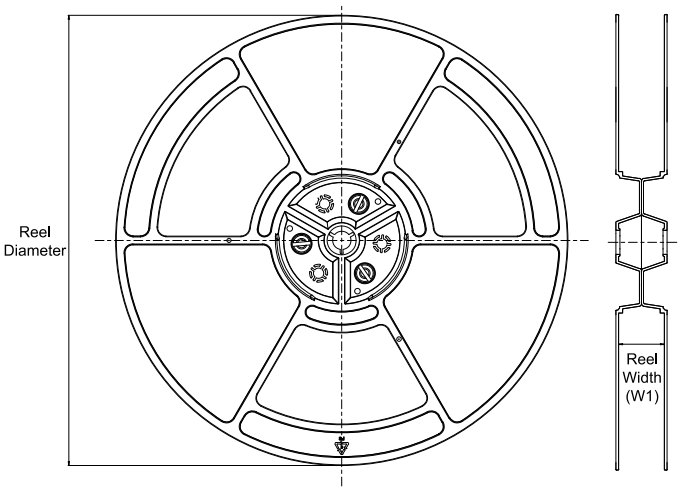
Figure 13-1. Soldering Temperature (reflow) Profile

Table 13-1. Soldering Temperature Parameter

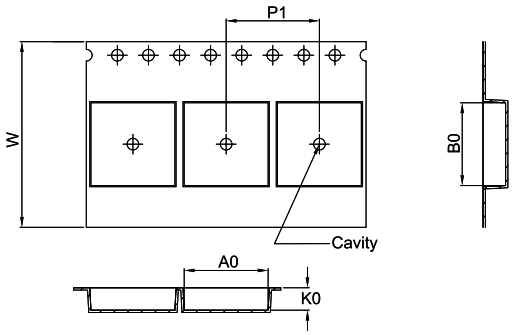
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217°C to Peak)	3°C /second max
Time of Preheat temp(from 150°C to 200°C	60-120 second
Time to be maintained above 217 °C	60-150 second
Peak temperature	260 +5/-0°C
Time within 5°C of actual peak temp	30 second
Ramp-down rate	6 °C /second max.
Time from 25 °C to peak temp	8 minutes max

14. Tape and Reel Information

REEL DIMENSIONS

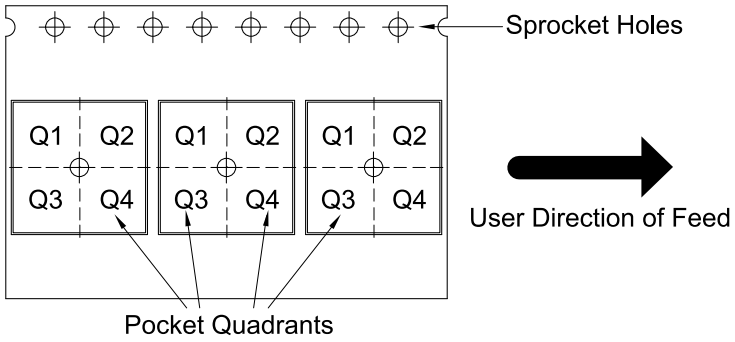


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF1169DT-Q1	DFN	DT	20	3000	330	12.4	3.30	4.80	1.10	8.00	12.00	Q1
CA-IF1169FDT-Q1	DFN	DT	20	3000	330	12.4	3.30	4.80	1.10	8.00	12.00	Q1
CA-IF1169VDT-Q1	DFN	DT	20	3000	330	12.4	3.30	4.80	1.10	8.00	12.00	Q1
CA-IF1169VFDT-Q1	DFN	DT	20	3000	330	12.4	3.30	4.80	1.10	8.00	12.00	Q1

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