Reliability Test Report

Product Name: CA-IS322X

Report Version: V1.2

Prepared by	Reviewed by	Approved by
邵晓梅	刘和芳	陈亮

Contents

1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on JEDEC JESD47. CA-IS322X series chips are packaged with the same wafer. The differences between part numbers are the package and bonding diagram. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family.

2. Part Number List

Package Type	**Part Number**
SOIC16-WB(W)	CA-IS3221AW/CA-IS3221BW/CA-IS3221CW/ CA-IS3222AW/ CA-IS3222BW/CA-IS3222CW
SOIC14-WB(K)	CA-IS3221AK/CA-IS3221BK/CA-IS3221CK/ CA-IS3222AK/ CA-IS3222BK/CA-IS3222CK
SOIC16-NB(N)	CA-IS3221AN/CA-IS3221BN
LGA13(A)	CA-IS3221AA/ CA-IS3221BA

Note: JEDEC specification is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs.

3. Product Information

3.1. Wafer Information

Wafer	SHENNONG, NVWA
Fab Process	18BCD

3.2. Package Information

Assembly site	UNIMOS	UNIMOS	JCET-D8	JCET-D3
FT site	UNIMOS	UNIMOS	JCET-D8	JCET-D3
Package	SOIC16-WB(W)	SOIC14-WB(K)	SOIC16-NB(N)	LGA13(A)
Lead frame	Cu	Cu	Cu	Cu
Bond wire	25um Au	25um Au	25um AuPdCu	25um AuPdCu
MSL level	MSL3	MSL3	MSL3	MSL3

4. Reliability Qualification Plan

4.1. Device Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
Electrical Parameter Assessment	JESD86	ED	Per Datasheet	Per Datasheet
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	$T_J \geq 125°C$ $V_{CC} \geq V_{CC}$ max	1000 hrs/0 Fail
Human Body Model ESD	JS-001	ESD-HBM	$T_A = 25°C$	Classification
Charged Device Model ESD	JS-002	ESD-CDM	$T_A = 25°C$	Classification
Latch-Up	JESD78	LU	Class I or Class II	0 Fail

4.2. Nonhermetic Package Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
MSL Preconditioning	JESD22-A113	PC	Per appropriate MSL level per J-STD-020	Electrical Test (optional)
High Temperature Storage	JESD22-A103 & A113	HTSL	150°C, 1000 hrs	1000 hrs/0 Fail
Temperature Humidity Bias	JESD22-A101	THB	85°C, 85% RH, V_{CC} max	1000 hrs/0 Fail
Highly Accelerated Temperature and Humidity Stress	JESD22-A110	HAST	130°C/110°C, 85% RH, 33.3/17.7 psia, V_{cc1}= 18V, V_{cc2}= 25V	96/264 hrs/0 Fail
Temperature Cycling	JESD22-A104	TC	-65°C to +150°C	500 cycles/0 Fail
Unbiased Temperature/Humidity	JESD22-A118	uHAST	130°C/110°C, 85% RH, 33.3/17.7 psia	96/264 hrs/0 Fail
Bond Pull Strength	M2011	BPS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Bond Shear	JESD22-B116	BS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Solderability	M2003 JESD22-B102	SD	Characterization	0 Fail

Note: Either HAST or THB may be chosen.

5. Reliability Test Results

5.1. Device Reliability Test Results

Stress	Condition	Duration	Sample Size	Result	Classification
ED	Per Datasheet	/	10*3 lot	Pass	/
HTOL	TA = 135℃, 1000 hrs, V_{cc1}= 18V, V_{cc2}= 30V, input f = 1kHz	1000 hrs	77*3 lot	Pass	/
ESD-HBM	T_A = 25℃	/	3*1 lot	Pass	Class 3A
ESD-CDM	T_A = 25℃	/	3*1 lot	Pass	Class C3
LU	T_A = 25℃	/	3*1 lot	Pass	Class I A

5.2. Package Reliability Test Results

Package Type: SOIC16-WB(W) & SOIC14-WB(K)				
Stress	**Condition**	**Duration**	**Sample size**	**Result**
PC	MSL 3	/	231*3 lot	Pass
HTSL	T_A = 150℃	1000 hrs	45*3 lot	Pass
HAST	130℃/85% RH, 33.3 psia, V_{cc1}= 18V, V_{cc2}= 25V	96 hrs	77*3 lot	Pass
TC	-65°C to +150°C	500 cycles	77*3 lot	Pass
uHAST	130°C/85% RH, 33.3psia	96 hrs	77*3 lot	Pass
BS	JESD22-B116	/	30 bonds/5 ea.	Pass
BPS	M2011	/	30 bonds/5 ea.	Pass
SD	Steam aging 8hrs,245℃ dipping 5S		22 leads*3 lot	Pass
Package Type: SOIC16-NB(N)				
Stress	**Condition**	**Duration**	**Sample size**	**Result**
PC	MSL 3	/	231*3 lot	Pass
HTSL	T_A = 150℃	1000 hrs	45*3 lot	Pass
HAST	130℃/85% RH, 33.3 psia, V_{cc1}= 18V, V_{cc2}= 25V	96 hrs	77*3 lot	Pass
TC	-65°C to +150°C	500 cycles	77*3 lot	Pass
uHAST	130°C/85% RH, 33.3psia	96 hrs	77*3 lot	Pass

BS	JESD22-B116	/	30 bonds/5 ea.	Pass
BPS	M2011	/	30 bonds/5 ea.	Pass
SD	Steam aging 8hrs,245℃ dipping 5S		22 leads*3 lot	Pass
Package Type: LGA13(A)				
Stress	**Condition**	**Duration**	**Sample size**	**Result**
PC	MSL 3	/	231*3 lot	Pass
HTSL	T_A = 150℃	1000 hrs	77*3 lot	Pass
HAST	130℃/85% RH, 33.3psia, V_{cc1}= 18V, V_{cc2}= 25V	96 hrs	77*3 lot	Pass
TC	-65°C to +150°C	500 cycles	77*3 lot	Pass
uHAST	130°C/85% RH, 33.3psia	96 hrs	77*3 lot	Pass
BS	JESD22-B116	/	30 bonds/5 ea.	Pass
BPS	M2011	/	30 bonds/5 ea.	Pass
SD	Steam aging 8hrs,245℃ dipping 5S		22 leads*3 lot	Pass

Note:

1. Package reliability test of SOIC14-WB(K) may be referred to SOIC16-WB(W).
2. Package reliability test of SOIC16-NB(N) comes from 1 lot qualification of CA-IS3221AN and 2 lot generic data of the same package family.
3. Package reliability test of LGA13(A) comes from 1 lot qualification of CA-IS3221AA and 2 lot generic data of the same package family.

6. Conclusion

CA-IS322X series products are qualified with JEDEC standards.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

License to customers to use the information is limited to the development of applications using the device. Apart from above, the information shall not be reproduced or displayed, and Chipanalog shall not be liable for any claims, compensation, costs, losses or liabilities arising out of the use of the information.

Trademarks

Chipanalog Inc.®、Chipanalog® are trademarks of Chipanalog.

Revision History

Revision	Change Log	Date
V1.0	Initial release	Jun. 2023
V1.1	Add SOIC16-NB(N) reliability results	Nov. 2023
V1.2	Add LGA13(A) package reliability results	Oct. 2025