CA-IF4905 3V to 5.5V Half-Duplex RS-485 Transceiver with ±30kV ESD Rating, ±65V Fault Protection and ±40V CMR

1 Key Features

- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- Data Rate
  - CA-IF4905S: Low EMI 500kbps
  - CA-IF4905M: Low EMI 2Mbps
- 3V to 5.5V Supply Voltage
- Driver with Current Limiter and Thermal Shutdown Protection
- Bus Pins ESD Protection
  - ±30kV HBM ESD
  - ±6kV IEC 61000-4-2 Contact Discharge
- 1/8 Unit Load (Up to 256 Bus Nodes)
- Open, Short and Idle Bus Failsafe Protection
- Hot Plug-in Protection
- Extended Industrial Temperature Range: –40°C to 125°C
- ±65V Fault Protection on Bus Pins
- ±40V Common Mode Range on Bus Pins
- Low Standby Current: <30μA
- Standard SOIC8 Narrow Body and Small MSOP8 Package

2 Applications

- HVAC
- Home and Building Automation
- Motion Controllers
- Industrial Automation
- Elevator Control
- Video Surveillance
- Power Grid Infrastructure

3 Description

The CA-IF4905 is the high-performance half-duplex RS-485 transceiver which could be used in harsh industrial and home-appliance environments. The bus pins could withstand high-level ESD events to protect internal circuit without damage.

This device has ±65V fault protection on bus pins, and the common-mode range (CMR) could be extended to ±40V when V_{CC} ranges from 4.5V to 5.5V, which is suitable for long-cable communication applications. Each device contains one driver and one receiver, supporting the power supply range from 3V to 5.5V.

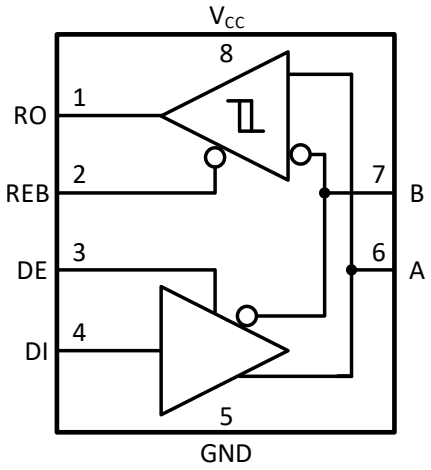
The CA-IF4905 features slew-rate-limited driver for low EMI and date rates up to 2Mbps. This device integrates failsafe circuit to guarantee a logical high on the receiver output when the bus inputs are open, short or on idle state. This device features a 1/8 unit load input impedance, allowing up to 256 transceivers on a bus.

The CA-IF4905 devices are packaged in narrow body, 8-pin SOIC or small MSOP8 packages and specified over ambient free-air temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IF4905S	SOIC8 (S)	3.90mm × 4.90mm
CA-IF4905M	MSOP8 (M)	3.00mm × 3.00mm

Simplified Schematic



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Full/Half-Duplex	Date Rate (Mbps)	Package
CA-IF4905S	Half-Duplex	0.5	SOIC8 (S)
CA-IF4905M	Half-Duplex	2	MSOP8 (M)

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5 Revision History

Revision	Description	Date	Page
Version 1.00	NA	2024.06.30	NA
Version 1.01	Add new part number: CA-IF4905M	2025.06.11	1, 5, 17, 19
Version 1.02	Add timing characteristics of CA-IF4905M Update tape and reel information of CA-IF4905S	2025.08.22	1, 5, 7 19

6 Pin Descriptions and Functions

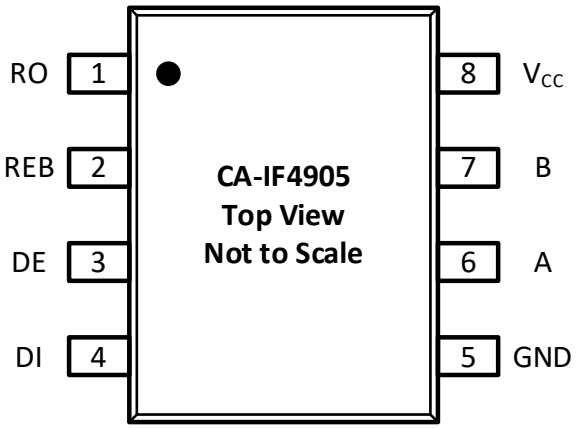


Figure 6-1 CA-IF4905 Pin Configuration

Table 6-1 CA-IF4905 Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
RO	1	Digital Output	Receiver data output.
REB	2	Digital Input	Receiver enable control, pulled up internally: 1. When REB is low, receiver is enabled; 2. When REB is high or open, receiver is disabled.
DE	3	Digital Input	Driver enable control, pulled down internally: 1. When DE is high, driver is enabled; 2. When DE is low or open, driver is disabled.
DI	4	Digital Input	Driver data input, pulled up internally.
GND	5	Ground	Ground.
A	6	Bus Input/Output	Noninverting driver output/receiver input.
B	7	Bus Input/Output	Inverting driver output/receiver input.
V_{CC}	8	Power	Power supply input, bypass V_{CC} to GND with at least 0.1μF capacitors as close as possible to the device.

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply voltage[2]	–0.5	7	V
V_{IO}	Bus voltage of A and B[2]	–65	65	V
V_{IO}	Input logical voltage of DI, DE and REB	–0.3	V_{CC} + 0.3[3]	V
V_{IO}	Output logical voltage of RO	–0.3	V_{CC} + 0.3[3]	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the ground terminal and are peak voltage values.
3. Maximum voltage must not exceed 7V.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pins (A, B) to GND	±30	kV
		All other pins	±4	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		±2	
	Contact discharge, per IEC 61000-4-2		±6	kV

7.3 Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, with respect to GND		3.0	5.0	5.5	V
V_{IN}	Bus input voltage		–40		40	V
V_{IH}	High-level input voltage of DI, DE and REB		2.0		V_{CC}	V
V_{IL}	Low-level input voltage of DI, DE and REB		0		0.8	V
R_L	Differential load resistance		54			Ω
$1/t_{UI}$	Data Rate	CA-IF4905S			0.5	Mbps
		CA-IF4905M			2	
T_A	Ambient Temperature		–40		125	°C
T_J	Junction Temperature		–40		150	°C

7.4 Thermal Information

THERMAL METRIC		PACKAGE		UNIT
		SOIC8 (S)	MSOP8 (M)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	160	°C/W

7.5 Electrical Characteristics

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{CC} = 5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\|V_{OD}\|$	Differential output voltage	R_L = 60Ω, –40V ≤ V_{test} ≤ 40V, see Figure 8-1		1.2	2.8		V
		R_L = 60Ω, –40V ≤ V_{test} ≤ 40V, 4.5V ≤ Vcc ≤ 5.5V, see Figure 8-1		2	2.8		V
		R_L = 100Ω, C_L = 50pF, see Figure 8-2		1.7	3.5		V
		R_L = 54Ω, C_L = 50pF, see Figure 8-2		1.2	2.8		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential-output voltage	R_L = 100Ω or 54Ω, C_L = 50pF, see Figure 8-2		–200		200	mV
V_{OC}	Common-mode output voltage			1		3.2	V
$\Delta V_{OC(SS)}$	Change in magnitude of common-mode output voltage			–100		100	mV
I_{OSD}	Driver short-circuit output current	DE = V_{CC}, –65V ≤ V_O ≤ 65V[1], or A shorted to B		–200		200	mA
Receiver							
I_I	Bus input current	DE = 0V, V_{CC} = 0V or 5.5V	V_I = 12V			125	μA
			V_I = –7V	–100			
			V_I = 40V			410	
			V_I = –40V	–400			
R_I	Bus input resistance	Over V_{CM} range		96			kΩ
V_{CM}	Common mode voltage range	3V ≤ Vcc ≤ 3.6V		–25		25	V
		4.5V ≤ Vcc ≤ 5.5V		–40		40	
V_{TH+}	Positive-going receiver input voltage threshold	Over V_{CM} range				–20	mV
$V_{TH–}$	Negative-going receiver input voltage threshold			–200			mV
V_{HYS}[2]	Receiver differential-input voltage threshold hysteresis, $V_{TH+} – V_{TH–}$				30		mV
V_{OH}	High-level output voltage	I_{OH} = –3mA		V_{CC} – 0.4	V_{CC} – 0.25		V
V_{OL}	Low-level output voltage	I_{OL} = 3mA			0.2	0.4	V
I_{OZR}	High-impedance output current	REB = V_{CC}, V_O = 0V or V_{CC}		–1		1	μA
I_{OSR}	Receiver short-circuit output current	REB = DE = 0V, see Figure 8-3				95	mA
Input Logic (DI, DE, REB)							
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{CC}, after hot-swap protection delay for DE		–10		10	μA
V_{IH}	High-level input voltage			2.0		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.8	V
Supply							
I_{CC}	Quiescent supply current	Both driver and receiver enabled, REB = 0V, DE = V_{CC}, empty load, no switching			2.2	3.5	mA
		Driver enabled and receiver disabled, REB = V_{CC}, DE = V_{CC}, empty load, no switching			2.2	3.5	
		Driver disabled and receiver enabled, REB = 0V, DE = 0V, empty load, no switching			1.4	2.5	
		Both driver and receiver disabled, REB = DI = V_{CC}, DE = 0V, empty load, no switching			10	30	μA
TSD	Thermal shutdown threshold				185		°C
	Thermal shutdown hysteresis				20		°C

NOTE:

1. In the case of high ambient temperature, when pin A or pin B applies a voltage with a high absolute value, overtemperature protection may be triggered. At this time, the driver outputs become high-impedance, and the short-circuit output current would be greatly reduced.
2. Under any specific conditions, V_{TH+} is specified to be at least V_{HYS} higher than $V_{TH–}$.

7.6 Timing Characteristics

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{CC} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CA-IF4905S						
Driver						
t_{DR}, t_{DF}	Differential output rise and fall time	R_L = 54Ω, C_L = 50pF, see Figure 8-4		110	500	ns
t_{DPHL}, t_{DPLH}	Driver propagation delay			170	600	ns
t_{DSKEW}	Driver pulse skew, $\lvert t_{DPHL} - t_{DPLH} \rvert$			5	50	ns
t_{DHZ}, t_{DLZ}	Driver disable time	see Figure 8-5 and Figure 8-6		70	250	ns
t_{DZH}, t_{DZL}	Driver enable time[1]	REB = 0V, see Figure 8-5 and Figure 8-6		180	900	ns
$t_{DZH(SHDN)}$, $t_{DZL(SHDN)}$	Driver enable time (from shutdown mode)	REB = V_{CC}, see Figure 8-5 and Figure 8-6		3.3	8	µs
Receiver						
t_{RPHL}, t_{RPLH}	Receiver propagation delay time	C_L = 15pF[2], see Figure 8-7		145	300	ns
t_{RSKEW}	Receiver pulse skew, $\lvert t_{RPHL} - t_{RPLH} \rvert$			3	30	ns
t_{RHZ}, t_{RLZ}	Receiver disable time	See Figure 8-8		10	80	ns
t_{RZH}, t_{RZL}	Receiver enable time[3]	DE = V_{CC}, see Figure 8-8		10	80	ns
$t_{RZH(SHDN)}$, $t_{RZL(SHDN)}$	Receiver enable time (from shutdown mode)	DE = 0V, see Figure 8-9		3.9	8	µs
CA-IF4905M						
Driver						
t_{DR}, t_{DF}	Differential output rise and fall time	R_L = 54Ω, C_L = 50pF, see Figure 8-4		55	200	ns
t_{DPHL}, t_{DPLH}	Driver propagation delay			80	250	ns
t_{DSKEW}	Driver pulse skew, $\lvert t_{DPHL} - t_{DPLH} \rvert$			1	100	ns
t_{DHZ}, t_{DLZ}	Driver disable time	see Figure 8-5 and Figure 8-6		100	250	ns
t_{DZH}, t_{DZL}	Driver enable time[1]	REB = 0V, see Figure 8-5 and Figure 8-6		100	250	ns
$t_{DZH(SHDN)}$, $t_{DZL(SHDN)}$	Driver enable time (from shutdown mode)	REB = V_{CC}, see Figure 8-5 and Figure 8-6		3.3	8	µs
Receiver						
t_{RPHL}, t_{RPLH}	Receiver propagation delay time	C_L = 15pF[2], see Figure 8-7		140	220	ns
t_{RSKEW}	Receiver pulse skew, $\lvert t_{RPHL} - t_{RPLH} \rvert$			1	30	ns
t_{RHZ}, t_{RLZ}	Receiver disable time	See Figure 8-8		10	80	ns
t_{RZH}, t_{RZL}	Receiver enable time[3]	DE = V_{CC}, see Figure 8-8		10	80	ns
$t_{RZH(SHDN)}$, $t_{RZL(SHDN)}$	Receiver enable time (from shutdown mode)	DE = 0V, see Figure 8-9		3.9	8	µs

NOTE:

1. When DE and REB are shorted together, driver enable time refers to the case when REB = 0V.
2. C_L includes probe and fixture capacitance.
3. When DE and REB are shorted together, receiver enable time refers to the case when DE = V_{CC}.

7.7 Typical Characteristics

All typical specifications are at T_A = 25°C and V_{CC} = 5V (unless otherwise noted).

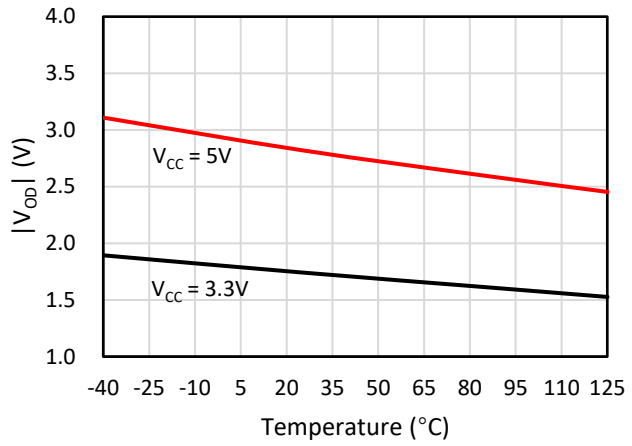


Figure 7-1 Differential Output Voltage vs Temperature @ R_L = 54Ω

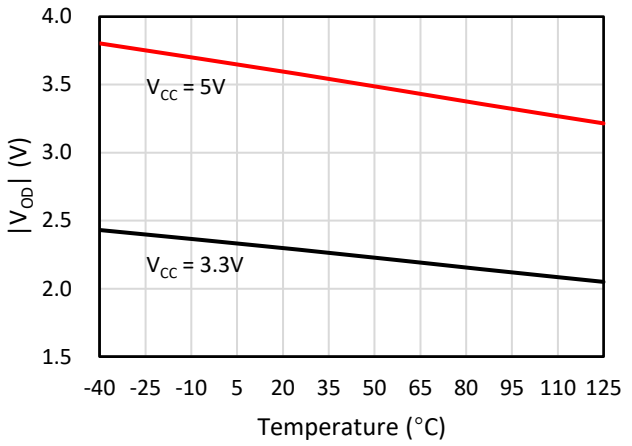


Figure 7-2 Differential Output Voltage vs Temperature @ R_L = 100Ω

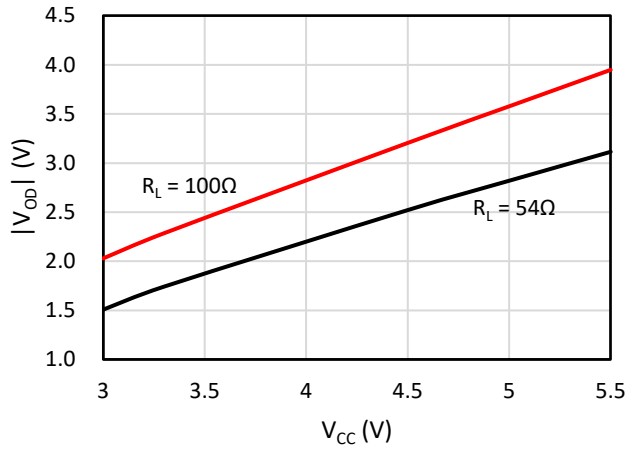


Figure 7-3 Differential Output Voltage vs Supply Voltage

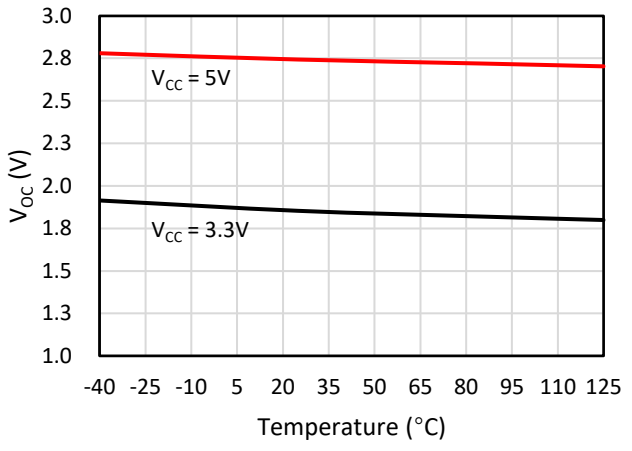


Figure 7-4 Common-Mode Output Voltage vs Temperature

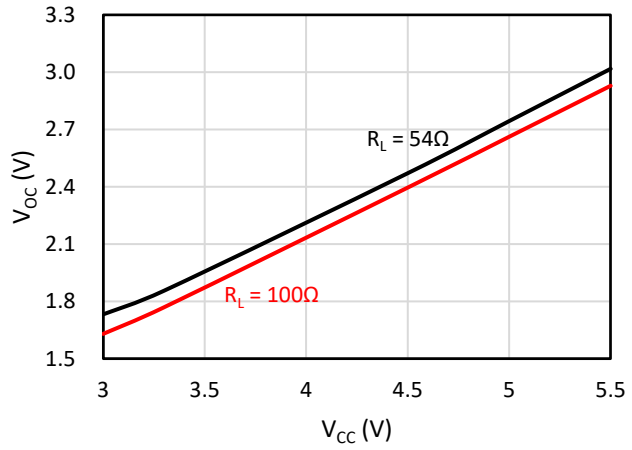


Figure 7-5 Common-Mode Output Voltage vs Supply Voltage

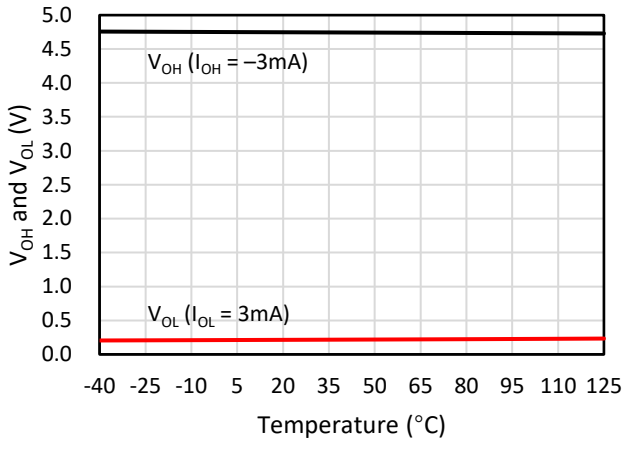


Figure 7-6 High- or Low-Level Output Voltage of RO vs Temperature

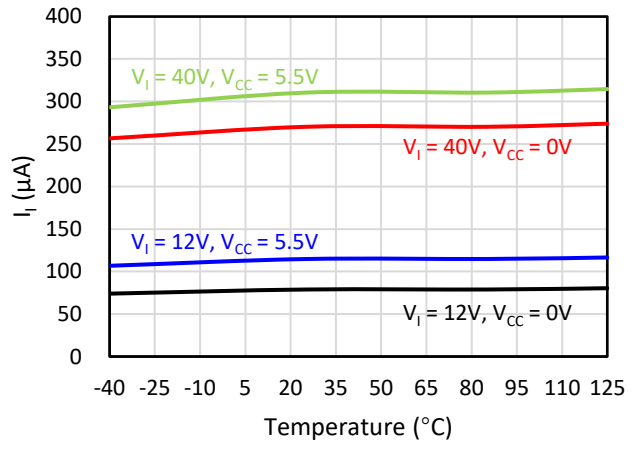


Figure 7-7 Bus Input Current vs Temperature @ V_I = 12V or 40V

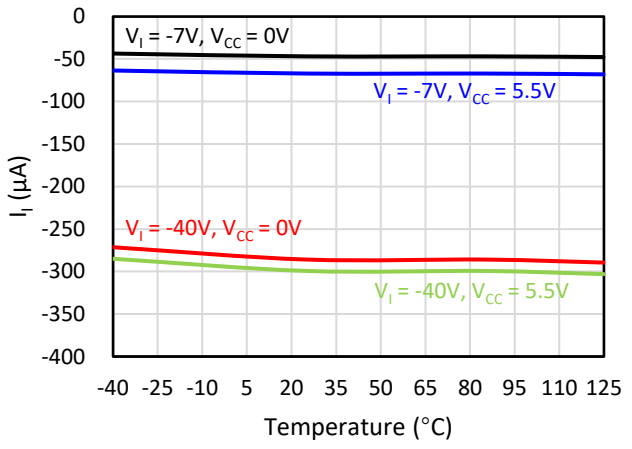


Figure 7-8 Bus Input Current vs Temperature @ V_I = –7V or –40V

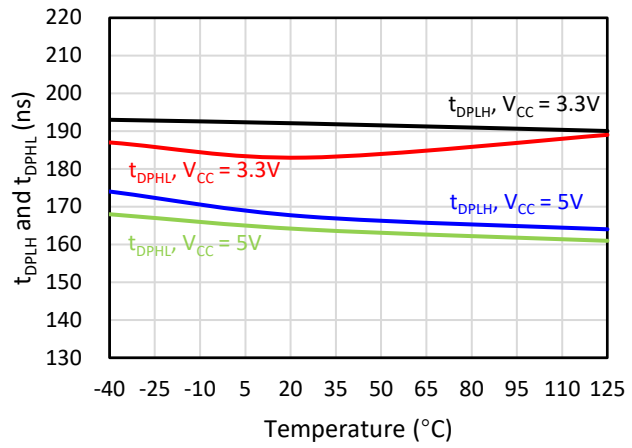


Figure 7-9 Driver Propagation Delay vs Temperature

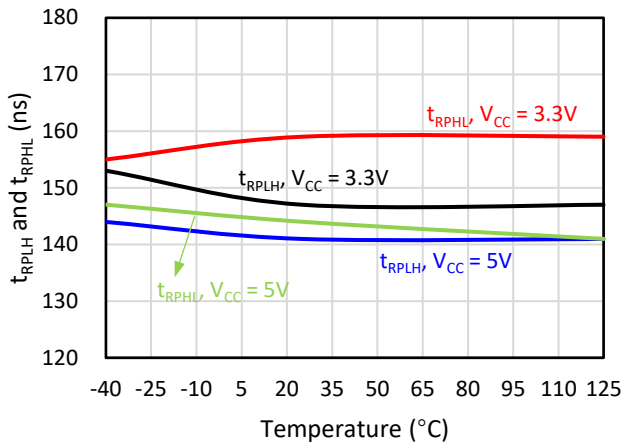


Figure 7-10 Receiver Propagation Delay vs Temperature

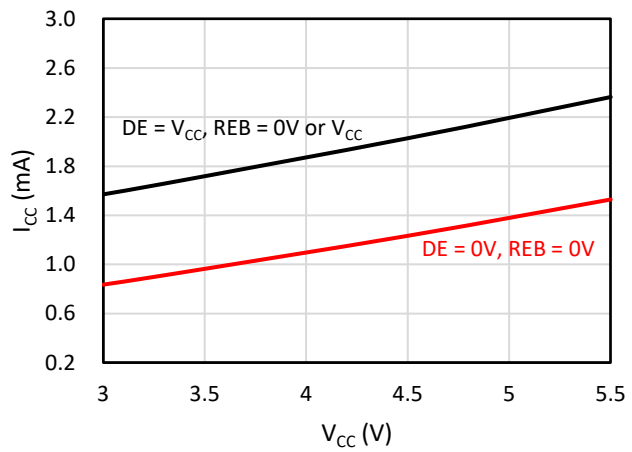


Figure 7-11 Quiescent Supply Current vs Supply Voltage

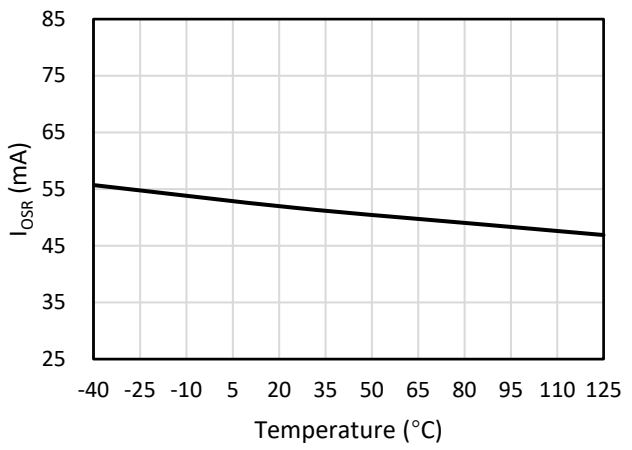


Figure 7-12 Receiver Short-Circuit Output Current vs Temperature

8 Parameter Measurement Information

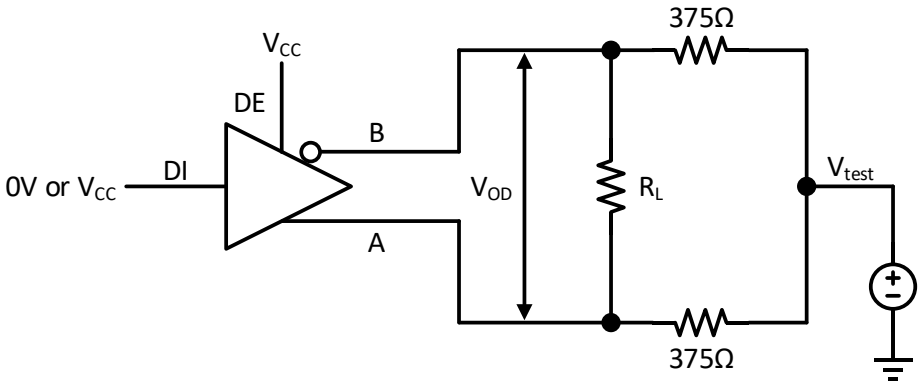


Figure 8-1 Measurement of Driver Differential Output Voltage With Common-Mode Load

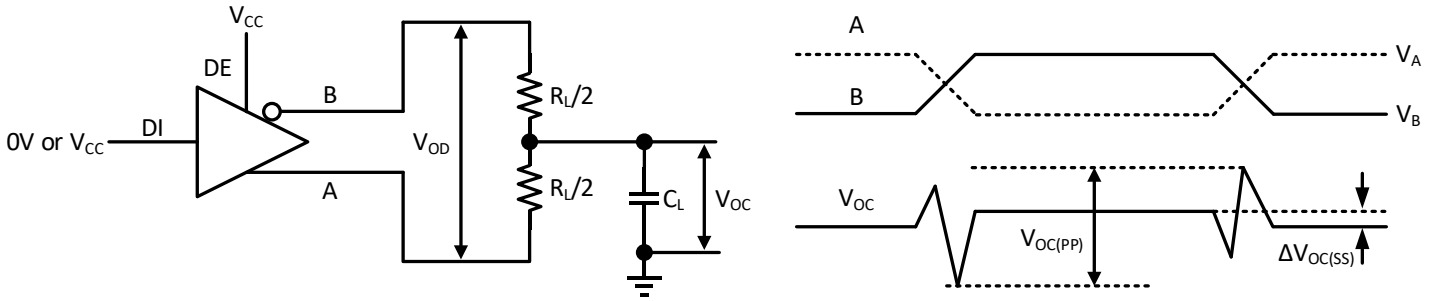


Figure 8-2 Measurement of Driver Differential and Common-Mode Output Voltage With RS-485 Load

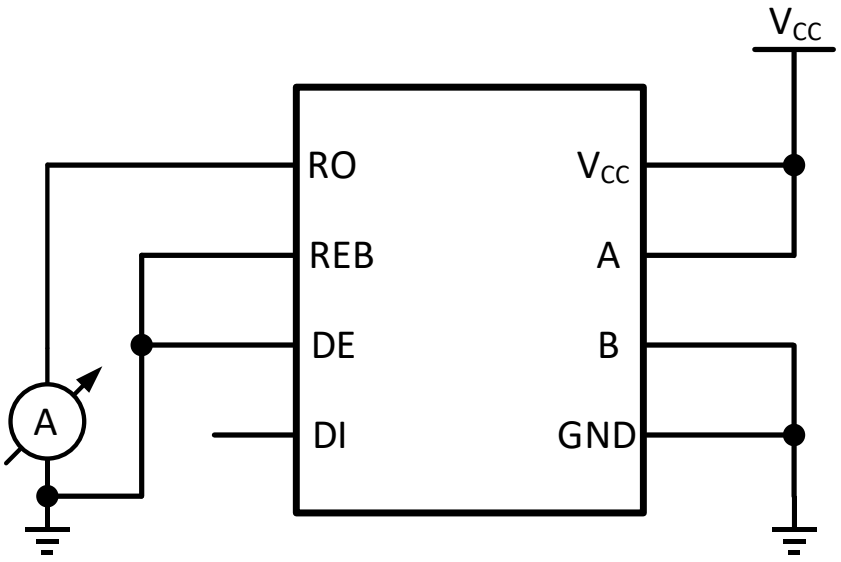


Figure 8-3 Measurement of Receiver Output Short Circuit Current

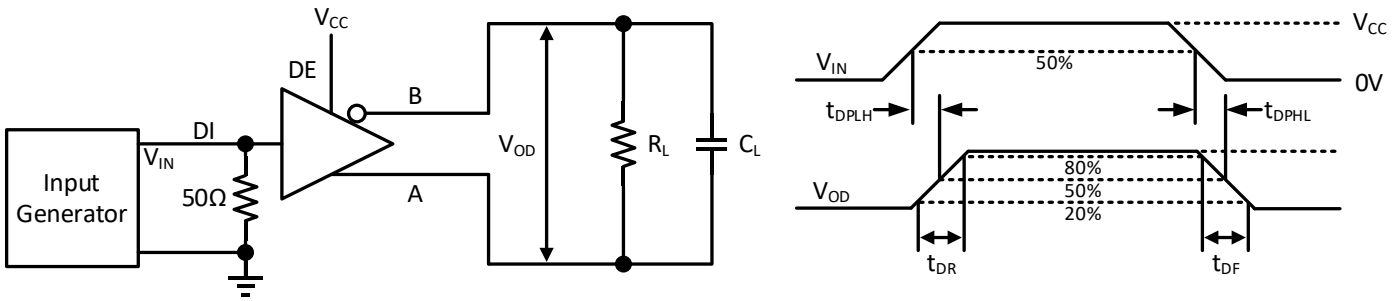


Figure 8-4 Measurement of Driver Output Rise and Fall Time and Propagation Delay

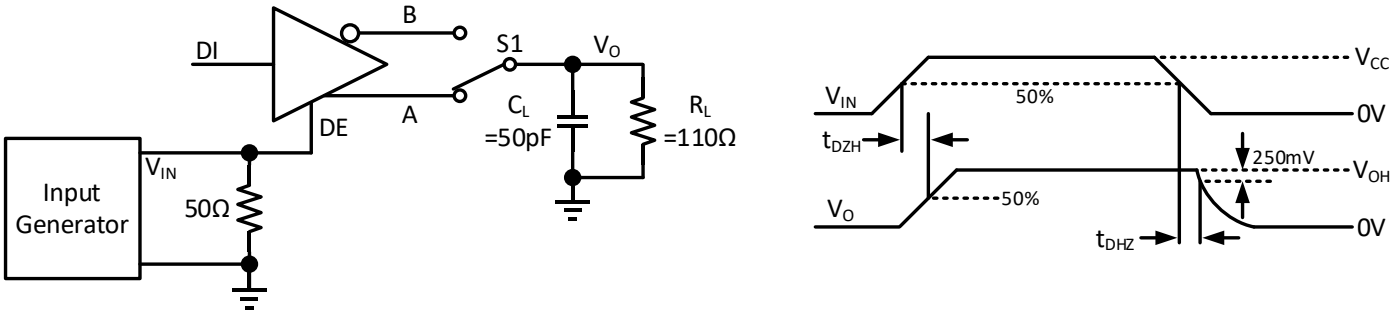


Figure 8-5 Measurement of Driver Enable and Disable Time With Active High Output and Pull-Down Load

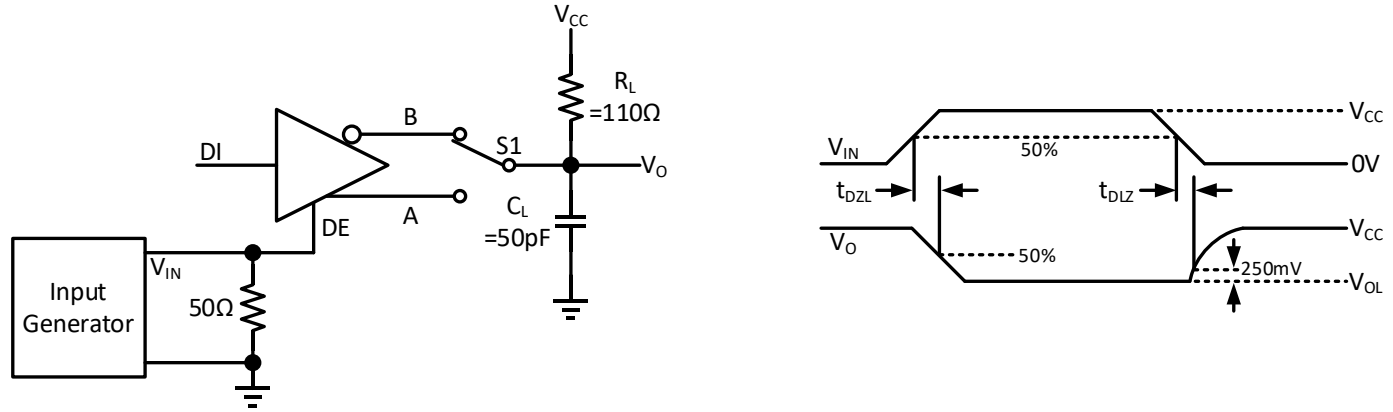


Figure 8-6 Measurement of Driver Enable and Disable Time With Active Low Output and Pull-Up Load

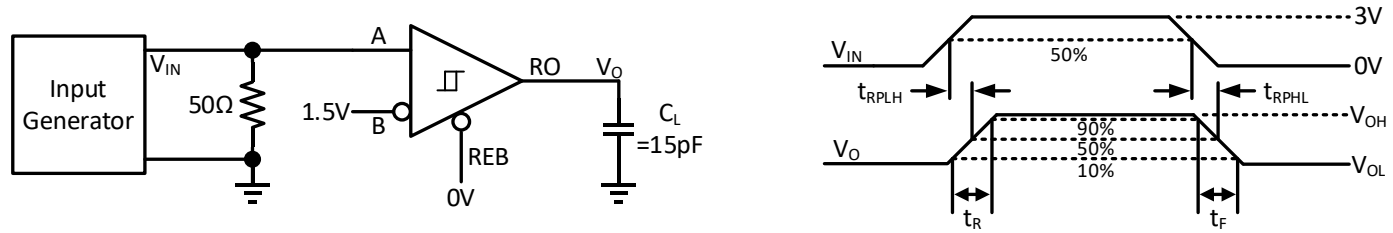


Figure 8-7 Measurement of Receiver Output Rise and Fall Time and Propagation Delay

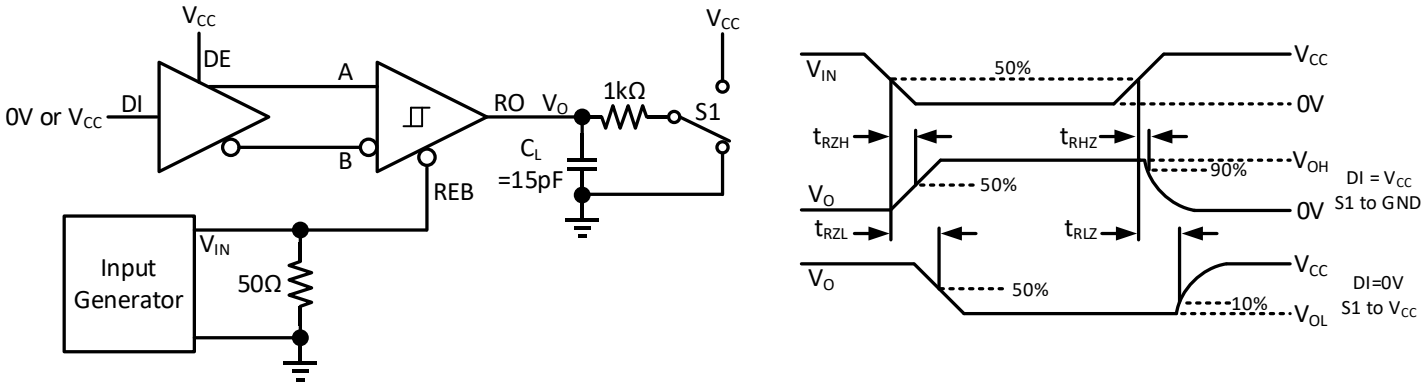


Figure 8-8 Measurement of Receiver Enable/Disable Time With Driver Enabled

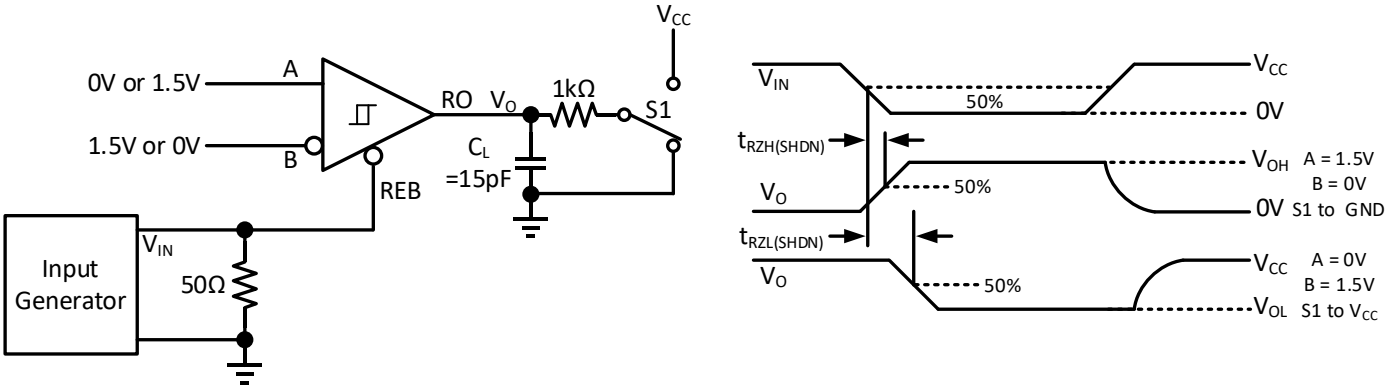


Figure 8-9 Measurement of Receiver Enable Time With Driver Disabled

9 Detailed Description

9.1 Device Feature Description

9.1.1 ±65V fault protection on Bus Pins

The bus pins of transceivers connected to a RS-485 network often experience faults when shorted to voltages that exceed the –7V to 12V input range specified in the EIA/TIA-485 standard. Under such circumstances, ordinary RS-485 transceivers generally require costly external protection devices which can compromise the performance. To reduce system complexity and the requirements of external protection devices, The CA-IF4905 has ±65V fault protection on bus pins with respect to ground whenever this device is under enabled, disabled or power-down mode. When the driver is enabled and the bus pins are short-circuited, the driver would limit the output short-circuit current within a certain range by the built-in current limiter firstly. If the absolute value of the bus pin's fault voltage is large, the device's junction temperature could increase rapidly to trigger the thermal shutdown protection. Once the device's junction temperature rises above the thermal shutdown temperature, the driver would be disabled and the outputs become high-impedance, resulting in the reduction of power consumption and thus avoiding further thermal damage.

9.1.2 ±40V Common-Mode Range

RS-485 standards define the common-mode range as –7V to 12V for the receiver. However, the common-mode range of the CA-IF4905 exceeds the standard with ±40V for both the driver and receiver. This feature was specifically designed for systems where there is a large common-mode voltage present due to either nearby electrically noisy equipment or large ground differences due to earth ground loop. Compared with ordinary RS-485 transceivers, ±40V common-mode range could ensure that the CA-IF4905 communicates correctly in a broader range of applications.

9.1.3 Bus Failsafe Protection

The input threshold of the CA-IF4905's receiver ranges from –20mV to –200mV, which guarantees a logical high on the receiver output when the bus inputs are open, short or on idle state.

9.1.4 Hot Plug-in Protection

Inserting circuit boards into a powered backplane may cause voltage transients on DE and bus input pins that can lead to data errors. For example, upon initial circuit board insertion, the processor undergoes a power-up sequence. During this period, the high-impedance state of the output drivers makes them unable to drive the DE input to a defined logic level. Meanwhile, coupling noise from V_{CC} or GND could cause the input of DE to drift to an indeterminate logic state. The internal hot plug-in protection circuit on DE pin could avoid unwanted driver activation during hot-swap situations. The basic working principle of this circuit is to strongly pull down the input of DE at least 15μs when detecting the rising from low voltage of the power supply. After the power-up sequence, this hot plug-in protection circuit is bypassed and DE could receive the normal control signal from outside.

9.1.5 Thermal Shutdown Protection

The CA-IF4905 integrates thermal shutdown protection circuit. When the junction temperature rises above 185°C (typical value), the output of driver is disabled and the output of RO is high-impedance. When the junction temperature falls below 165°C (typical value), the output of both driver and receiver is re-enabled.

9.2 Device Function Mode

9.2.1 Driver

When the enable pin DE of driver is logical high, the differential outputs of A and B follow with the data input DI, which is shown in Table 9-1.

When DE is logical low or open, the driver is disabled, the outputs of A and B are high-impedance and are irrelevant to the state at DI pin. DI pin is weakly pulled up to V_{CC} internally, the output of A is high while B is low when driver is enabled and DI's input is open.

Table 9-1 Truth Table of Driver[1]

INPUT	ENABLE	OUTPUT		FUNCTION
DI[2]	DE[3]	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	High-Z	High-Z	Driver disabled
X	Open	High-Z	High-Z	Driver disabled by default
Open	H	H	L	Actively drive bus high by default

NOTE:
1. H = high level, L = low level, X = irrelevant, High-Z = high impedance.
2. DI is weakly pulled up to V_{CC} internally.
3. DE is weakly pulled down to GND internally.

9.2.2 Receiver

When the enable pin REB of receiver is logical low, receiver is enabled. The truth table of receiver is shown in Table 9-2.

When the bus differential input voltage V_{ID} is greater than or equal to –20mV, receiver output RO is logical high. When V_{ID} is less than or equal to –200mV, receiver output RO is logical low. When V_{ID} is between –20mV and –200mV, receiver output RO is indeterminate.

When REB is logical high or open, the receiver output RO is high-impedance and is irrelevant to the magnitude and polarity of V_{ID}.

When the bus inputs are open, short or on idle state, a failsafe logic high output at RO pin is achieved, avoiding indeterminate state which may result in system communication errors.

Table 9-2 Truth Table of Receiver[1]

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	REB[2]	RO	
$V_{ID} \geq -20mV$	L	H	Output valid high
$-200mV < V_{ID} < -20mV$	L	?	Indeterminate bus state
$V_{ID} \leq -200mV$	L	L	Output valid low
X	H	High-Z	Receiver disabled
X	Open	High-Z	Receiver disabled by default
Open-circuit bus	L	H	Failsafe output high
Short-circuit bus	L	H	Failsafe output high
Idle (terminated) bus	L	H	Failsafe output high

NOTE:
1. H = high level, L = low level, X = irrelevant, High-Z = high impedance, Open = no connection, ? = indeterminate.
2. REB is weakly pulled up to V_{CC} internally.

10 Application and Implementation

10.1 Typical Application

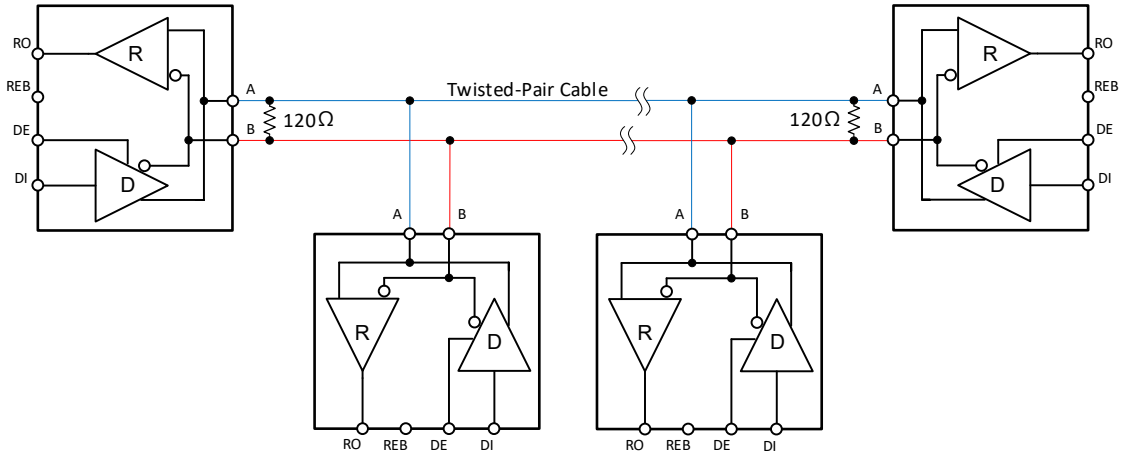


Figure 10-1 Typical RS-485 Network

The typical RS-485 network consists of multiple transceivers connecting in parallel to a bus cable. To eliminate the line reflection, both ends of the cable terminate a termination resistor R_T which should be matched to the characteristic impedance Z_O of the cable. At the same time, please keep the stub lengths off the main line as short as possible. This parallel termination method could achieve higher data rates over longer cable length. The typical RS-485 network utilizing CA-IF4905 is shown in Figure 10-1.

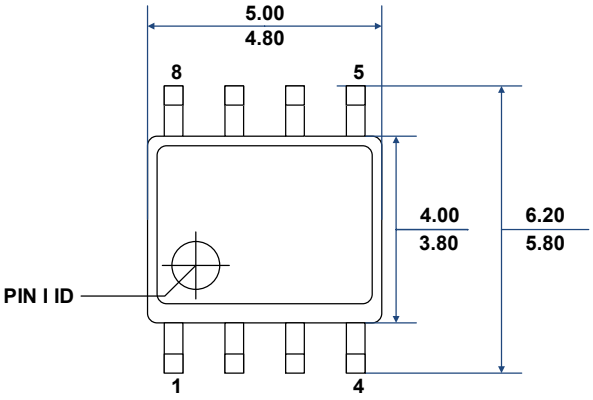
10.2 Power Supply Recommendation

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with at least 0.1μF ceramic capacitors located as close as possible to the supply pins. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes. At the same time, please keep the voltage in V_{CC} pin with respect to GND pin is below 5.5V.

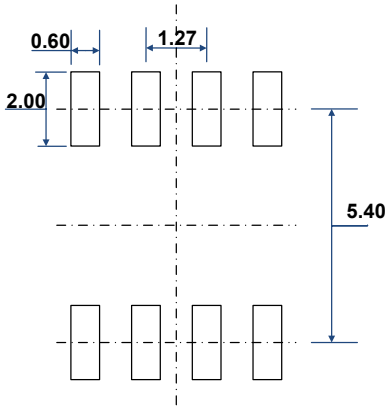
11 Package Information

11.1 SOIC8 (S) Package

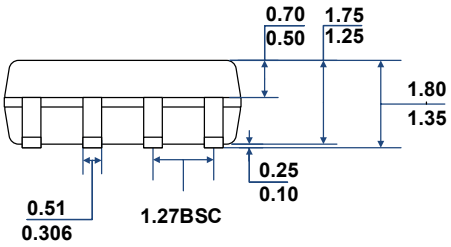
The values for the dimensions are shown in millimeters.



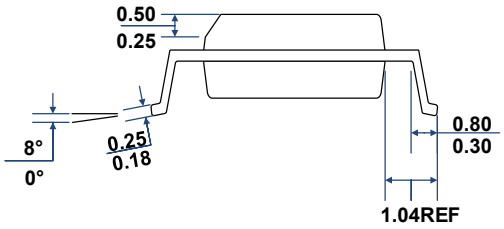
TOP VIEW



RECOMMENDED LAND PATTERN



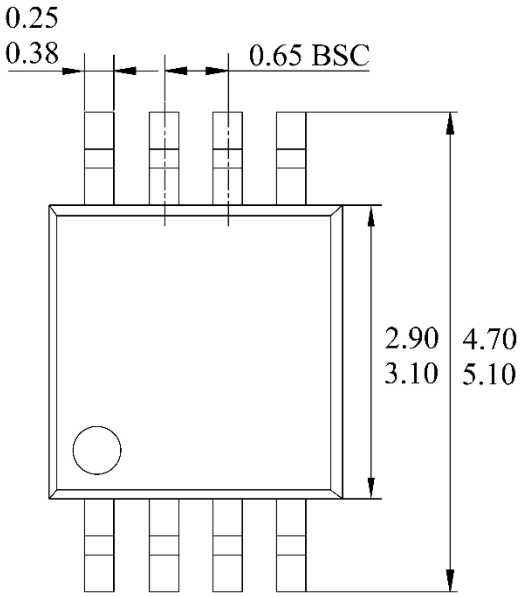
FRONT VIEW



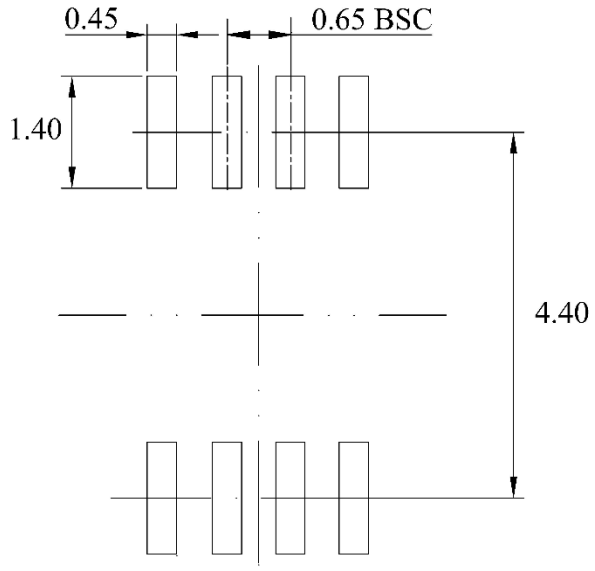
LEFT-SIDE VIEW

11.2 MSOP8 (M) Package

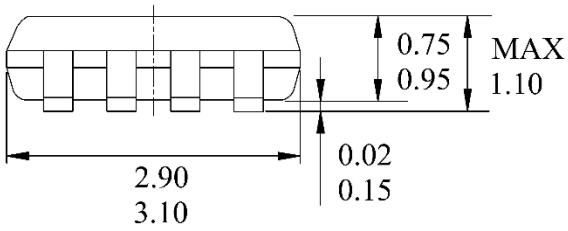
The values for the dimensions are shown in millimeters.



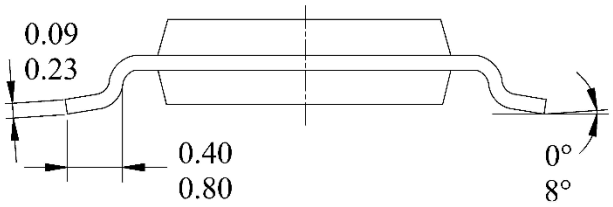
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

12 Soldering Information

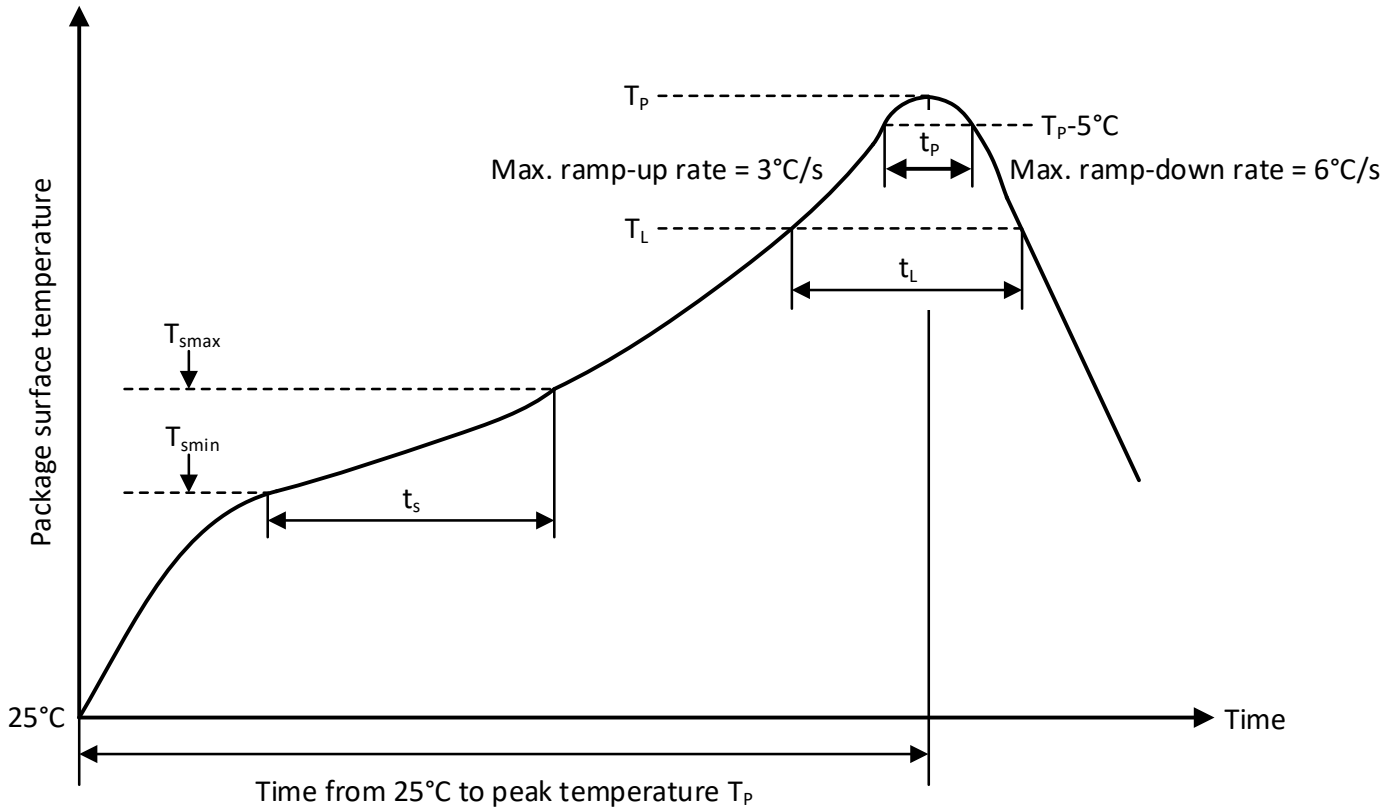


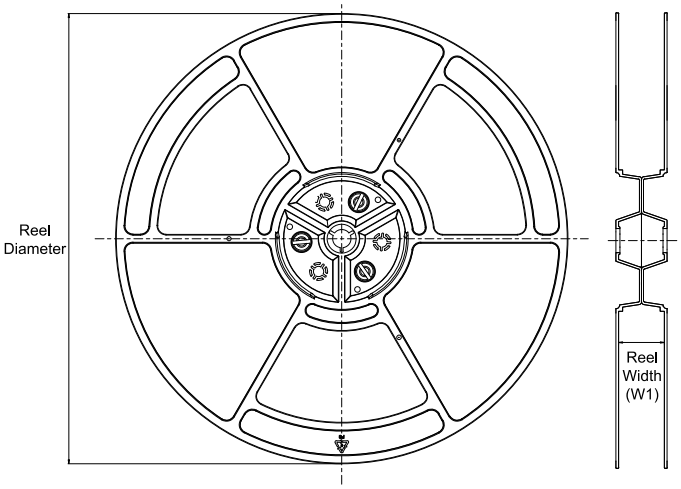
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

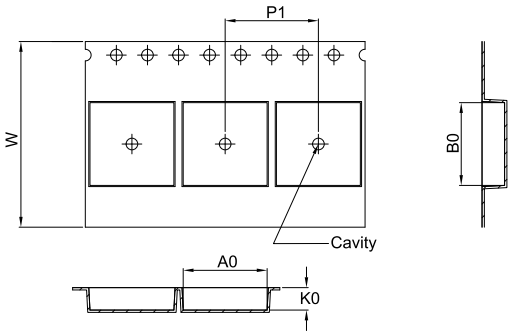
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

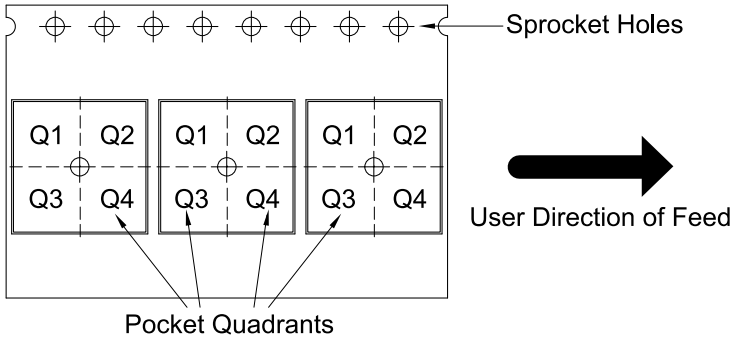


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF4905S	SOIC8	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IF4905M	MSOP8	M	8	5000	330	12.4	5.20	3.30	1.50	8.00	12.00	Q1

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