



AEC-Q100 Qualification Report

Product Series: CA-IF1145FXX-Q1

Report Version: V 1.1

Reference Doc.: AEC-Q100-REV-H

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1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on AEC-Q100.

2. Part Number List

Package Type	Part Number
SOIC14(NF)	CA-IF1145FNF-Q1
SOIC14(DF)	CA-IF1145FDF-Q1

Note: AECQ-100 provides the guideline for the use of generic data to accelerate and streamline the qualification process. Products sharing the same major product, process and materials elements may be categorized in a product qualification family.

3. Production Information

3.1. Wafer information

Fab site	SMIC
Wafer	LIBRA
Fab Process	18BCDA

3.2. Package information

Assembly site	JCET-D8	JCET-D3
FT site	JCET-D8	JCET-D3
Package	SOIC14(NF)	DFN14(DF)
Lead Frame	Cu	Cu
Bond wire	20um Au	20um Au
MSL level	MSL1	MSL1
Operation Temp.	Grade 1(-40°C - 125°C)	Grade 1(-40°C - 125°C)

4. Reliability Qualification Plan

Test Group A-Accelerated Environment Stress Tests					
Group	Item	Refer.	Test condition	QTY	Remark
A1	PC	J-STD-020 JESD22-A113	Test @ Rm, SMD only, Moisture Preconditioning before THB/BHAST, AC/UHAST, TC, and PTC stress, MSL = 1, Peak Reflow Temp = 260°C	231 pcs *3 lots	
A2	BHAST	JESD22-A110	BHAST: 130°C, 85% RH, V _{cc} =28V, 96 hrs (Test @ Rm/Hot)	77 pcs *3 lots	
A3	UHAST	JESD22-A101	UHAST: 130°C, 85% RH, 96 hrs (Test @ Rm)	77 pcs *3 lots	
A4	TC	JESD22-A104	-65°C-150°C, 500 cycles (Test @ Hot)	77 pcs *3 lots	
A5	PTC	JESD22-A105	-40°C-125°C, 1000 cycles (Test @ Rm/Hot)	NA	
A6	HTSL	JESD22-A103	T _a = 150°C, 1000 hrs (Test @ Rm/Hot)	45 pcs *1 lot	
Test Group B-Accelerated Lifetime Simulation Tests					
Group	Item	Refer.	Test condition	QTY	Remark
B1	HTOL	JESD22-A108	T _a = 125°C, V _{cc} = 28V, 1000 hrs (Test @ Rm/Cold/Hot)	77 pcs*3 lots	
B2	ELFR	AEC-Q100-008	T _a = 125°C, V _{cc} = 28V, 48 hrs (Test @ Rm/Hot)	800 pcs*3 lots	
B3	EDR	AEC-Q100-005	Test @ Rm/Hot	NA	No memory device
Group C-Package Assembly Integrity Tests					
Group	Item	Refer.	Test condition	QTY	Remark
C1	WBS	AEC-Q100-001 AEC-Q003	Cpk > 1.67, Each bonder used, T0 samples	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	Cpk > 1.67, Each bonder used, T0 samples	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	0 fails, Each bonder used, post-TC samples	30 bonds from 5 pcs	
C3	SD	JESD22-B102 JSTD-002D	> 95% coverage, 8hr steam aging prior to testing	15 pcs*1 lot	
C4	PD	JESD22-B100 JESD22-B108 AEC-Q003	Cpk > 1.67	10 pcs*3 lots	
C5	SBS	AEC-Q100-010 AEC-Q003	Cpk > 1.67, 5 balls from min. of 10 devices	NA	No solder ball

C6	LI	JESD22 B105	10 leads from each of 5 devices	NA	No need for SMD device
Test Group D-Die Fabrication Reliability Tests					
Group	Item	Refer.	Test condition	QTY	Remark
D1	EM	JESD61	---	---	Done by Fab
D2	TDDDB	JESD35	---	---	Done by Fab
D3	HCI	JESD60 & 28	---	---	Done by Fab
D4	NBTI	JESD90	---	---	Done by Fab
D5	SM	JESD61, 87, & 202	---	---	Done by Fab
Group E-Electrical Verification Tests					
Group	Item	Refer.	Test condition	QTY	Remark
E1	TEST	per datasheet	Pre and Post Stress Electrical Test	all	
E2	HBM	AEC Q100-002	$\pm 500V$, $\pm 1KV$, $\pm 2KV$ (Test @ Rm/Hot)	3 pcs*1 lot	
E3	CDM	AEC-Q100-011	$\pm 250V$, $\pm 500V$, $\pm 750V$, $\pm 2KV$ (Test @ Rm/Hot)	3 pcs*1 lot	
E4	LU	AEC-Q100-004	125°C, I-trigger $\pm 200mA$ (Test @ Rm/Hot)	6 pcs*1 lot	
E9	EMC	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	
E10	SC	AEC-Q100-012	/	NA	Not 12V smart power device
E11	SER	JESD89-1/-2/-3	/	NA	No memory device
E12	LF	AEC-Q005	/	2 pcs*3 lots	
Group S-Special Requirement Tests					
S1	BLR-Bending	JESD22-B113	Align with customer	NA	
S2	BLR-Drop	JESD22-B11	Align with customer	NA	
S3	BLR-TC	IPC-9701	Refer test requirement	NA	
S4	BLR-Vibration	JESD22-B103	Refer test requirement	NA	

Note: Group E5, E6, E7 and Group F are not reliability related items. Group G are not applicable to non-hermetic packaged devices.

5. Reliability Test Results

Test Group A–Accelerated Environment Stress Test						
Group	Item	Test Condition	QTY	Lot NO. JCET-D8	Lot NO. JCET-D3	Result
A1	PC	Test @ Rm, SMD only, Moisture Preconditioning before BHAST, UHAST, TC stress, MSL = 1, Peak Reflow Temp = 260°C	231 pcs*3 lots	2435A	2511B	Pass
				2436A	2512B	Pass
				2437A	2513B	Pass
A2	BHAST	130°C, 85% RH, 96 hrs, V _{cc} = 28V	77 pcs*3 lots	2435A	2511B	Pass
				2436A	2512B	Pass
				2437A	2513B	Pass
A3	UHAST	130°C, 85% RH, 96 hrs	77 pcs*3 lots	2435A	2511B	Pass
				2436A	2512B	Pass
				2437A	2513B	Pass
A4	TC	-65°C-150°C, 500 cycles	77 pcs*3 lots	2435A	2511B	Pass
				2436A	2512B	Pass
				2437A	2513B	Pass
A6	HTSL	T _a = 150°C, 1000 hrs	45 pcs*1 lot	2437A	2511B	Pass
Test Group B–Accelerated Lifetime Simulation Tests						
Group	Item	Test Condition	QTY	Lot NO.		Result
B1	HTOL	T _a = 125°C, 1000 hrs, V _{cc} = 28V, input f = 100kHz, VIH=5.5V, VIL=0V;	77 pcs*3 lots	2428A		Pass
				2436A		Pass
				2437A		Pass
B2	ELFR	T _a = 125°C, 48 hrs, V _{cc} = 28V, input f = 100kHz, VIH=5.5V, VIL=0V;	800 pcs*3 lots	2435A		Pass
				2436A		Pass
				2437A		Pass
Group C–Package Assembly Integrity Tests						
Group	Item	Test Condition	QTY	Lot NO.		Result
C1	WBS	Cpk > 1.67, Each bonder used, T0 samples	30 bonds from 5 pcs	2435A	2511B	Pass
C2	WBP	Cpk > 1.67, each bonder used, T0 samples	30 bonds from 5 pcs	2435A	2511B	Pass
C2	WBP	0 fails, Each bonder used, post-TC500 samples	30 bonds from 5 pcs	2435A	2511B	Pass
C3	SD	>95% coverage, 8 hrs steam aging prior to testing	15 pcs*1 lot	2435A	2511B	Pass
C4	PD	Cpk > 1.67	10 pcs*3 lots	2435A	2511B	Pass
				2436A	2512B	Pass
				2437A	2513B	Pass

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TEST GROUP D–Die Fabrication Reliability Tests					
Group	Item	Test Condition	ADDITIONAL REQUIREMENTS		
D1	EM	---	The Die Fabrication Reliability Tests are carried out by every fabrication site. The data, test method, calculations and internal criteria are available to the customer upon request.		
D2	TDDDB	---			
D3	HCI	---			
D4	NBTI	---			
D5	SM	---			
Group E-Electrical Verification Tests					
Group	Item	Test Condition	QTY	Lot NO.	Result
E1	TEST	Pre and Post Stress Electrical Test	all	all	Pass
E2	HBM	± 500V, ± 1KV, ± 2KV (Test @ Rm/Hot)	3 pcs*1 lot	2501A	Class 2
E3	CDM	± 250V, ± 500V, ± 750V, ± 2KV (Test @ Rm/Hot)	3 pcs*1 lot	2501A	Class C3
E4	LU	125°C, I-trigger ±200mA(Test @ Rm/Hot)t	3 pcs*1 lot	2501A	Class II A
E9	EMC	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	2501A	Refer to appendix 1
E12	LF	DFN&SOIC	Refer to JCET SOP & DFN Tin Whisker report		

6. MTBF&FIT

Supporting Data (Ea = 0.7 eV, Confidence Level = 60%)							MTBF (hrs)	FIT
Test Temp.	Test Voltage	Duration	QTY	Fail QTY	Operation Temp.	Operation Voltage	2.94E+07	33.96
125°C	28V	1000 hrs	231	0	55°C	28V		
125°C	28V	48 hrs	2400	0	55°C	28V		

Note: The FIT data is generated based on Arrhenius model and voltage acceleration model.

7. Conclusion

CA-IF1145FNF-Q1 & CA-IF1145FDF-Q1 series products are qualified by AEC-Q100 standard.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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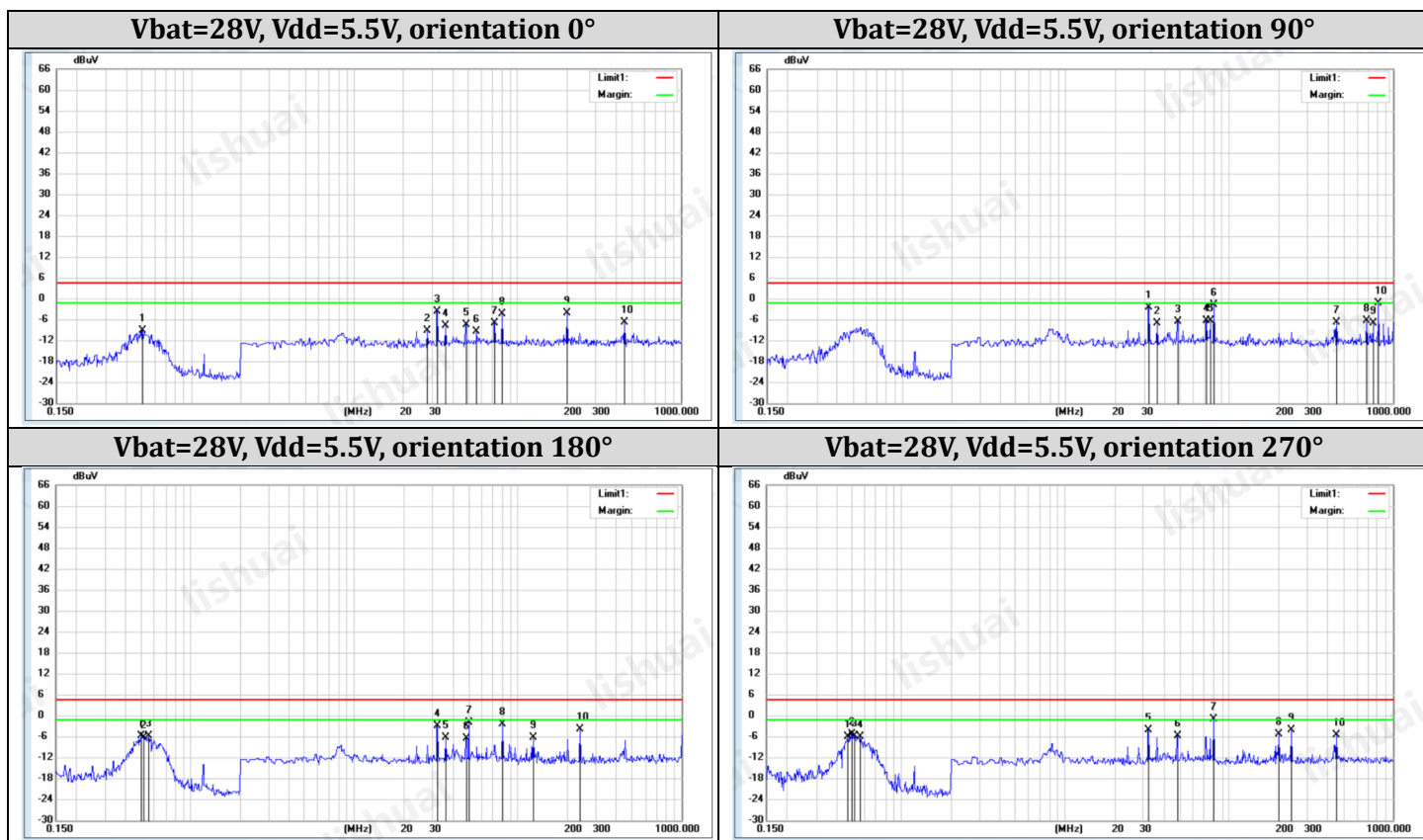
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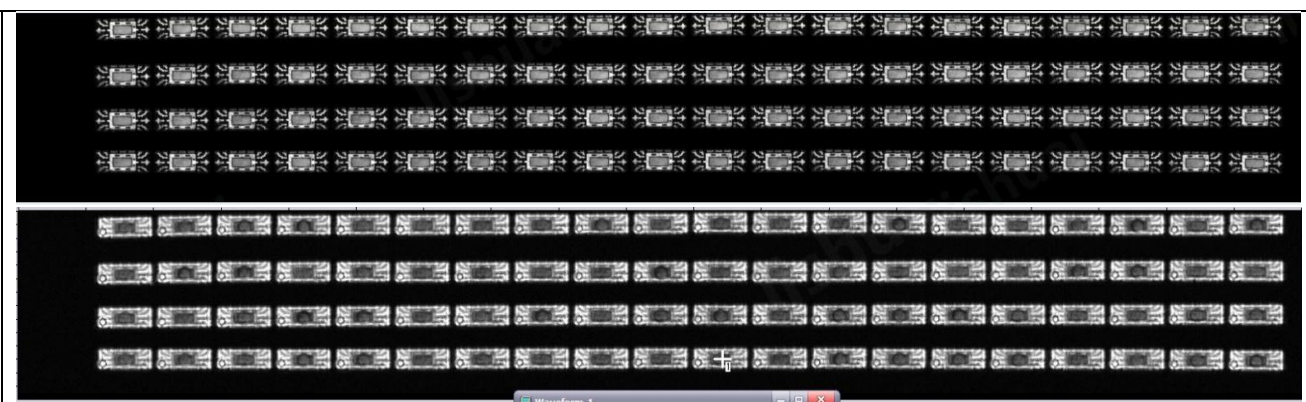
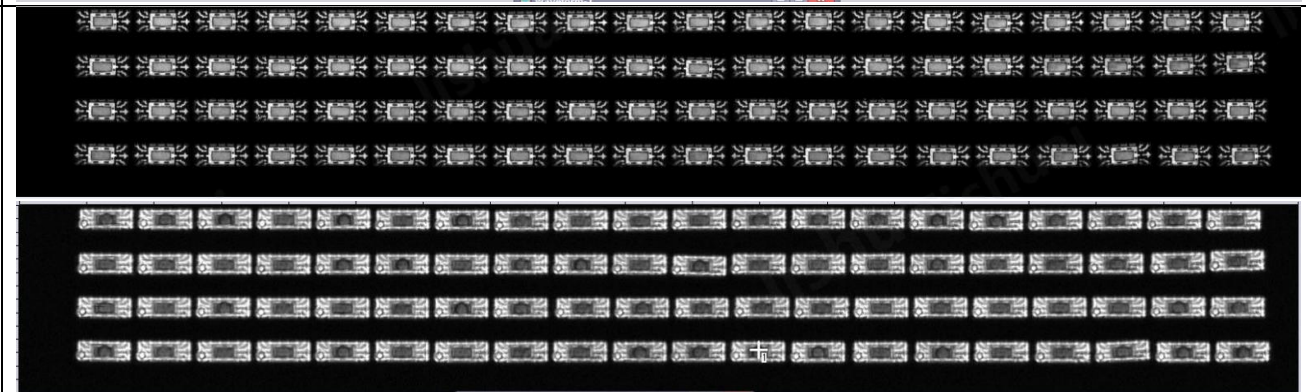
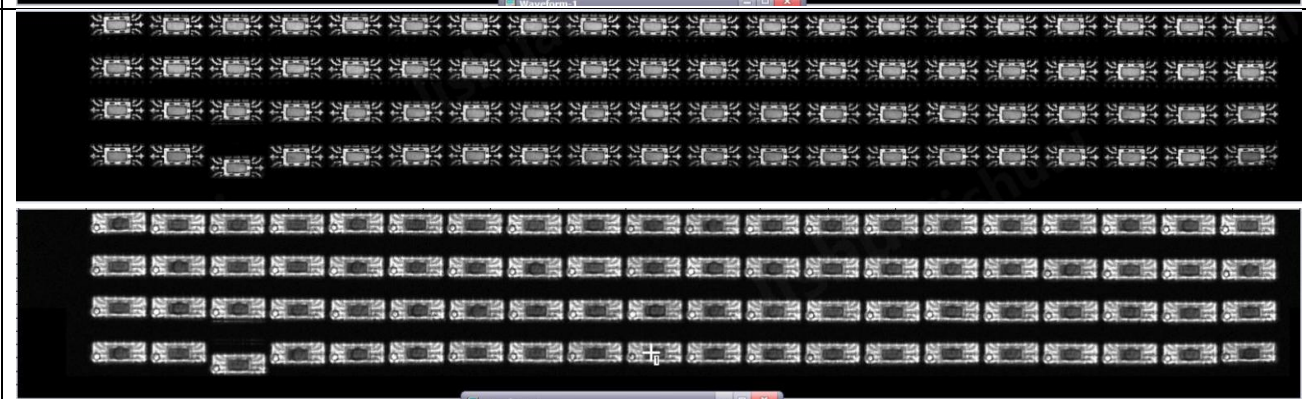
Revision History

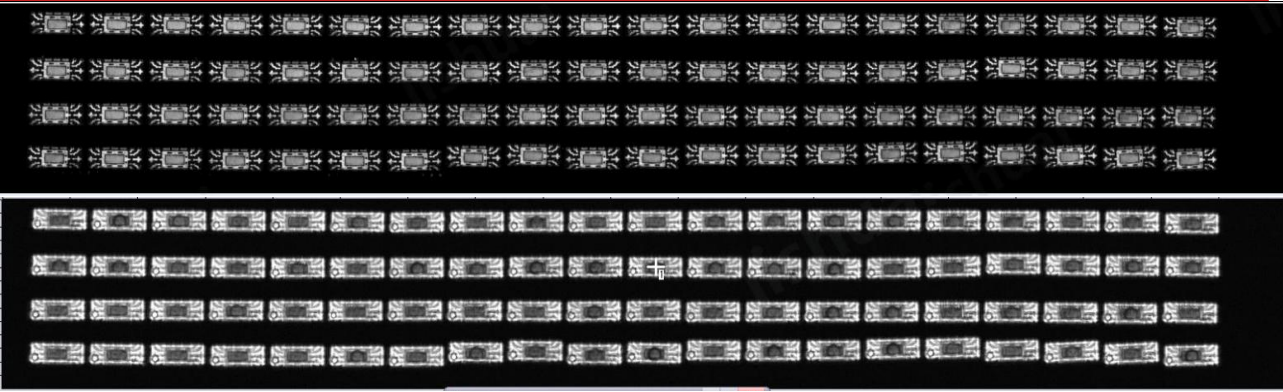
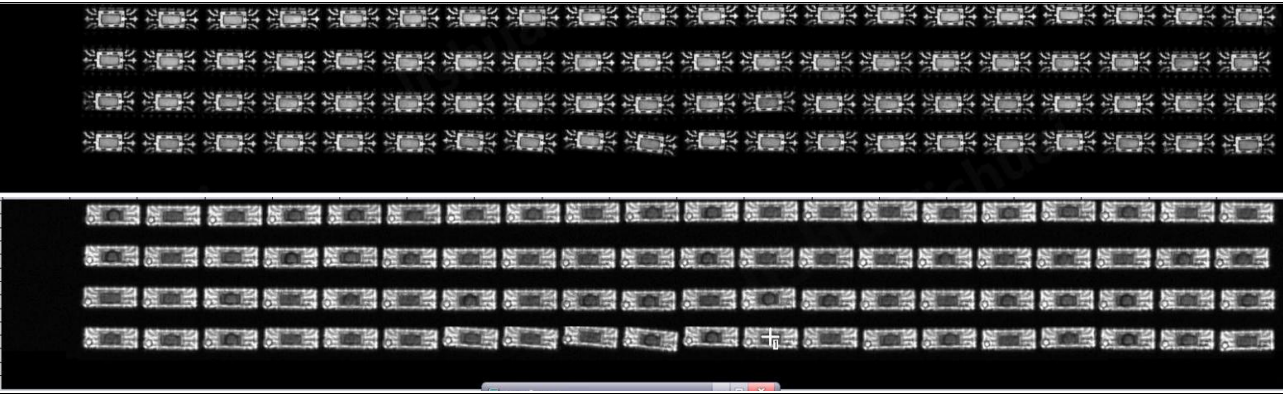
Revision	Change Log	Date
V1.0	Initial	2025/3/4
V1.1	Add DFN package qual. result	2025/11/4

Appendix 1: EMC Test Results



Appendix 2: SAT Test Results

Lot 1 pre- MSL	 This section contains two rows of microscopic images. The top row shows three images of component surfaces with visible defects. The bottom row shows three images of component surfaces, also with visible defects. A small scale bar is visible at the bottom of the second row.
Lot 1 post- MSL	 This section contains two rows of microscopic images. The top row shows three images of component surfaces with improved quality. The bottom row shows three images of component surfaces, also with improved quality. A small scale bar is visible at the bottom of the second row.
Lot 2 pre- MSL	 This section contains two rows of microscopic images. The top row shows three images of component surfaces with visible defects. The bottom row shows three images of component surfaces, also with visible defects. A small scale bar is visible at the bottom of the second row.
Lot 2 post- MSL	 This section contains two rows of microscopic images. The top row shows three images of component surfaces with improved quality. The bottom row shows three images of component surfaces, also with improved quality. A small scale bar is visible at the bottom of the second row.

Lot 3 pre- MSL	 This block contains two rows of microscopic images of Lot 3 pre-MSL chips. The top row shows four horizontal strips of chips, each strip containing approximately 20 individual chip images. The bottom row also shows four horizontal strips of chips, each strip containing approximately 20 individual chip images. The chips appear as small, rectangular, metallic structures with a grid-like pattern.
Lot 3 post- MSL	 This block contains two rows of microscopic images of Lot 3 post-MSL chips. The top row shows four horizontal strips of chips, each strip containing approximately 20 individual chip images. The bottom row also shows four horizontal strips of chips, each strip containing approximately 20 individual chip images. The chips appear as small, rectangular, metallic structures with a grid-like pattern.