CA-IS1306x 5-kV$_{RMS}$ Isolated Sigma-Delta Modulator With External Clock

1 Key Features

- Differential Input Voltage Range: ±250 mV
- Uncoded Data Output Options
- Low Offset Error: ±100 µV (max) at 25°C
- Low Gain Error: ±0.2% (max) at 25°C
- Excellent Drift Specifications
  - ±3.5 µV/°C (max) Offset Drift
  - ±40 ppm/°C (max) Gain Drift
- Excellent AC Performance
  - SNR: 85dB (typ)
  - THD: –93dB (typ)
- 16-Bit Resolution With No Missing Codes
- 3.3-V or 5-V Operation for Both High- and Low-Side
- High CMTI: ±150 kV/µs (typ)
- Fault Diagnostic Functions for System Safety
- Wide Operating Temperature Range: –40°C to 125°C
- Safety-Related Certifications
  - VDE certification according to DIN EN IEC 60747-17(VDE 0884-17):2021-10
  - UL certification according to UL 1577
  - CQC certification according to GB4943.1-2022
  - TUV certification
- >40-year Life at Rated Working Voltage

2 Applications

- Industrial Motor Controls and Drives
- Isolated Switch Mode Supplies
- Uninterruptible Power Supplies

3 Description

The CA-IS1306x devices are series of high-precision isolated sigma-delta (ΣΔ) modulators and optimized for shunt-resistor-based current sensing. Low offset and gain error and drift guarantee that measuring accuracy is maintained over the entire operating temperature range.

The CA-IS1306x devices utilize silicon oxide (SiO_2) isolation barriers and support up to 5-kV$_{RMS}$ galvanic isolation per UL 1577. This technology separates high- and low-voltage domain to protect lower-voltage parts from damage and provides low emissions as well as strong anti-interference capability from magnetic changes. The high common-mode transient immunity (CMTI) means that the CA-IS1306x devices transmit correct signals through isolation barriers and are suitable for industrial motor controls and drives which require high-voltage and high-power switching. The internal input common-mode overvoltage and missing high-side supply voltage detection functions contribute to fault diagnostics and system safety.

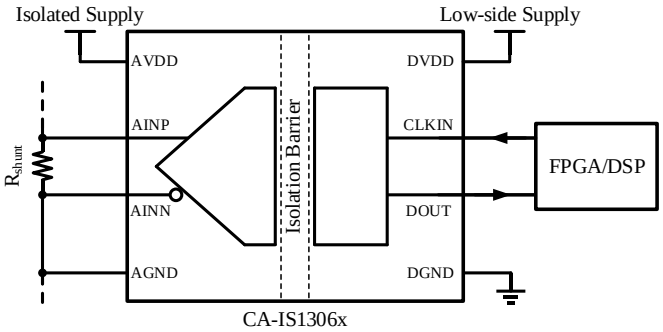
The CA-IS1306x devices can achieve an 86 dB signal-to-noise (SNR) and 16-bit resolution at 78.1 kSPS with a sinc^3 filter. The external clock frequency ranges from 5 MHz to 21 MHz and offers flexibility of use.

The CA-IS1306x devices are packaged in wide body, 8-pin or 16-pin SOIC packages and specified over the extended industrial temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS1306M25G	SOIC8-WB (G)	5.85 mm × 7.50 mm
CA-IS1306AM25W	SOIC16-WB (W)	10.30 mm × 7.50 mm
CA-IS1306M25W	SOIC16-WB (W)	10.30 mm × 7.50 mm

Simplified Schematic



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Specified Input Range	Package	Isolation Rating	Digital Output Encoded Mode
CA-IS1306M25G	±250 mV	SOIC8-WB (G)	5000 V_{RMS}	Uncoded CMOS
CA-IS1306AM25W	±250 mV	SOIC16-WB (W)	5000 V_{RMS}	Uncoded CMOS
CA-IS1306M25W	±250 mV	SOIC16-WB (W)	5000 V_{RMS}	Uncoded CMOS

NOTE:

1. The only difference between CA-IS1306M25W and CA-IS1306AM25W is pin arrangement. Refer to 6.2 and 6.3 for more detailed information.

Table of Contents

5 Revision History

Revision	Description	Page
Version 1.00	Revised the CA-IS1306M25 specs	7~9
	Added typical characteristics and waveforms	10~13
Version 1.01	Add CA-IS1306AM25 part number and package information	5, 26
	Updated CMRR, PSRR data	10
	Updated I_{DVDD} data and some typical curves	10, 16
	Updated INL, DNL, CMRR and PSRR curves	18
Version 1.02	Added CA-IS1306M25W part number and PIN descriptions	1, 2, 6, 30
Version 1.03	Removed part number CA-IS1306E25G	30
Version 1.04	Updated UL certification	9
Version 1.05	Updated TUV and VDE certification	8~9
Version 1.06	Updated TUV and UL certification	9
Version 1.07	Updated safety-related certifications	8~9
	Updated recommended land patterns for SOIC8-WB and SOIC16-WB	27~28
	Updated tape and reel information of CA-IS1306M25G	30
	Modified other items to keep same with Chinese version	All

6 Pin Descriptions and Functions

6.1 CA-IS1306x25G

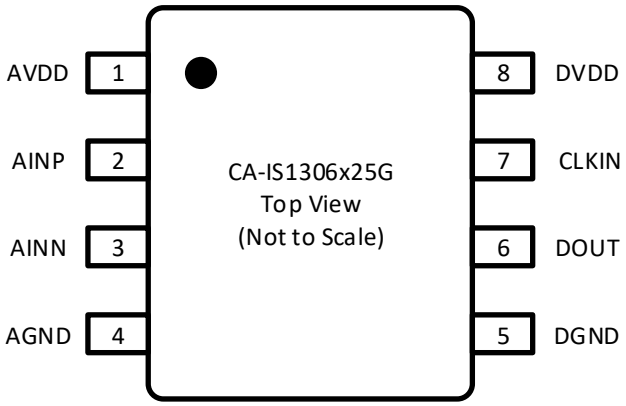


Figure 6-1 CA-IS1306x25G Top View

Table 6-1 CA-IS1306x25G Pin Description and Functions

NAME	NUMBER	TYPE	DESCRIPTION
AVDD	1	Power	High-side (analog) power supply, 3 V to 5.5 V
AINP	2	Input	Noninverting analog input
AINN	3	Input	Inverting analog input
AGND	4	Ground	High-side (analog) ground
DGND	5	Ground	Low-side (digital) ground
DOUT	6	Output	Modulator data output
CLKIN	7	Output	Modulator clock input with internal 1.5-MΩ pulldown resistor, 5 MHz to 21 MHz
DVDD	8	Power	Low-side (digital) power supply, 3 V to 5.5 V

6.2 CA-IS1306AM25W

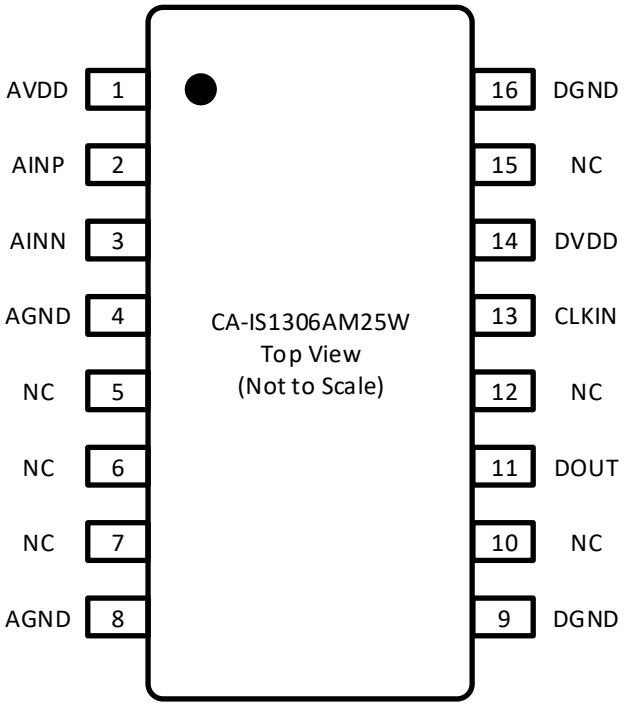


Figure 6-2 CA-IS1306AM25W Top View

Table 6-2 CA-IS1306AM25W Pin Description and Functions

NAME	NUMBER	TYPE	DESCRIPTION
AVDD	1	Power	High-side (analog) power supply, 3 V to 5.5 V
AINP	2	Input	Noninverting analog input
AINN	3	Input	Inverting analog input
AGND	4, 8	Ground	High-side (analog) ground
DGND	9, 16	Ground	Low-side (digital) ground
DOUT	11	Output	Modulator data output
CLKIN	13	Output	Modulator clock input with internal 1.5-MΩ pulldown resistor, 5 MHz to 21 MHz
DVDD	14	Power	Low-side (digital) power supply, 3 V to 5.5 V
NC	5, 6, 7	--	No internal connection, could be left floating or connect to AVDD or AGND
	10, 12, 15	--	No internal connection, could be left floating or connect to DVDD or DGND

6.3 CA-IS1306M25W

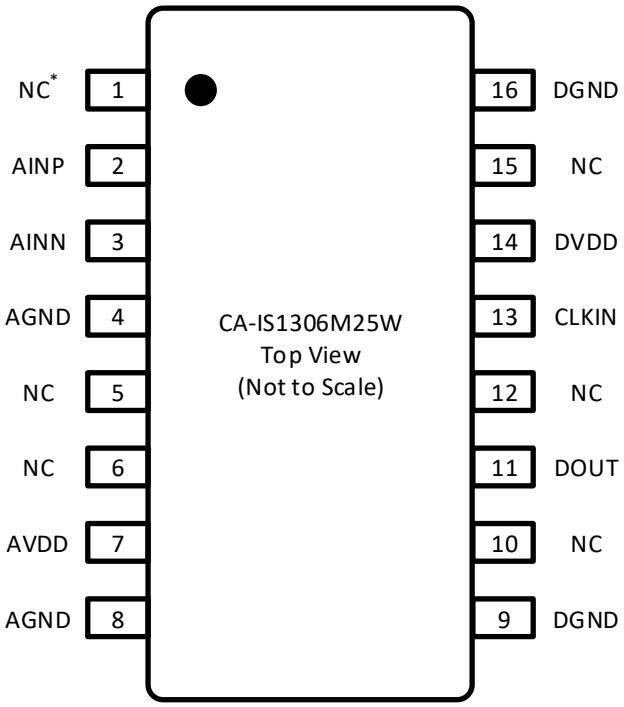


Figure 6-3 CA-IS1306M25W Top View

Table 6-3 CA-IS1306M25W Pin Description and Functions

NAME	NUMBER	TYPE	DESCRIPTION
AVDD	7	Power	High-side (analog) power supply, 3 V to 5.5 V
AINP	2	Input	Noninverting analog input
AINN	3	Input	Inverting analog input
AGND	4, 8	Ground	High-side (analog) ground
DGND	9, 16	Ground	Low-side (digital) ground
DOUT	11	Output	Modulator data output
CLKIN	13	Output	Modulator clock input with internal 1.5-MΩ pulldown resistor, 5 MHz to 21 MHz
DVDD	14	Power	Low-side (digital) power supply, 3 V to 5.5 V
NC	1*	--	This pin connects to AVDD internally, could be left floating or connect to AVDD
	5, 6	--	No internal connection, could be left floating or connect to AVDD or AGND
	10, 12, 15	--	No internal connection, could be left floating or connect to DVDD or DGND

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
AVDD, DVDD	Supply voltage[2]	–0.5	6.5	V
AINP, AINN	Analog input voltage	AGND – 6	6.5	V
CLKIN, DOUT	Digital input or output voltage	DGND – 0.5	DVDD + 0.5[3]	V
I_{IN}	Input current to any pin except supply pins	–10	10	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the local ground terminal (AGND or DGND) and are peak voltage values.
3. Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±2000	

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
AVDD	High-side (analog) supply voltage, with respect to AGND	3.0	5.0	5.5	V
DVDD	Low-side (digital) supply voltage, with respect to DGND	3.0	3.3	5.5	V
T_A	Operating ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC		VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation for both sides	CA-IS1306Mx, AVDD = DVDD = 5.5 V	129.25	mW
P_{D1}	Maximum power dissipation for high-side	AVDD = 5.5 V	90.75	mW
P_{D2}	Maximum power dissipation for low-side	CA-IS1306Mx, DVDD = 5.5 V	38.50	mW

7.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	7070	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	9846	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~ 1	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
Reinforced insulation (SOIC8-WB/SOIC16-WB) V_{IORM}: 1414 V_{PK} V_{IOTM}: 7070 V_{PK} V_{IOSM}: 12800 V_{PK}	Single protection SOIC8-WB: 5000V_{RMS} SOIC16-WB: 5000V_{RMS}	Reinforced insulation (Altitude ≤ 5000 m)	EN 61010-1 SOIC8-WB: 5000V_{RMS} SOIC16-WB: 5000V_{RMS} EN 62368-1 SOIC8-WB: 5000V_{RMS} SOIC16-WB: 5000V_{RMS}
Certification Number: 40057278	Certification Number: E511334	Certification Number: SOIC16-WB: CQC23001406424 SOIC8-WB: CQC24001434134	Client reference number: 2253313

7.8 Electrical Characteristics: CA-IS1306x25

All minimum and maximum specifications apply from T_A = –40°C to 125°C, AVDD = 3 V to 5.5 V, DVDD = 3 V to 5.5 V, AINP = –250 mV to 250 mV, AINN = AGND = 0 V, and sinc3 filter off chip configured to 16 bits with OSR = 256 (unless otherwise noted). All typical specifications are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5 V, and DVDD = 3.3 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
$V_{Clipping}$	Maximum input voltage before clipping output	AINP – AINN		±320		mV
V_{FSR}	Specified linear full-scale input range	AINP – AINN	–250		250	mV
V_{CM}	Operating common-mode input voltage	(AINP + AINN) / 2 to AGND	–0.16		AVDD – 2.1	V
V_{CMOV}	Common-mode overvoltage threshold	(AINP + AINN) / 2 to AGND	AVDD – 2			V
	Hysteresis of common-mode over-voltage threshold			100		mV
C_{IN}	Single-ended input capacitance	AINN = AGND		2		pF
C_{IND}	Differential input capacitance			1		pF
R_{IN}	Single-ended input resistance	AINN = AGND		19		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IN}	Input current	AINP = AINN = AGND, $I_{IN} = (I_{INP} + I_{INN}) / 2$	–41	–30	–24	µA
TCI_{IN}	Input current drift			±1		nA/°C
I_{INOS}	Input offset current	$I_{INOS} = I_{INP} – I_{INN}$		±5		nA
CMRR	Common-mode rejection ratio	DC, AINP = AINN		–85		dB
		f_{IN} = 10 kHz, AINP = AINN		–85		
PSRR	Power supply rejection ratio	At AVDD, DC, AINP = AINN = AGND		–98		dB
		At AVDD, 100-mV and 10-kHz ripple, AINP = AINN = AGND		–98		
BW_{IN}	Input bandwidth (–3 dB)[1]			1000		kHz
CMTI	Common-mode transient immunity	|AGND – DGND| = 1.5 kV	100	150		kV/µs
MODULATOR ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity[1]	Resolution: 16 bits,	–6	±2	6	LSB
E_O	Offset error	Initial, at T_A = 25°C, AINP = AINN = AGND	–100	±4.5	100	µV
TCE_O	Offset drift		–3.5	±0.5	3.5	µV/°C
E_G	Gain error	Initial, at T_A = 25°C	–0.2%	±0.05%	0.2%	
TCE_G	Gain drift		–40	±20	40	ppm/°C
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10kHz		85		dB
SINAD	Signal-to-noise-and-distortion ratio			84		dB
THD	Total harmonic distortion			–93		dB
SFDR	Spurious-free dynamic range			94		dB

NOTE:

1. Guaranteed by design.
2. The INL is defined as the maximum deviation from a straight line passing through the end-point of the ideal ADC transfer function once the gain and offset errors have been nullified and expressed as number of LSBs over the specified linear full-scale input range.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	0		7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	Logic high-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Logic low-level input voltage		–0.3		0.3 × DVDD	V
DIGITAL OUTPUT						
C_L	Output load capacitance	f_{CLKIN} = 20 MHz		30		pF
V_{OH}	Logic high-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			
V_{OL}	Logic low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
POWER SUPPLY						
$AVDD_{UV}$	AVDD undervoltage threshold	AVDD rising		2.5	2.7	V
I_{AVDD}	High-side supply current	3.0 V ≤ AVDD ≤ 3.6 V		10.5	15.0	mA
		4.5 V ≤ AVDD ≤ 5.5 V		11.5	16.5	
I_{DVDD}	Low-side supply current with C_L = 15 pF[1]	CA-IS1306M25, 3.0 V ≤ DVDD ≤ 3.6 V		3.3	5.3	mA
		CA-IS1306M25, 4.5 V ≤ DVDD ≤ 5.5 V		4.0	7.0	

NOTE:
1. C_L is approximately 15 pF including probe and stray capacitance.

7.9 Switching Characteristics

All minimum and maximum specifications apply from T_A = –40°C to 125°C, AVDD = 3 V to 5.5 V, DVDD = 3 V to 5.5 V, AINP = –50 mV to 50 mV for CA-IS1306x05, AINP = –250 mV to 250 mV for CA-IS1306x25, AINN = AGND = 0 V, and sinc3 filter off chip configured to 16 bits with OSR = 256 (unless otherwise noted). All typical specifications are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLKIN}	CLKIN clock frequency	4.5 V ≤ AVDD ≤ 5.5 V	5		21	MHz
		3.0 V ≤ AVDD ≤ 5.5 V	5		20	
Duty Cycle	CLKIN clock duty cycle	t_{HIGH} / t_{CLKIN}, 3.0 V ≤ AVDD ≤ 5.5 V	45%	50%	55%	
		t_{HIGH} / t_{CLKIN}, 4.5 V ≤ AVDD ≤ 5.5 V	42.5%	50%	57.5%	
t_h	Hold time of DOUT after rising edge of CLKIN[1]	C_L = 15 pF[1]; *See Figure 7-1*	3.5			ns
t_d	Delay time of DOUT after rising edge of CLKIN[1]	C_L = 15 pF[1]; *See Figure 7-1*			16	ns
t_r	Rise time of DOUT (20%–80%)	C_L = 15 pF[1]		1.8	5	ns
t_f	Fall time of DOUT (80%–20%)	C_L = 15 pF[1]		1.8	5	ns
t_{astart}	Analog startup time	AVDD step to 3.0 V with 3.0 V ≤ DVDD; *See Figure 7-2*		500		µs

NOTE:
1. C_L is approximately 15 pF including probe and stray capacitance.

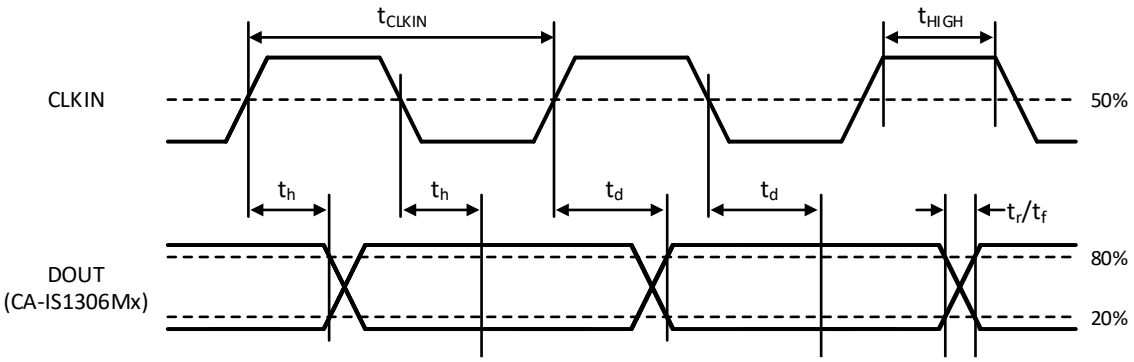


Figure 7-1 CA-IS1306x Digital Output Timing

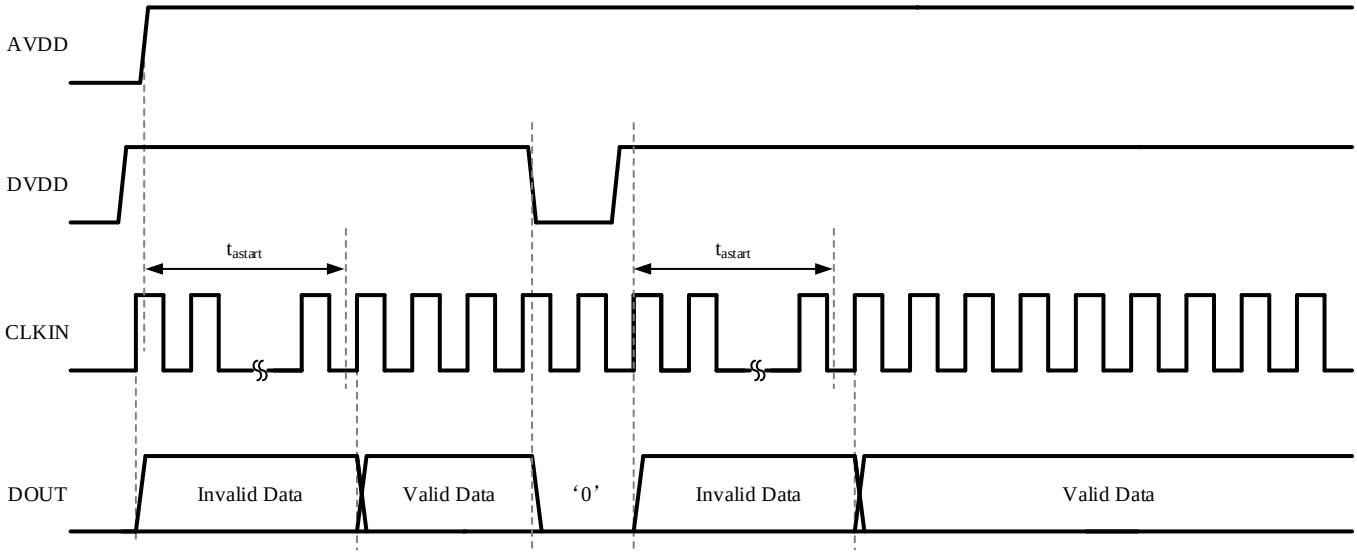


Figure 7-2 CA-IS1306x Startup Timing

7.10 Typical Characteristics

All typical specifications are at AINP = –250 mV to 250 mV, AINN = AGND = 0 V, AVDD = 5 V, DVDD = 3.3 V, CLKIN = 20MHz, and sinc3 filter off chip configured to 16 bits with OSR = 256 (unless otherwise noted).

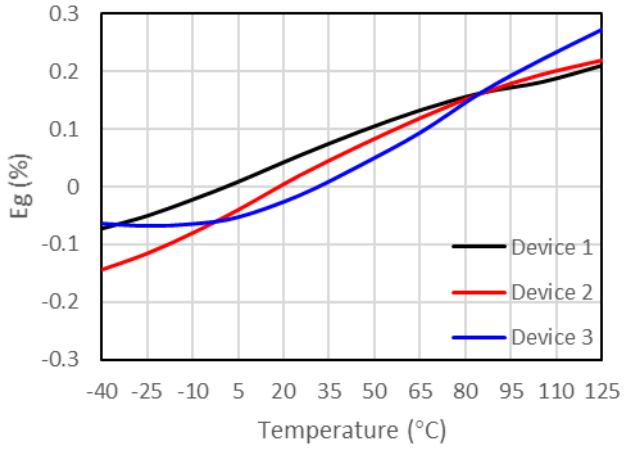


Figure 7-3 Gain Error vs. Temperature

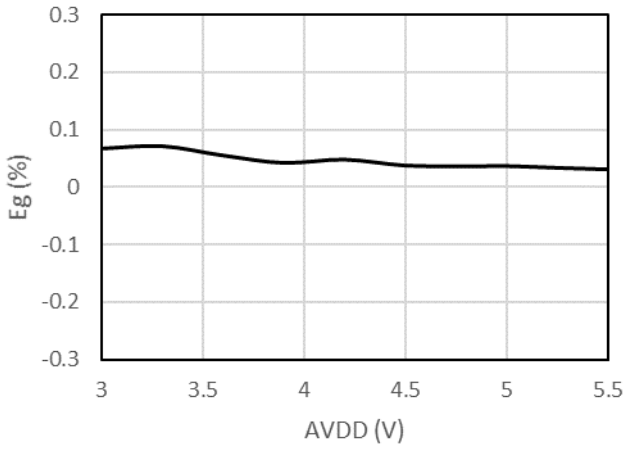


Figure 7-4 Gain Error vs. High-side Supply Voltage

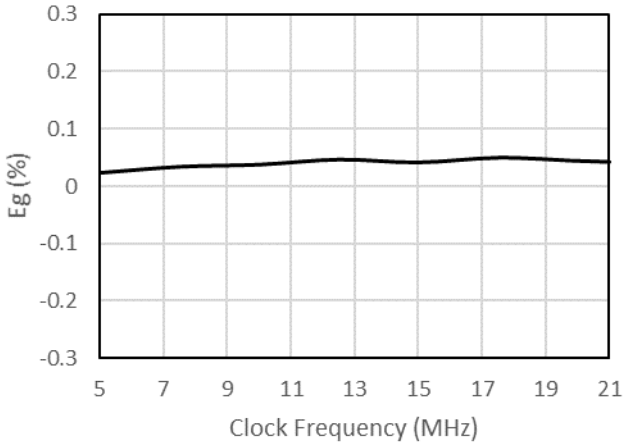


Figure 7-5 Gain Error vs. Clock Frequency

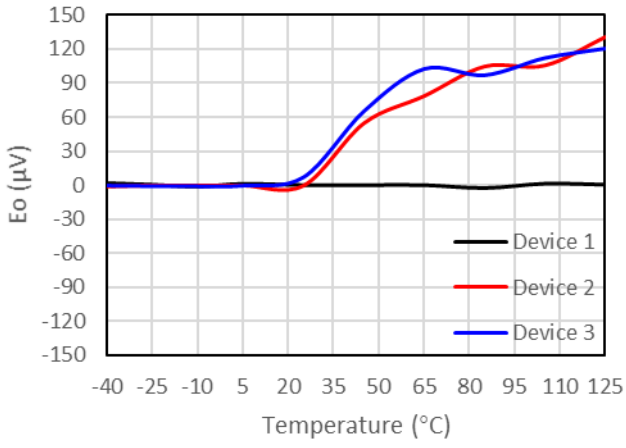


Figure 7-6 Offset Error vs. Temperature

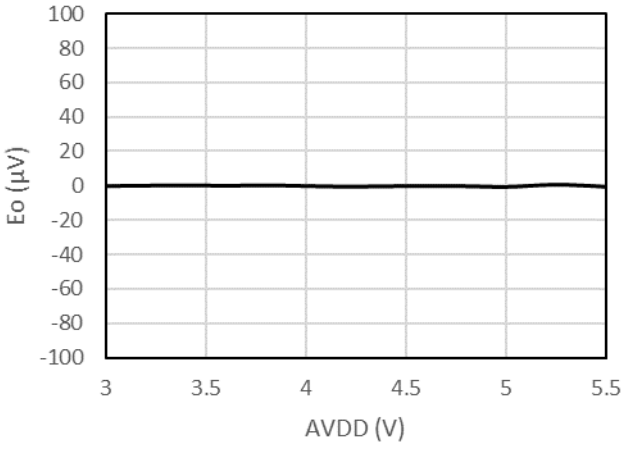


Figure 7-7 Offset Error vs. High-side Supply Voltage

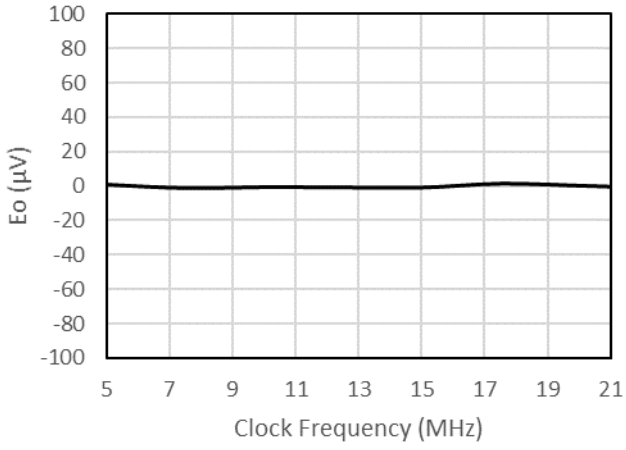


Figure 7-8 Offset Error vs. Clock Frequency

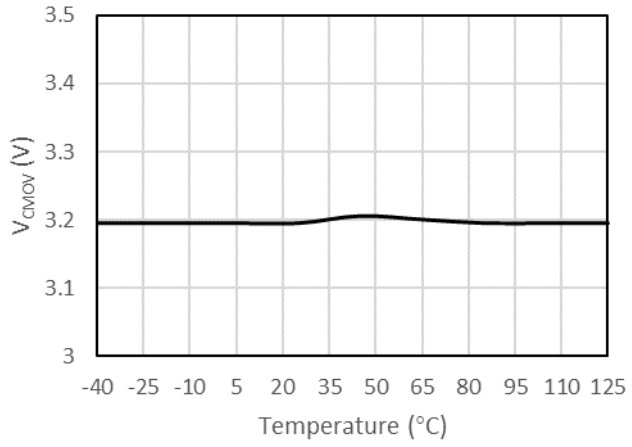


Figure 7-9 Common-Mode Overvoltage Threshold vs. Temperature

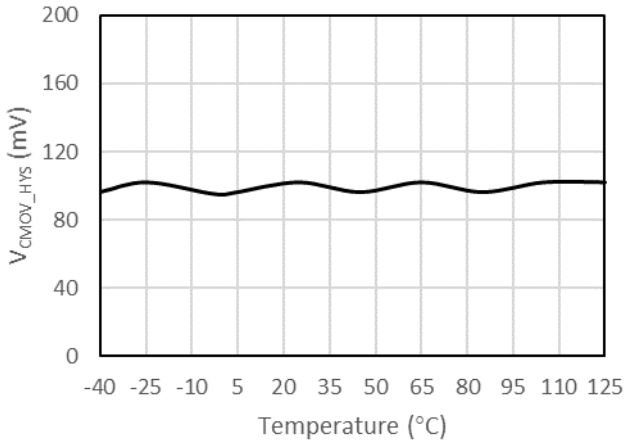


Figure 7-10 Hysteresis of V_{CMOV} vs. Temperature

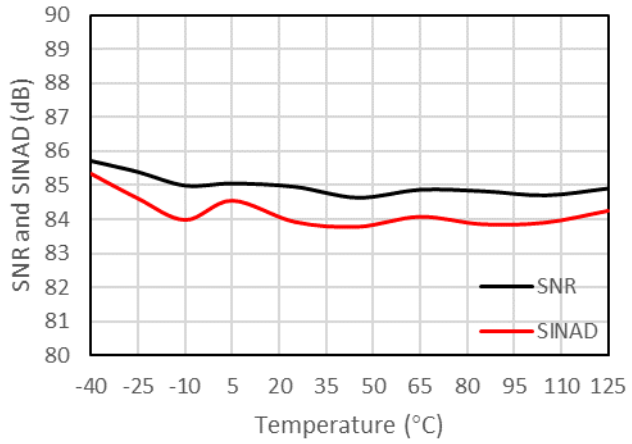


Figure 7-11 SNR and SINAD vs. Temperature

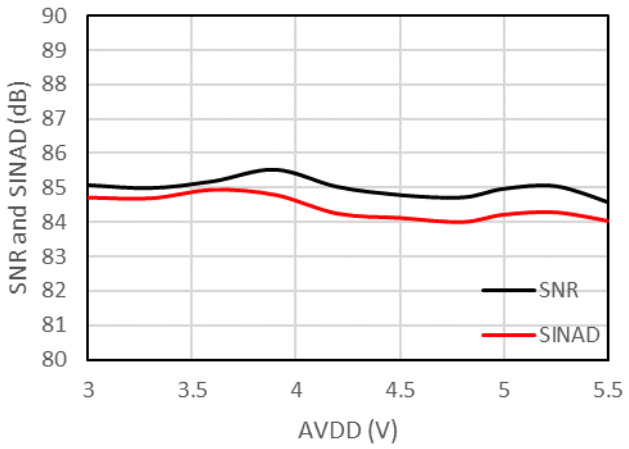


Figure 7-12 SNR and SINAD vs. High-side Supply Voltage

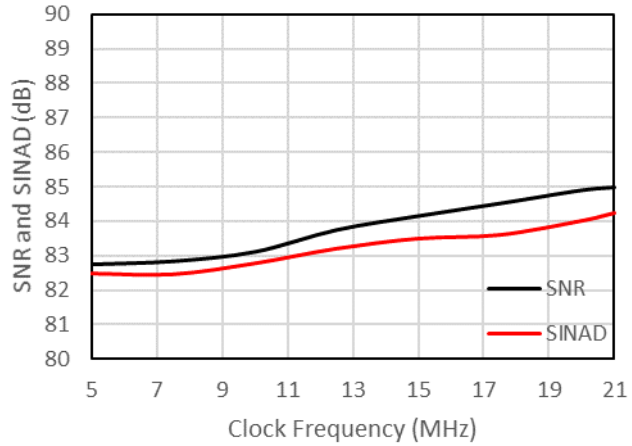


Figure 7-13 SNR and SINAD vs. Clock Frequency

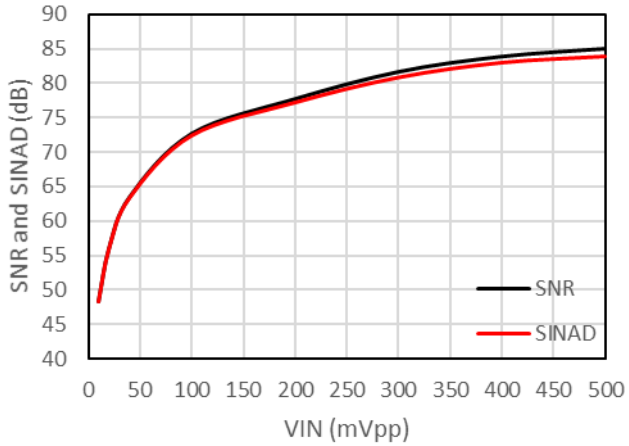


Figure 7-14 SNR and SINAD vs. Input Signal Amplitude

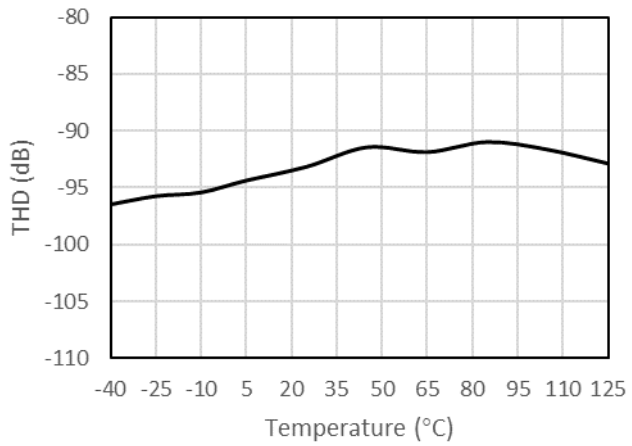


Figure 7-15 THD vs. Temperature

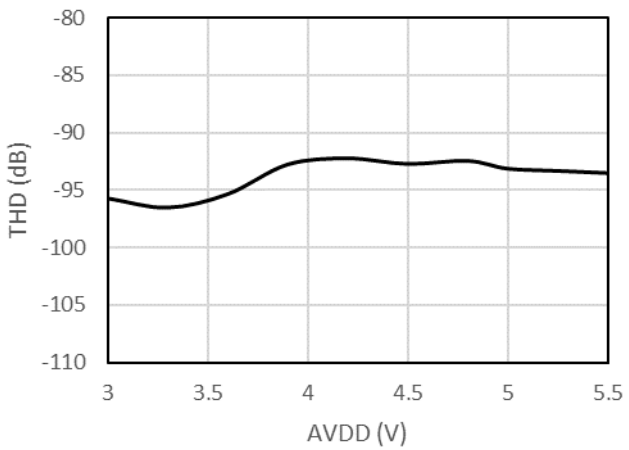


Figure 7-16 THD vs. High-side Supply Voltage

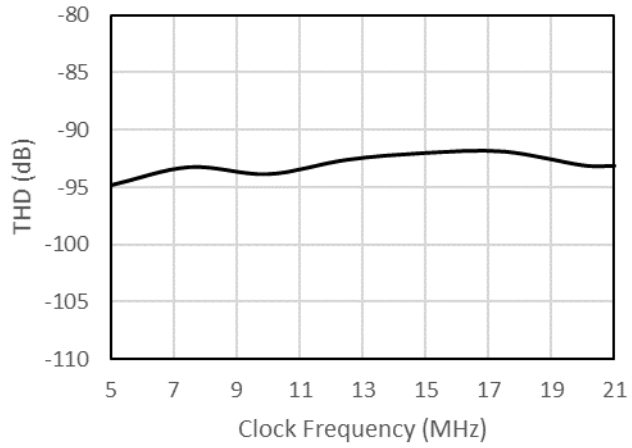


Figure 7-17 THD vs. Clock Frequency

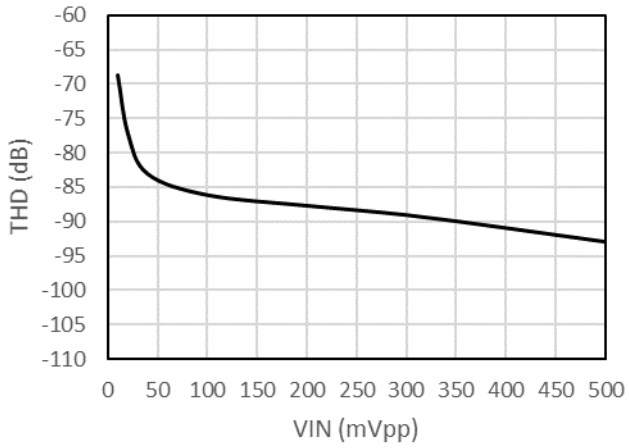


Figure 7-18 THD vs. Input Signal Amplitude

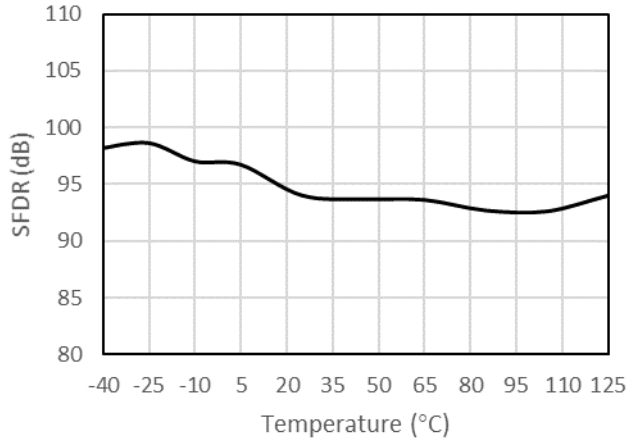


Figure 7-19 SFDR vs. Temperature

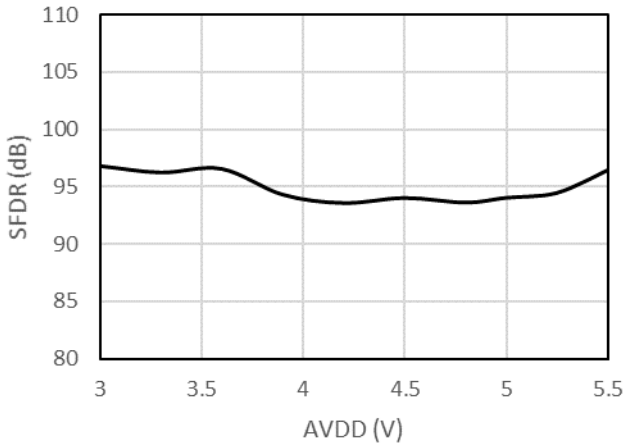


Figure 7-20 SFDR vs. High-side Supply Voltage

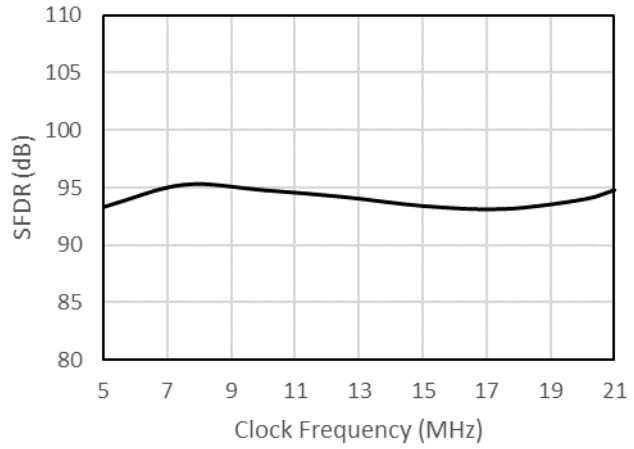


Figure 7-21 SFDR vs. Clock Frequency

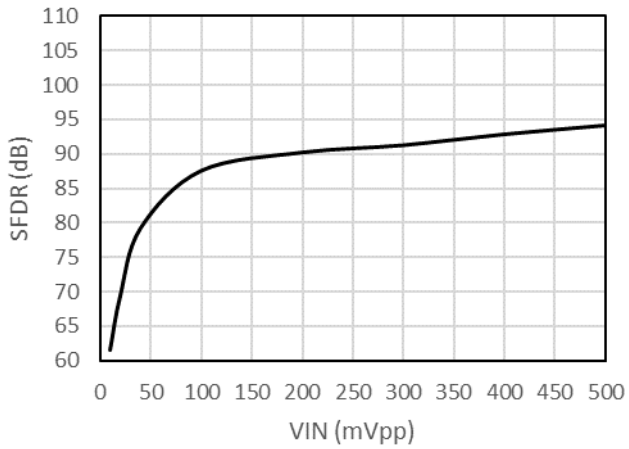


Figure 7-22 SFDR vs. Input Signal Amplitude

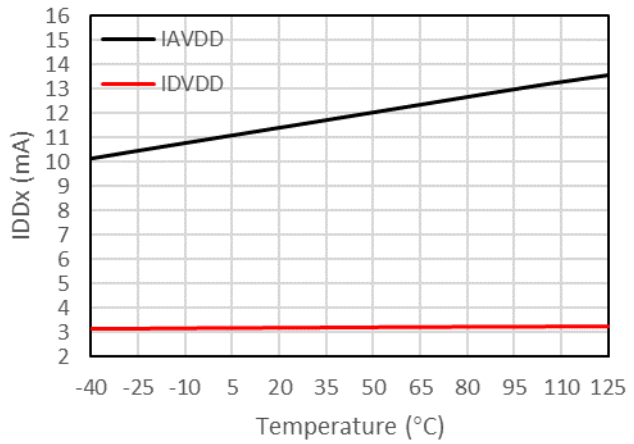


Figure 7-23 Supply Current vs. Temperature

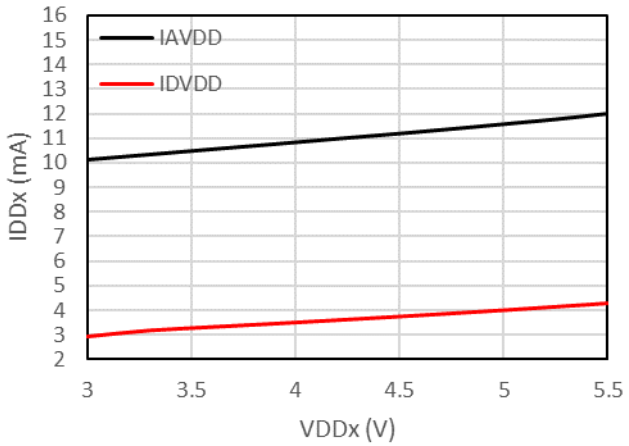


Figure 7-24 Supply Current vs. Supply Voltage

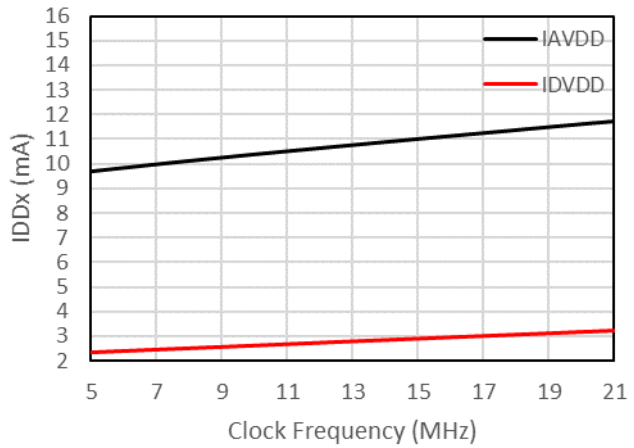


Figure 7-25 Supply Current vs. Clock Frequency

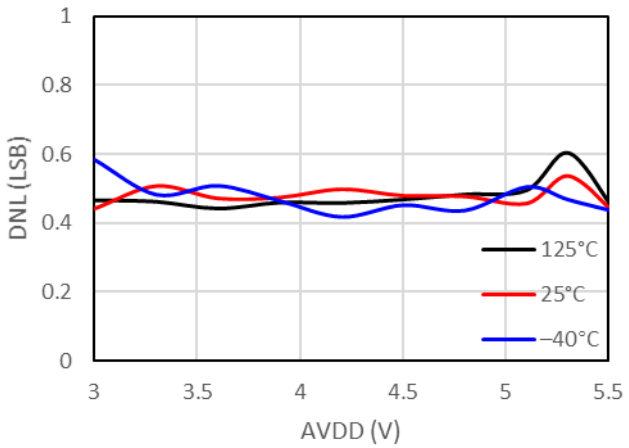


Figure 7-26 DNL vs. Supply Voltage

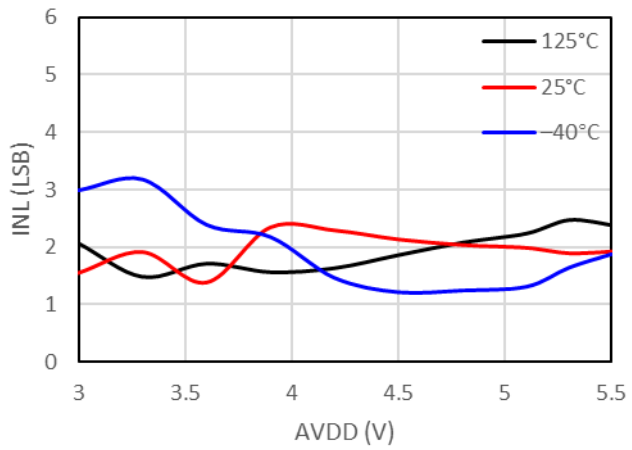


Figure 7-27 INL vs. Supply Voltage

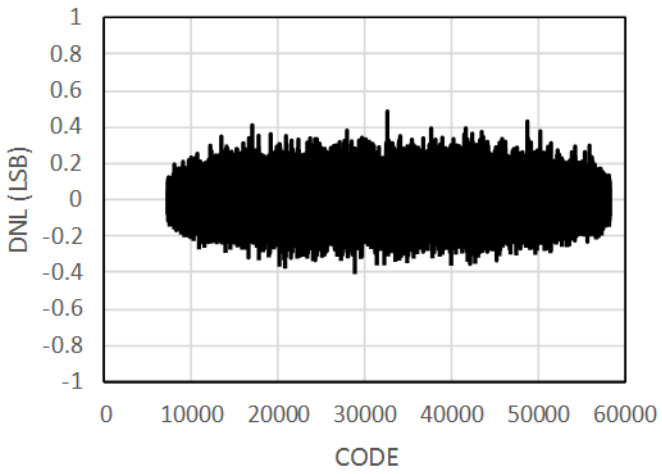


Figure 7-28 Typical DNL Curve

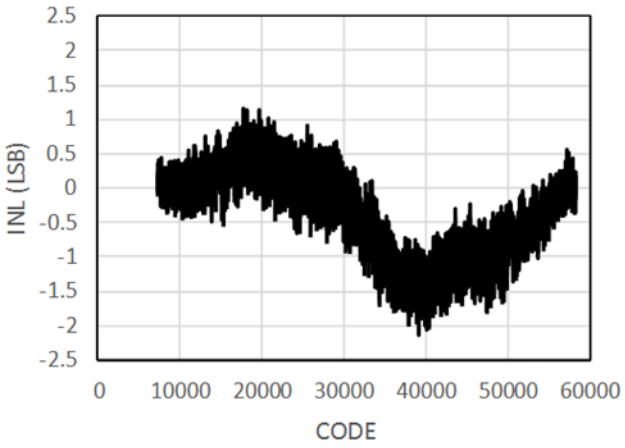


Figure 7-29 Typical INL Curve

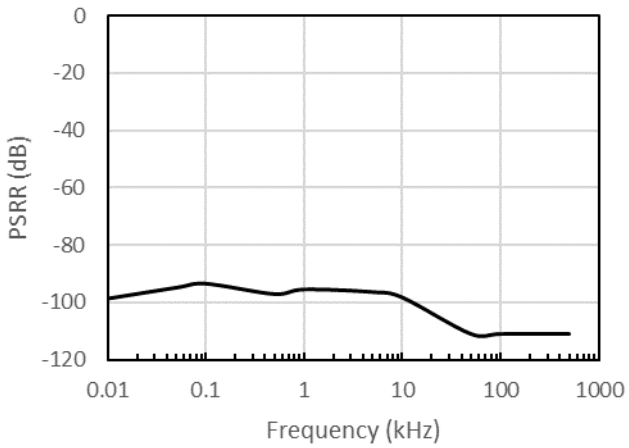


Figure 7-30 PSRR vs. Frequency

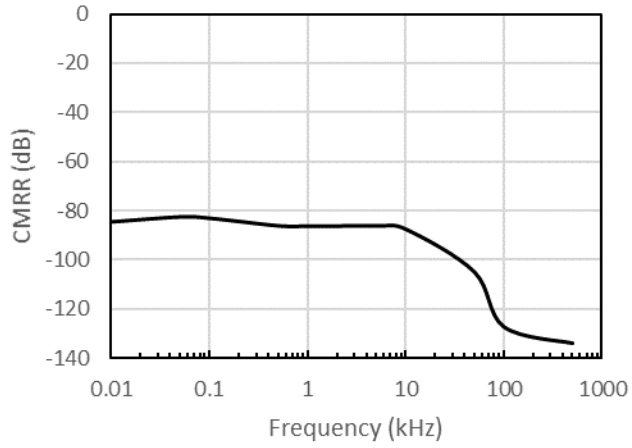


Figure 7-31 CMRR vs. Frequency

8 Detailed Description

8.1 System Overview

The CA-IS1306x devices are series of high-precision isolated sigma-delta (ΣΔ) modulators optimized for shunt-resistor-based current sensing. The functional block diagram of this device is shown in Figure 8-1. At high side, the fully differential amplifier pre-amplifies the measuring voltage across a shunt resistor and then drives a 2nd-order sigma-delta (ΣΔ) modulator. This modulator converts the analog signal to a 1-bit digital bitstream. For transmission across the SiO_2-based isolation barrier, the digital stream is further modulated with a high-frequency carrier using a simple on-off keying (OOK) modulation scheme. The receiver (RX) recoveries the modulated signal to the original digital bitstream at low side. For synchronization of the whole chip, the external clock is sent back to high side ensuring that all clocks come from one source. The output bitstream is synchronous to the external clock at CLKIN pin. The time average of this serial bitstream is proportional to the analog input voltage within the specific range. The external clock input contributes to the synchronization of multiple current-sensing channels at the system level.

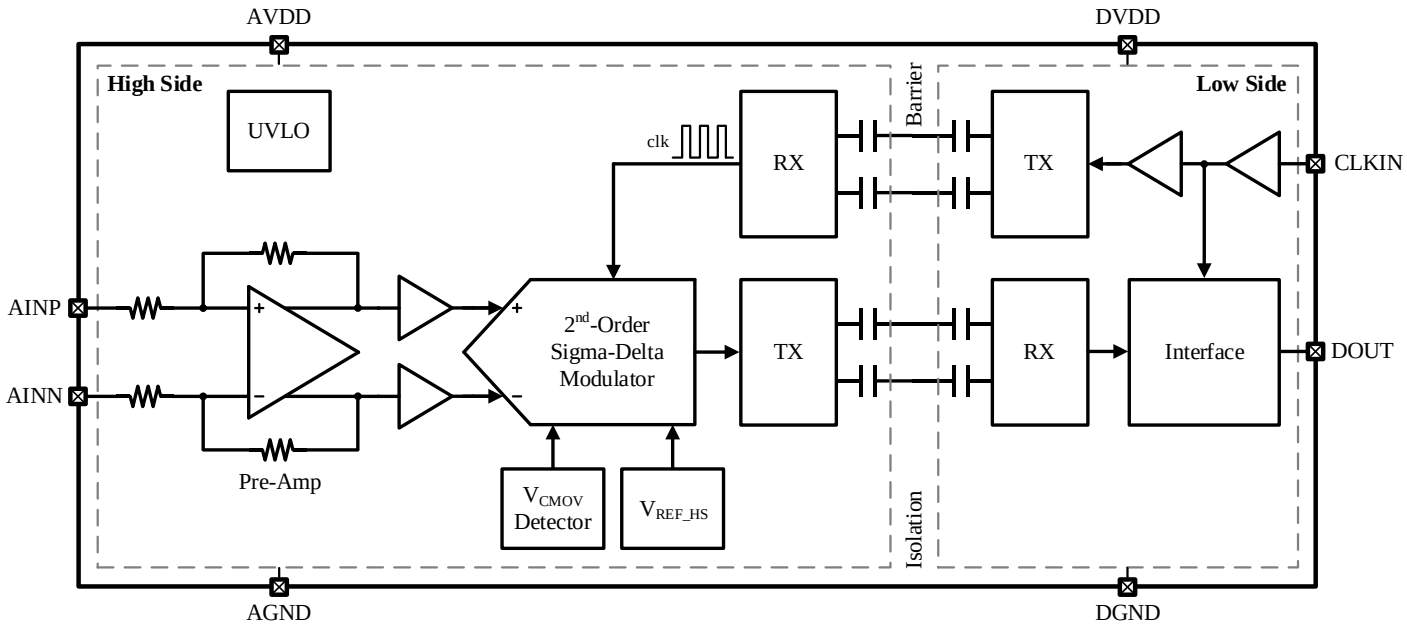


Figure 8-1 Functional Block Diagram of CA-IS1306x

8.2 Feature Description

8.2.1 Analog Input

The CA-IS1306x device utilizes a fully differential amplifier stage to pre-amplify the measuring voltage across the shunt resistor. The nominal gain of the front-end differential amplifier is 4 for CA-IS1306x25 (±250-mV input voltage range), ensuring that the 2nd-order sigma-delta modulator is not saturated in both cases within the specific input voltage range. This gain is set by the internal high-precision resistor network and different gain brings different differential input resistance. The tens-of-several-kΩ input resistance means it can bring in more gain error and offset if CA-IS1306x devices are applied in measurement where the input signal sources are high-impedance.

The ESD structure of CA-IS1306x supports the absolute maximum analog input voltage (with respect to AGND) to range from AGND – 6 V to AVDD + 0.5 V. To guarantee the long-term reliability and device performance, the differential analog input voltage and the input common-mode voltage of CA-IS1306x must be kept within the specific range.

8.2.2 Signal Transmission Across Isolation Barrier

The CA-IS1306x devices utilize a simple on-off keying (OOK) modulation scheme to transmit the digital bitstream across the SiO_2-based isolation barrier which supports up to 5-kV_{RMS} galvanic isolation between high- and low-voltage domain. The block diagram of an isolation channel is shown in Figure 8-2. As shown in Figure 8-3, the transmitter (TX) modulates the digital bitstream with a high-frequency carrier when the signal is HIGH while sends no signal when the signal is LOW. The receiver (RX) demodulates the signal across the isolation barrier and reproduces the digital bitstream faithfully. The isolation channel adopts fully differential capacitive-coupled structure which is insensitive to common-mode transient noises, thus the CMTI performance can be maximized. This structure and related circuitry also provide low emissions and strong anti-interference capability from magnetic changes.

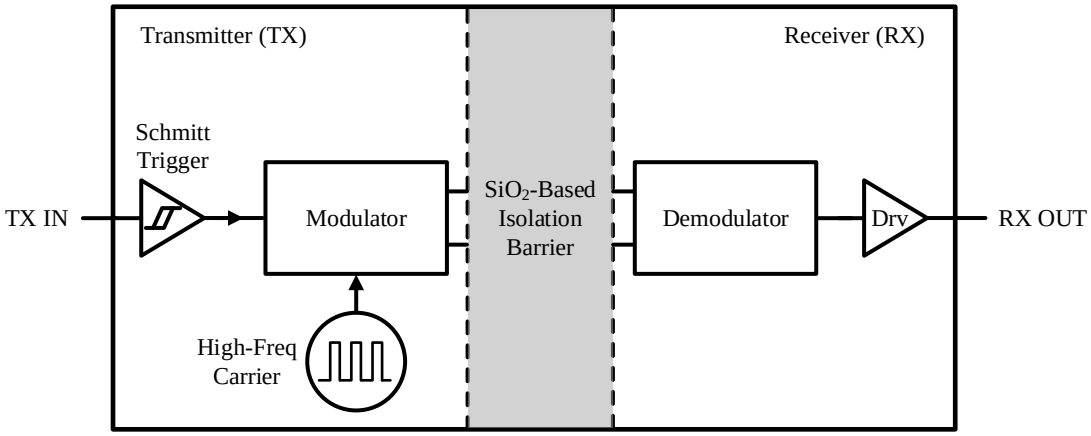


Figure 8-2 Block Diagram of an Isolation Channel

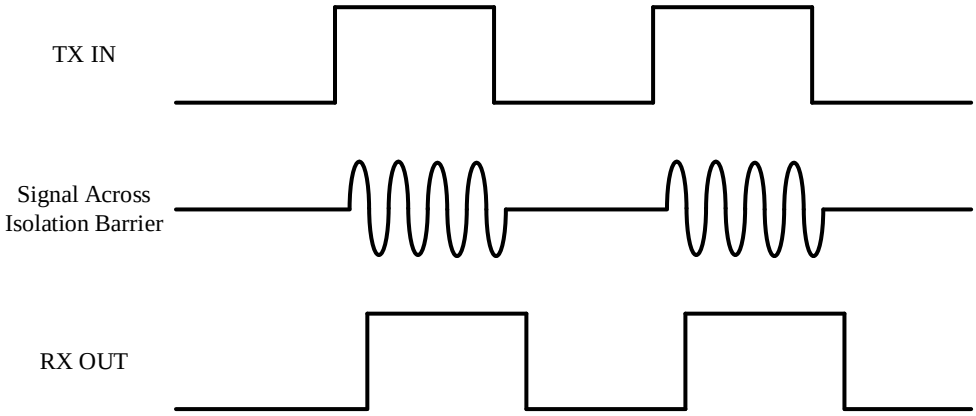


Figure 8-3 Conceptual Operation Waveforms of OOK Modulation Scheme

8.2.3 Digital Output and Encoding

The relationship between the analog input (AINP – AINN) and output of modulator is shown in Figure 8-4. The analog input of 0 V theoretically corresponds to a digital bitstream of ONEs and ZEROs which are 50% of the time. The density of ONEs in the digital output bitstream for certain analog input voltage could be calculated by the following equation:

$$Density|_{ONEs} = (V_{IN} + V_{Clipping}) / (2 \times V_{Clipping}) \quad \textbf{(Eq. 1)}$$

Eq. 1 is true only when the analog input is within the full-scale input range (±320 mV for CA-IS1306x25). If the input voltage exceeds above these ranges, the sigma-delta modulator would be saturated and behave nonlinearly. The output of the modulator clips to only ONEs or ZEROs under these conditions. To be distinguished from the fail-safe output cases, a single ZERO

(the analog input greater than or equal to 320 mV for CA-IS1306x25) or ONE (the analog input less than or equal to –320 mV for CA-IS1306x25) is interpolated into the bitstream every 128 clock cycles (refer to Overrange Output section for more detailed information).

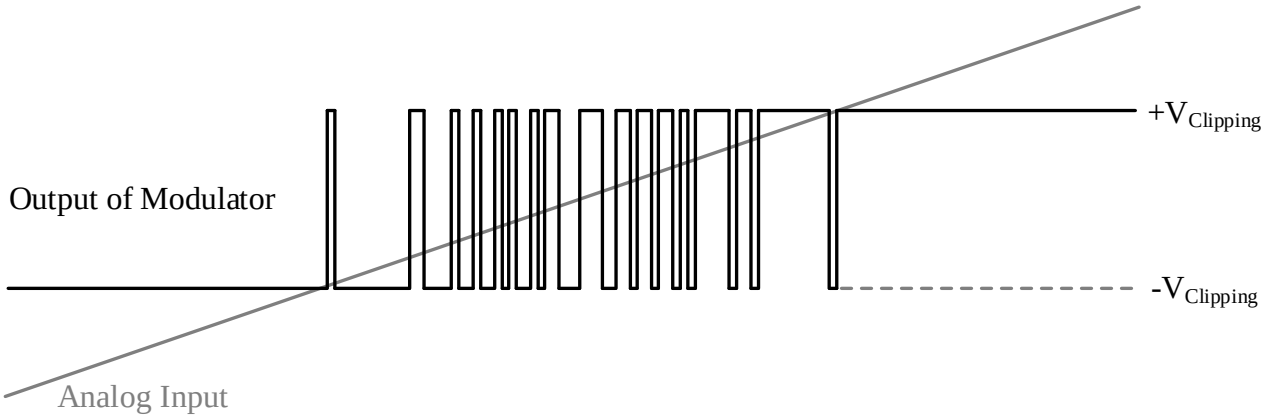


Figure 8-4 Modulator Output of CA-IS1306x versus Analog Input (AINP – AINN)

8.2.4 Fail-Safe Output

The CA-IS1306x devices have fail-safe output function which is activated in two conditions:

- The high-side power supply (AVDD) is missing;
- The common-mode input voltage V_{CM} exceeds the common-mode overvoltage threshold V_{CMOV}.

As shown in Figure 8-5, the DOUT output is held to logic ONE when the input common-mode voltage V_{CM} exceeds V_{CMOV}. In the case of missing high-side power supply (AVDD), the DOUT output is kept to logic ZERO. When both cases occur at the same time, missing high-side power supply (AVDD) has a higher priority, thus the DOUT output is held to logic ZERO. This function indicates exceptional situations at high side which contributes to fault diagnostics and system safety.

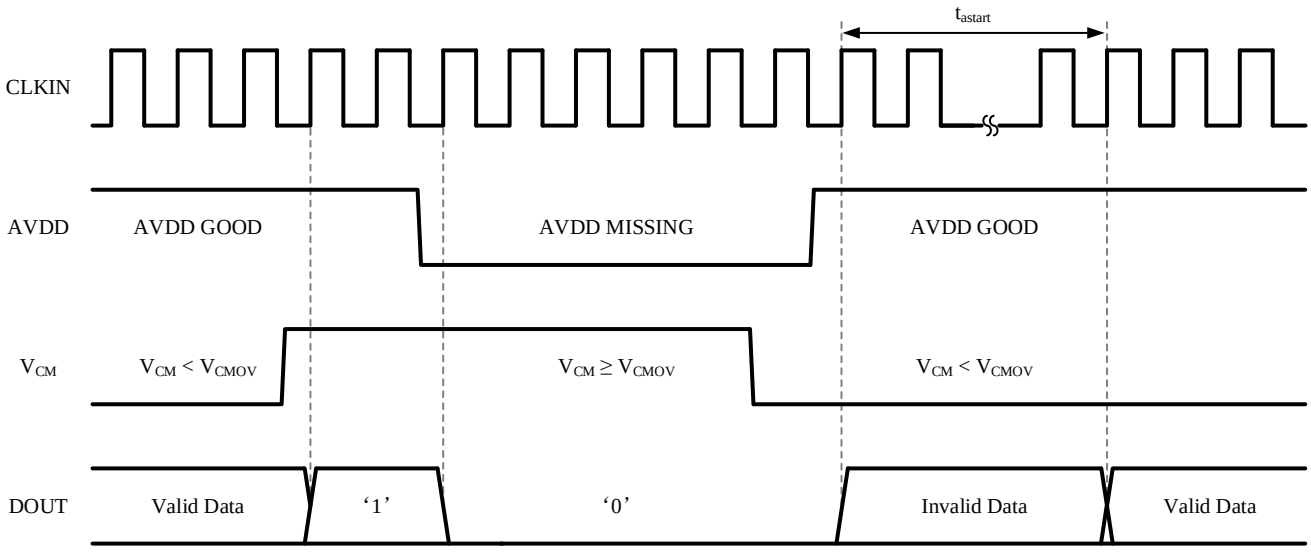


Figure 8-5 Fail-Safe Output Waveforms of CA-IS1306x

8.2.5 Overrange Output

As shown in Figure 8-6, the CA-IS1306x devices generate a single ZERO every 128 clock cycles when the analog input $V_{IN} \geq |V_{Clipping}|$ while a single ONE when $V_{IN} \leq -|V_{Clipping}|$. This overrange output behavior could be distinguished from the fail-safe output behavior and thus be recognized at the system level.

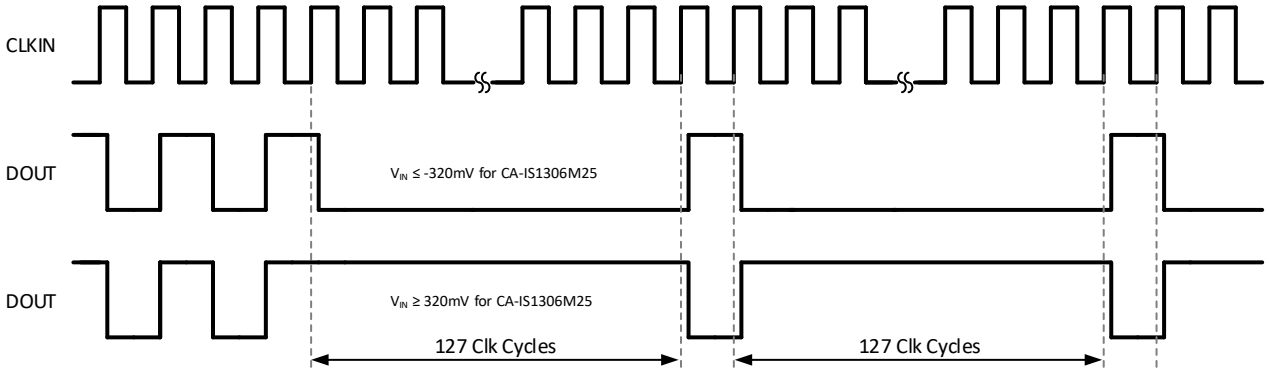


Figure 8-6 Overrange Output Waveforms of CA-IS1306x

9 Application and Implementation

9.1 Typical Application for Current Sensing

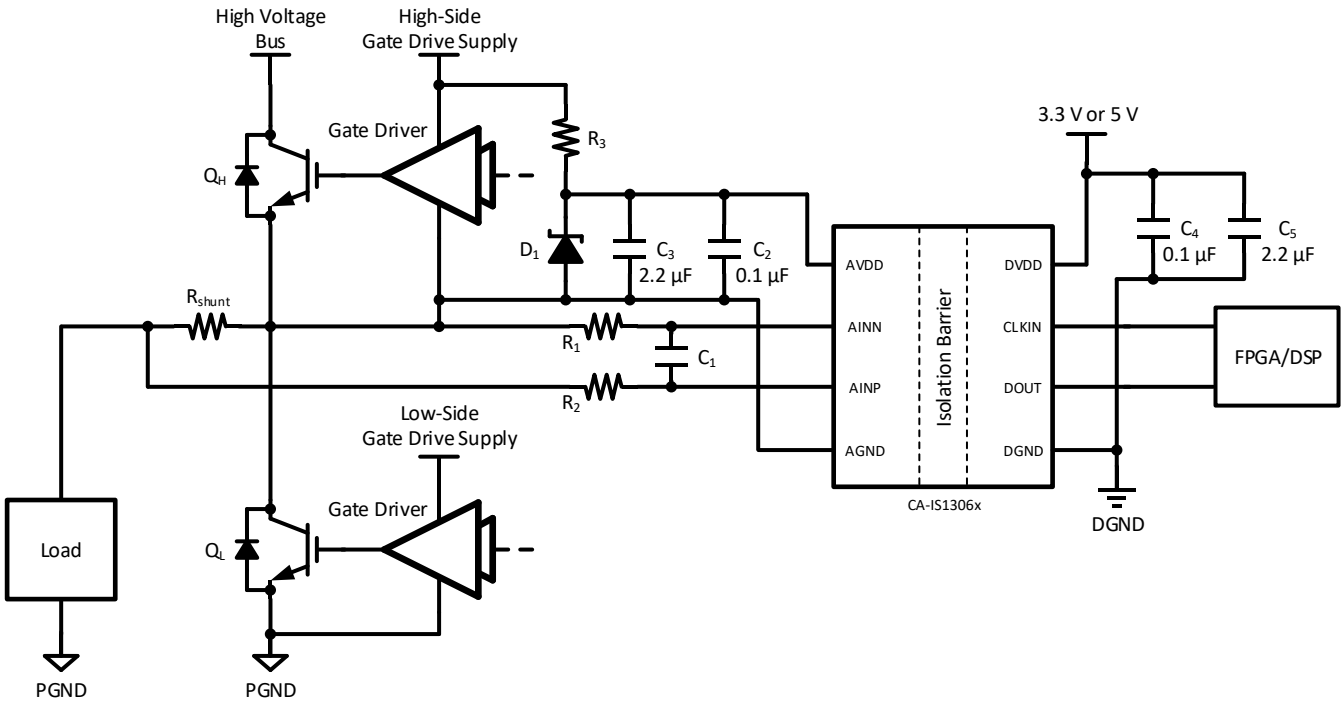


Figure 9-1 Typical Application for Current Sensing

The typical application for current sensing is shown in Figure 9-1. The CA-IS1306x device is used to amplify the voltage across the shunt resistor (R_{shunt}), convert the analog signal into digital bitstream by the sigma-delta modulator and transmit it to the low-voltage side for control circuit to process. The differential input and the high CMTI of CA-IS1306x ensure the reliable and accurate measurement in the high-noise and high-power switching applications such as industrial motor drives. The voltage of R_{shunt} with respect to PGND varies from 0 V to the high voltage bus when switching, thus isolation is required. The CA-IS1306x devices support up to 5-kV_{RMS} galvanic isolation, making them suitable for these high-voltage industrial applications.

In a three-phase motor drive application, this circuit could be repeated three times and one for each phase in order to measure each phase current.

9.2 Choose Proper R_{shunt}

The value chosen of shunt resistor is a trade-off between power dissipation and measuring accuracy. Small value resistors minimize power dissipation, while large value resistors take advantage of the full performance input range of the sigma-delta modulator.

Consider the following restrictions to choose proper value of the shunt resistor R_{shunt}:

- The voltage drop across R_{shunt} caused by the nominal measured current is within the linear differential input voltage range V_{FSR};
- The voltage drop across R_{shunt} caused by the maximum allowed current must not exceed the maximum input voltage before clipping output $|V_{Clipping}|$.

For best performance, place the shunt resistor close to the inputs of CA-IS1306x and keep the layout of both connections symmetrical. This ensures that any noises occurring at high side are coupled equally to the inputs and would be rejected as a

common-mode signal. Kelvin connection is recommended between R_{shunt} and the inputs of CA-IS1306x to remove the impact from any voltage drops across the trace and leads.

9.3 Input Filter

A first-order passive RC low-pass filter could be placed between R_{shunt} and the inputs to filter high-frequency noise. Choose R_1 = R_2 = 10 Ω and C_1 = 20 nF could provide a cutoff frequency of approximately 400 kHz. R_1 and R_2 should be low-value enough compared to the input impedance of CA-IS1306x to reduce gain error.

9.4 Power Supply Recommendations

The high-side power supply of CA-IS1306x could be generated directly derived from the high-side gate drive power supply by utilizing a Zener diode (D_1) to produce a 3.3-V or 5-V (±10%) voltage. And a low-ESR decoupling capacitor of 0.1 µF (C_2) is recommended to place as close as possible to the AVDD pin of CA-IS1306x. Additional capacitor (C_3) with a value ranging from 2.2 µF to 10 µF is recommended for better filtering to the high-side power-supply path.

Similarly, a 0.1-µF decoupling capacitor (C_4) followed by an additional capacitor (C_5) from 2.2 µF to 10 µF should be placed as close as to the DVDD pin of CA-IS1306x to filter the low-side power supply path.

9.5 Digital Filter

The output of the CA-IS1306x is a 1-bit digital bitstream which contains abundant high-frequency shaped quantization noise due to the mechanism of sigma-delta modulator. Off-chip digital filter is required (implemented in controllers such as FPGA or DSP) to filter out high-frequency noise and obtain a digital word. A $sinc^3$ filter is recommended mainly for two reasons: one for its simplicity and lower hardware cost, the other is that this filter is one order higher than the 2^{nd}-order sigma-delta modulator utilized in CA-IS1306x, which could reconstruct the original input signal information from the bitstream. Eq. 2 describes the transfer function of a $sinc^3$ filter.

$$H(Z)=\left[\frac{1}{DR}\frac{\left(1-Z^{-DR}\right)}{\left(1-Z^{-1}\right)}\right]^3 \quad \textbf{(Eq. 2)}$$

where Z is the sample and DR is the decimation rate.

The decimation rate (DR) is the ratio between the modulator clock frequency f_{CLKIN} and throughput rate of the $sinc^3$ filter f_{DATA}, which is also called oversampling rate (OSR).

$$DR = OSR = f_{CLKIN}/f_{DATA} \quad \textbf{(Eq. 3)}$$

The output data width is expressed in Eq. 4.

$$Data\ Width = 3 \times \log_2 DR \quad \textbf{(Eq. 4)}$$

All the characterization in this datasheet is tested by utilizing a $sinc^3$ filter with an oversampling ratio (OSR) of 256 and intercepting the 16 most significant bits as a 16-bit result.

The characteristics of the $sinc^3$ filter are summarized in Table 9-1. As the decimation rate increases, the output data width from the $sinc^3$ filter also increases, while the throughput rate decreases, resulting in higher SNR performance. Thus, there exists a trade-off between data rate and conversion accuracy.

Table 9-1 Characteristics of sinc³ Filter with 20-MHz f_{CLKIN}

Decimation Rate (DR)	f_{DATA} (kHz)	Output Data Width (Bits)	Filter Response (kHz)
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

9.6 Error Analysis in Voltage Sensing

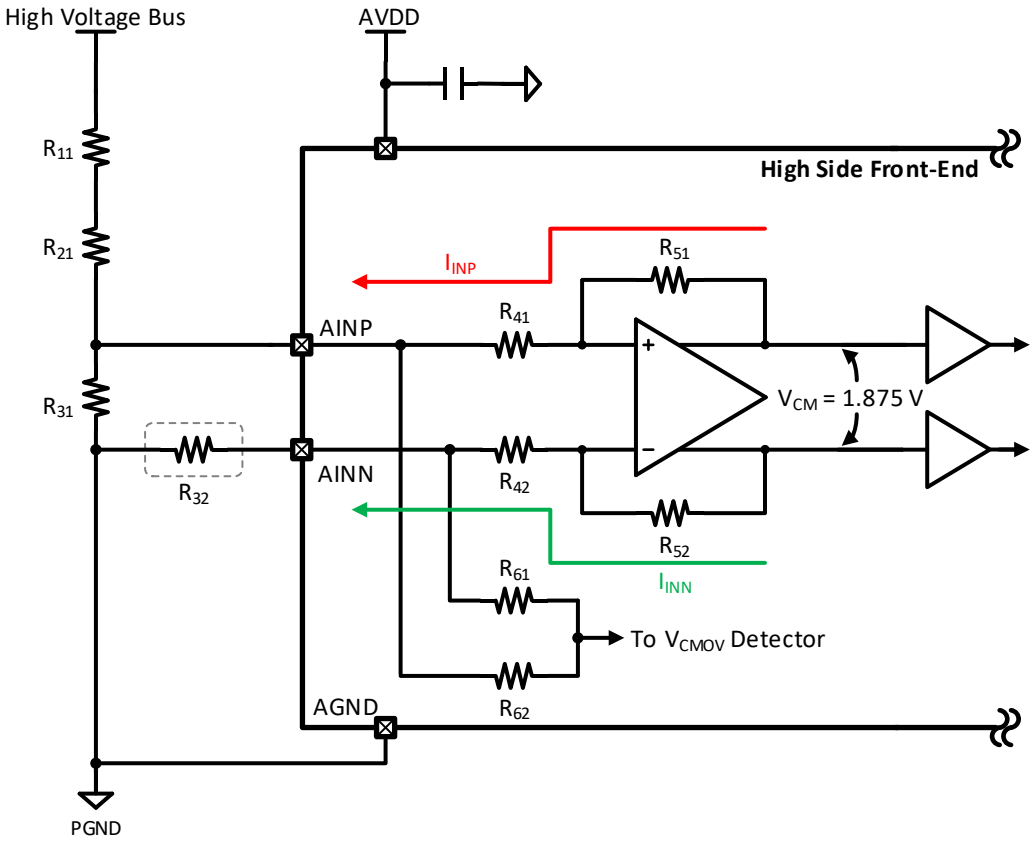


Figure 9-2 Typical Application for Voltage Sensing

The CA-IS1306x devices may also be used in the applications of voltage sensing as shown in Figure 9-2. The resistors R_{11}, R_{21} and R_{31} make up the resistor divider to scale down the high voltage from bus. Typically, the value of R_{11} and R_{21} is much larger than R_{31} to keep the input voltage of CA-IS1306x within the specific range.

In CA-IS1306x, resistors R_{41} and R_{51} (or R_{42} and R_{52}) are used to set the gain of front-end amplifier. The typical values are $R_{41} = R_{42} = 12.5$ kΩ, and $R_{51} = R_{52} = 50$ kΩ for CA-IS1306x25. Resistors R_{61} and R_{62} are used to sense the common-mode voltage of the input in CA-IS1306x. The typical values are $R_{61} = R_{62} = 100$ kΩ.

First, consider the situation in which R_{32} is not used. Additional gain error and offset would arise in these applications for CA-IS1306x. On the one hand, the limited input impedance of CA-IS1306x is parallel with the external sensing resistor R_{31}, resulting in impedance change and thus additional gain error. On the other hand, the output common-mode voltage V_{CM} of the front-end differential amplifier in CA-IS1306x is biased to 1.875V, which would generate bias current I_{INP} and I_{INN} flowing through the front-

end resistor network. The bias current I_{INP} also flows through R_{31} while I_{INN} flows directly to PGND in the case of omitting R_{32}, which results in unbalance and thus additional offset.

To eliminate the effect of the bias current, resistor R_{32} equal to sensing resistor R_{31} is recommended to be added between VINN and PGND. The resistor R_{31} would bring in additional gain error E_{GA} and could be calculated as Eq. 5 describes.

$$E_{GA} = R_{31} / (R_{31} + R_{41}) \quad \textbf{(Eq. 5)}$$

To reduce the effect of this gain error, the value of R_{31} should be chosen much smaller compared to R_{41}. And this gain error could also be minimized by the system-level gain calibration.

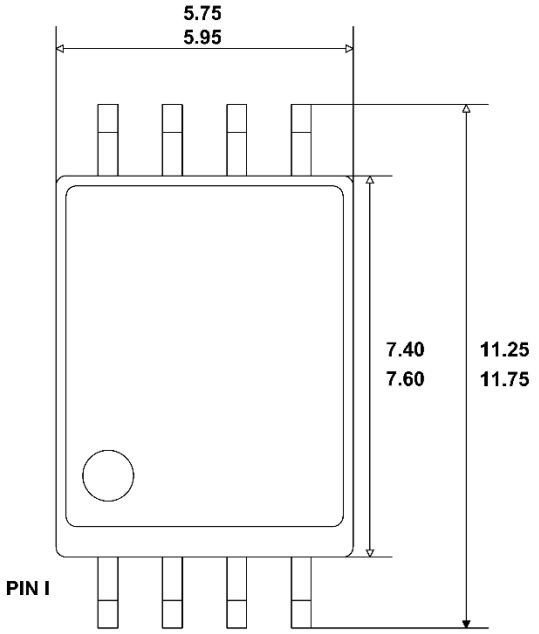
9.7 Caution

Do not leave the inputs of CA-IS1306x floating. If the AINP and AINN are left floating, the input common-mode voltage would be pulled to a high level by internal bias, which could activate the fail-safe mode under certain power supply and may lead to system-level abnormal reaction (refer to Fail-Safe Output for detailed information).

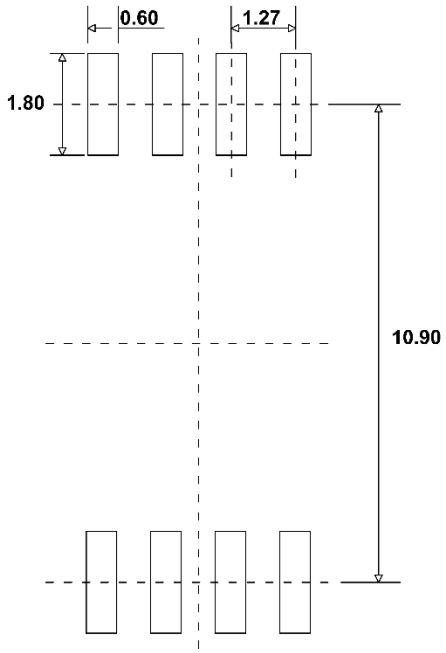
10 Package Information

10.1 8-Pin Wide Body SOIC Package

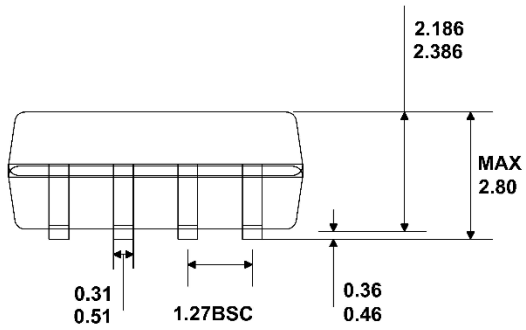
The figure below illustrates the package details and the recommended land pattern details for the CA-IS1306x isolated sigma-delta modulator in an 8-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.



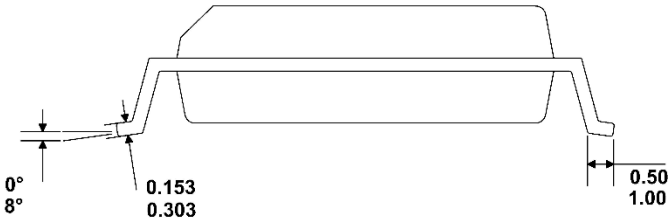
TOP VIEW



RECOMMENDED LAND PATTERN



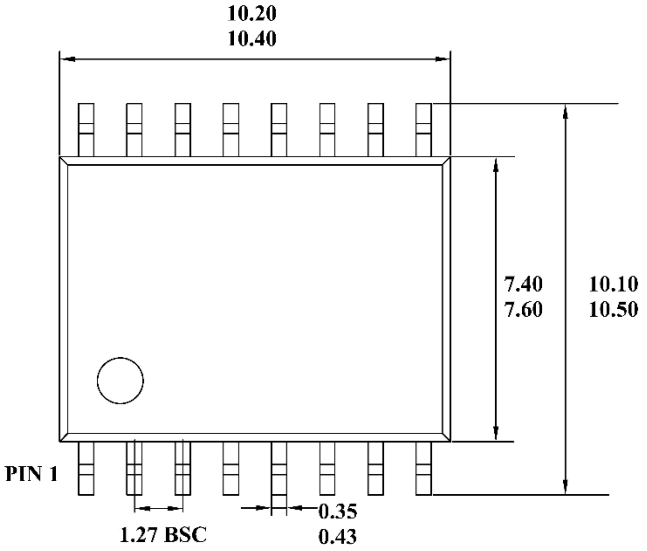
FRONT VIEW



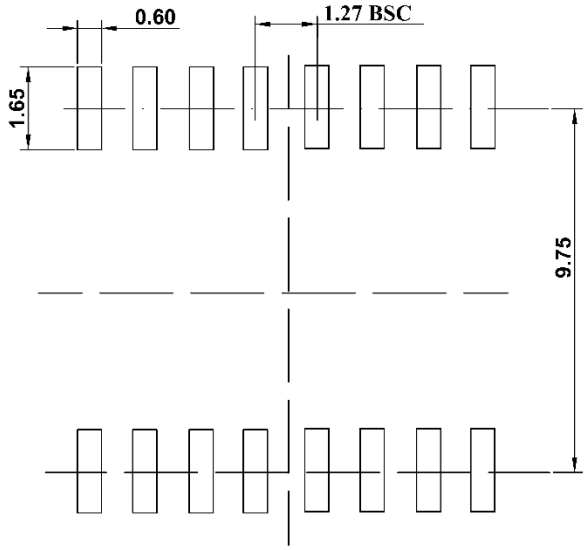
LEFT-SIDE VIEW

10.2 16-Pin Wide Body SOIC Package

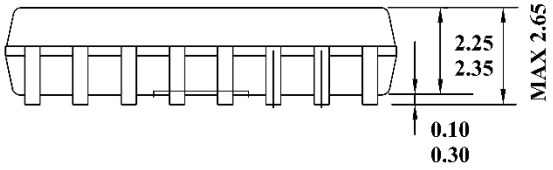
The figure below illustrates the package details and the recommended land pattern details for the CA-IS1306x isolated sigma-delta modulator in a 16-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.



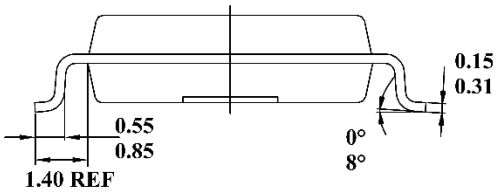
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

11 Soldering Information

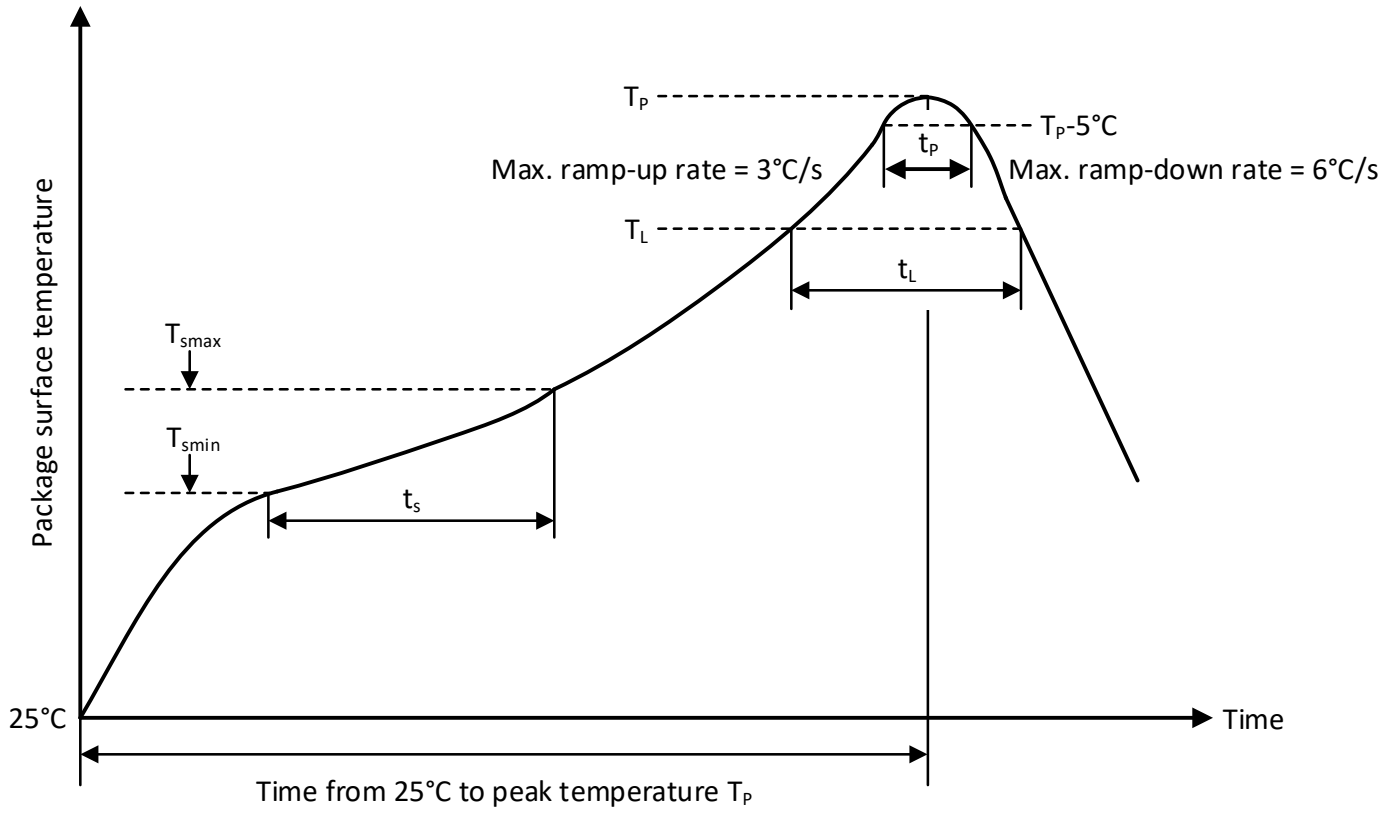


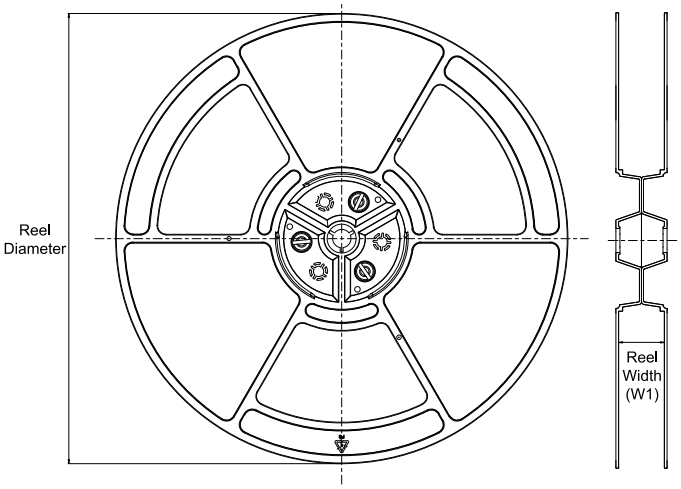
Figure 11-1 Soldering Temperature Curve

Table 11-1 Soldering Temperature Parameters

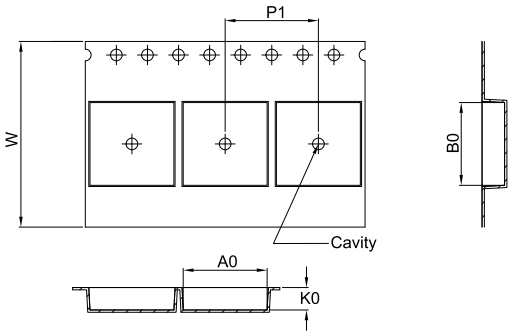
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

12 Tape and Reel Information

REEL DIMENSIONS

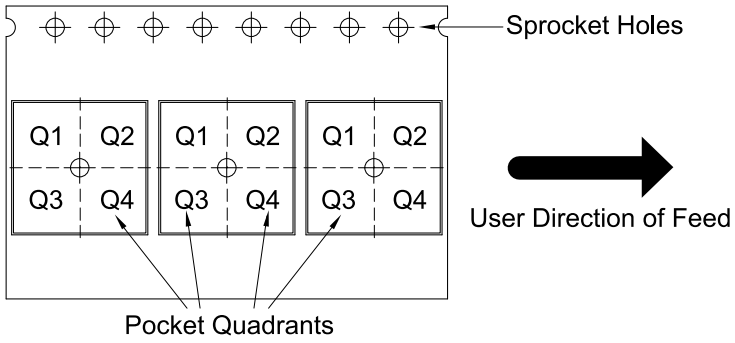


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS1306M25G	SOIC	G	8	1000	330	16.4	11.95	6.15	3.2	16.0	16.0	Q1
CA-IS1306AM25W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS1306M25W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

13 Important Notice

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