CA-IS303x 1.1-Gbps Dual-Channel LVDS Isolators

1 Key Features

- Passes EN55032 Class B Radiated Emissions Limits with Dual-Channel Configuration
- 3.75kV$_{RMS}$ Isolation Rating
- Supply Voltage: 2.5V or 3.3V
- High CMTI: >25kV/μs
- Fail-Safe Output High for Open, Short, and Terminated Input Conditions (CA-IS3031T/CA-IS3032T)
- Supports up to 1.1-Gbps Data Rate
  - 3.5-ns Typical Propagation Delay
  - 5-ps Typical (RMS) Random Jitter
  - 120-ps Typical Peak-to-Peak Total Jitter
- Power Supply Ripple Rejection and Glitch Immunity: −80dBc
- ±6-kV IEC 61000-4-2 ESD Protection on LVDS Ports
- 16-Pin or 20-Pin Wide-Body SOIC Package
- Extended Industrial Temperature Range: –40°C to 125°C
- Safety-Related Certifications (Pending):
  - 3.75-kV$_{RMS}$ Isolation for 1 Minute per UL 1577
  - 5300-V$_{PK}$ V$_{IOTM}$ per DIN EN IEC 60747-17 (VDE 0884-17):2021-10
  - CQC Certification According to GB4943.1-2022
  - TUV Certification

2 Applications

- Communication Equipment
- Enterprise System
- Industrial High-Speed Analog-Front Module
- Industrial High-Speed Clock and Data Links

3 Description

The CA-IS303x devices are high-performance, dual-channel, isolated low-voltage differential signaling (LVDS) buffers with up to 3.75-kV$_{RMS}$ isolation rating and up to 1.1-Gbps ultra-fast data rate. These devices are compliant with TIA/EIA-644-A LVDS standard and offer all possible unidirectional channel configurations to accommodate any 2-channel isolated LVDS I/O applications. The CA-IS3030 features two channels transferring LVDS signals in one direction; The CA-IS3031 and CA-IS3032 devices have 2 channels with 1 channel in each direction.

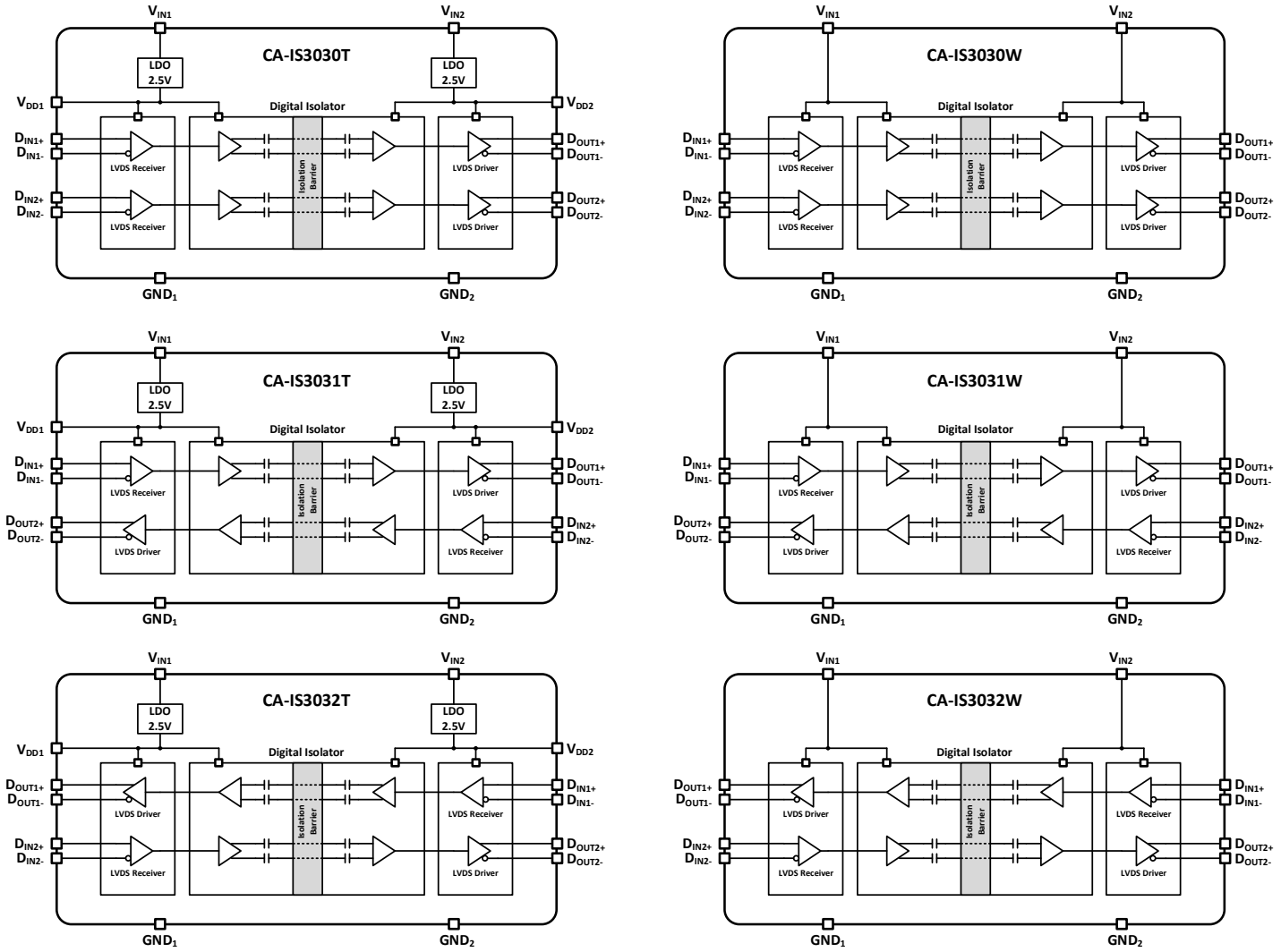
The CA-IS303xT devices feature internal LDO. When operating from 3.3V power supply, the integrated LDO generates 2.5V regulated voltage from 3.3V input for LVDS and isolator circuits. The CA-IS303xT LVDS isolator accepts both 2.5V and 3.3V supplies. When operating from 2.5V power supply, connect V$_{DDx}$ to V$_{INx}$ to bypass internal LDO. The CA-IS303xW devices do not have V$_{DDx}$ pins which are powered directly from V$_{INx}$ pins. The CA-IS3031T/CA-IS3032T feature a fail-safe mechanism to ensure a Logic 1 on the corresponding LVDS driver output when the inputs are floating, shorted, or terminated, but not driven.

The CA-IS303x devices are available in 16-pin and 20-pin wide-body SOIC package, and specified over extended industrial temperature range of –40°C to +125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS3030W CA-IS3031W CA-IS3032W	SOIC16-WB (W)	10.30mm × 7.50mm
CA-IS3030T CA-IS3031T CA-IS3032T	SOIC20-WB (T)	12.75mm × 7.50mm

Simplified Block Diagram



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Number of Channels	Forward-Direction Channels	Reverse-Direction Channels	Isolation Rating (V_{RMS})	Package
CA-IS3030W	2	D1 & D2	NA	3750	SOIC16-WB (W)
CA-IS3031W	2	D1	D2	3750	SOIC16-WB (W)
CA-IS3032W	2	D2	D1	3750	SOIC16-WB (W)
CA-IS3030T	2	D1 & D2	NA	3750	SOIC20-WB (T)
CA-IS3031T	2	D1	D2	3750	SOIC20-WB (T)
CA-IS3032T	2	D2	D1	3750	SOIC20-WB (T)

Table of Contents

5 Pin Descriptions and Functions

5.1 CA-IS303xW

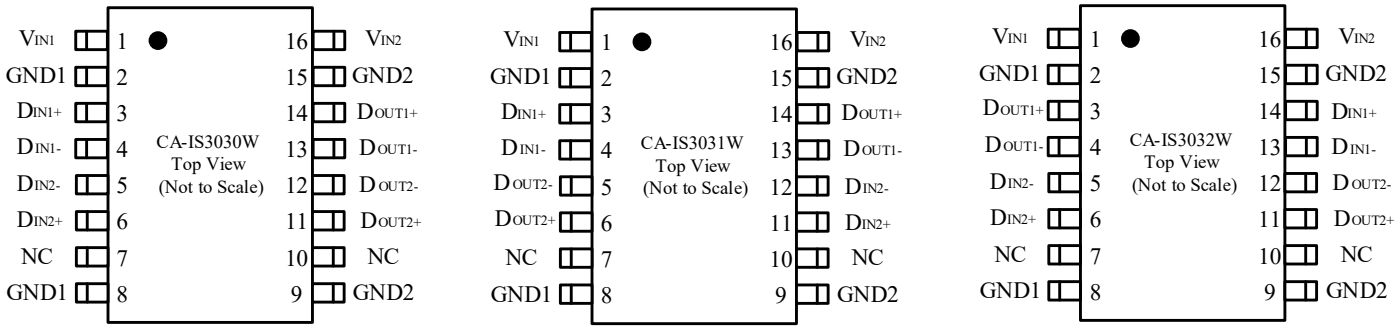


Figure 5-1 Pin Configuration

Table 5-1 Pin Description and Functions

NAME	PIN NUMBER			DESCRIPTION
	CA-IS3030W	CA-IS3031W	CA-IS3032W	
V_{IN1}	1	1	1	3.3V power supply input for side 1. Bypass V_{IN1} to GND1 with 1μF capacitor as close to the device as possible.
GND1	2, 8	2, 8	2, 8	Ground reference for side 1.
D_{IN1+}	3	3	14	Channel 1 noninverting LVDS input.
D_{IN1-}	4	4	13	Channel 1 inverting LVDS input.
D_{IN2-}	5	12	5	Channel 2 inverting LVDS input.
D_{IN2+}	6	11	6	Channel 2 noninverting LVDS input.
NC	7, 10	7, 10	7, 10	No connection.
GND2	9, 15	9, 15	9, 15	Ground reference for side 2.
D_{OUT2+}	11	6	11	Channel 2 noninverting LVDS output.
D_{OUT2-}	12	5	12	Channel 2 inverting LVDS output.
D_{OUT1-}	13	13	4	Channel 1 inverting LVDS output.
D_{OUT1+}	14	14	3	Channel 1 noninverting LVDS output.
V_{IN2}	16	16	16	3.3V power supply input for side 2. Bypass V_{IN2} to GND2 with 1μF capacitor as close to the device as possible.

5.2 CA-IS303xT

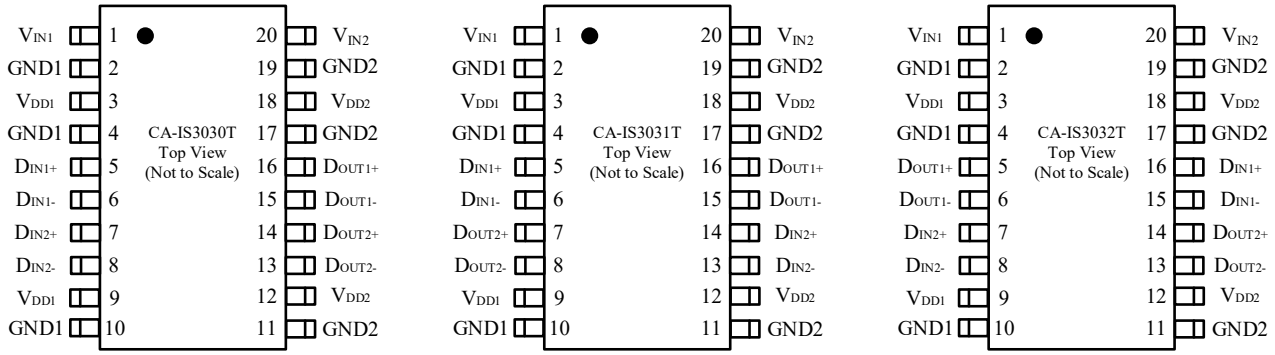


Figure 5-2 Pin Configuration

Table 5-2 Pin Description and Functions

NAME	PIN NUMBER			DESCRIPTION
	CA-IS3030T	CA-IS3031T	CA-IS3032T	
V_{IN1}	1	1	1	3.3V power supply input for side 1. Bypass V_{IN1} to GND1 with 1μF capacitor as close to the device as possible. For 2.5V power supply input, connect V_{IN1} to V_{DD1}.
GND1	2, 4, 10	2, 4, 10	2, 4, 10	Ground reference for side 1.
V_{DD1}	3, 9	3, 9	3, 9	2.5V power supply input for side 1. Bypass V_{DD1} to GND1 with 0.1μF capacitor as close to the device as possible. For 3.3V power supply input, bypass pin 3 to GND1 with 1μF capacitor.
D_{IN1+}	5	5	16	Channel 1 noninverting LVDS Input
D_{IN1-}	6	6	15	Channel 1 inverting LVDS input.
D_{IN2+}	7	14	7	Channel 2 noninverting LVDS input.
D_{IN2-}	8	13	8	Channel 2 inverting LVDS input.
GND2	11, 17, 19	11, 17, 19	11, 17, 19	Ground reference for side 2.
V_{DD2}	12, 18	12, 18	12, 18	2.5V power supply input for side 2. Bypass V_{DD2} to GND1 with 0.1μF capacitor as close to the device as possible. For 3.3V power supply input, bypass pin 18 to GND1 with 1μF capacitor.
D_{OUT2-}	13	8	13	Channel 2 inverting LVDS output.
D_{OUT2+}	14	7	14	Channel 2 noninverting LVDS output.
D_{OUT1-}	15	15	6	Channel 1 inverting LVDS output.
D_{OUT1+}	16	16	5	Channel 1 noninverting LVDS output.
V_{IN2}	20	20	20	3.3V power supply input for side 2. Bypass V_{IN2} to GND2 with 1μF capacitor as close to the device as possible. For 2.5V power supply input, connect V_{IN2} to V_{DD2}.

6 Specifications

6.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{IN1}, V_{IN2}	Supply voltage[2]	–0.3	6.5	V
D_{INx+}, $D_{INx–}$	Input voltage[2]	–0.3	V_{DD} + 0.3	V
D_{OUTx+}, $D_{OUTx–}$	Output voltage[2]	–0.3	V_{DD} + 0.3	V
T_J	Junction Temperature	–40	150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the local ground (GND1 or GND2) and are peak voltage values.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±4	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±2	
		Contact discharge, per IEC 61000-4-2, LVDS pins to isolated GNDx across isolation barrier	±6	

6.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
Power Supply for CA-IS303xT					
V_{IN1}	Supply voltage of side 1, with respect to GND1	3.0	3.3	3.6	V
V_{IN2}	Supply voltage of side 2, with respect to GND2	3.0	3.3	3.6	V
V_{DD1}	LDO is bypassed, connect V_{IN1} to V_{DD1}, with respect to GND1	2.375	2.5 or 3.3	3.6	V
V_{DD2}	LDO is bypassed, connect V_{IN2} to V_{DD2}, with respect to GND2	2.375	2.5 or 3.3	3.6	V
Power Supply for CA-IS303xW					
V_{IN1}	Supply voltage of side 1, with respect to GND1	2.375	2.5 or 3.3	3.6	V
V_{IN2}	Supply voltage of side 2, with respect to GND2	2.375	2.5 or 3.3	3.6	V
Other					
R_L	TX far-end differential termination		100		Ω
DR	Data Rate			1.1	Gbps
T_A	Ambient Temperature	–40		125	°C
T_J	Junction Temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC		PACKAGE		UNIT
		SOIC20-WB (T)	SOIC16-WB (W)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50	83.4	°C/W

6.5 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE W/T	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	19	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150V_{RMS}	I-IV	
		Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	637	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	450	V_{RMS}
		DC voltage	637	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	5300	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	6500	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin(2πft), f = 1MHz	1	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	3750	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

6.6 Safety-Related Certifications

VDE (Pending)	UL (Pending)	CQC (Pending)	TUV (Pending)
Certified according to DIN EN IEC 60747-17(VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
Basic insulation V_{IORM}: 637V_{PK} V_{IOTM}: 5300V_{PK} V_{IOSM}: 6500V_{PK}	Single protection: 3750V_{RMS}	Basic insulation (Altitude ≤ 5000m)	EN 61010-1: 3750V_{RMS} EN 62368-1: 3750V_{RMS}
Certification number: Pending	Certification number: Pending	Certification number: Pending	Client reference number: 2253313

6.7 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CA-IS303xW						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 83.4°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			416	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 83.4°C/W, T_J = 150°C, T_A = 25°C			1498	mW
T_S	Maximum safety temperature				150	°C
CA-IS303xT						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 50°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			694	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 50°C/W, T_J = 150°C, T_A = 25°C			2500	mW
T_S	Maximum safety temperature				150	°C

6.8 Electrical Characteristics

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 2.5V for CA-IS303xT and V_{IN1} = V_{IN2} = 2.5V for CA-IS303xW (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input (LVDS RX)						
V_{TH}	Differential input high threshold	See Figure 7-3			100	mV
V_{TL}	Differential input low threshold		–100			mV
$\|V_{ID}\|$	Differential input voltage		100			mV
V_{IC}	Input common-mode voltage		$0.5\|V_{ID}\|$		$2.4 – 0.5\|V_{ID}\|$	V
I_{IH}, I_{IL}	Input current	$D_{INx±}$ = V_{DD} or 0V, other inputs = 1.2V, V_{DD} = 2.5V or 0V	–5		5	µA
$C_{INx±}$	Differential input capacitance [1]	$D_{INx±} = 0.4\sin(30 \times 10^6 \pi t) + 0.5V$, other inputs = 1.2V		3		pF
Output (LVDS TX)						
$\|V_{OD}\|$	Differential output voltage	See Figure 7-1 and Figure 7-2, R_L = 100Ω	250	330	450	mV
$\|\Delta V_{OD}\|$	Magnitude change of V_{OD}		50	60	70	mV
V_{OS}	Offset voltage	See Figure 7-1, R_L = 100Ω	1.125	1.21	1.375	V
ΔV_{OS}	Magnitude change of V_{OS}				50	mV
$V_{OS(PP)}$	V_{OS} peak-to-peak voltage[1]			90		mV
I_{OS}	Output short-circuit current	$D_{OUTx±}$ = 0V		–12	–20	mA
		$\|V_{OD}\|$ = 0V		3.5	7	
$C_{OUTx±}$	Differential output capacitance[1]	$D_{OUTx±} = 0.4\sin(30 \times 10^6 \pi t) + 0.5V$, other inputs = 1.2V, V_{DD1} or V_{DD2} = 0V		5		pF
Power Supply						
I_{DD1}, I_{IN1}, I_{DD2}, or I_{IN2}	Supply Current (CA-IS3031/CA-IS3032)	No output load, inputs with 100Ω, no applied $\|V_{ID}\|$	20	42	60	mA
		All outputs loaded, R_L = 100Ω, f = 550MHz	20	55	72	
I_{DD1}, I_{IN1}, I_{DD2}, or I_{IN2}	Supply Current (CA-IS3030)	No output load, inputs with 100 Ω, $\|V_{ID}\|$ = 200mV	20	45	60	mA
		All outputs loaded, R_L = 100Ω, f = 550MHz	20	59	72	
V_{DD1} or V_{DD2}	LDO output voltage[2]		2.375	2.5	2.625	V
PSRR	Power supply rejection ratio	Phase spur level on $D_{OUTx±}$ with 550MHz clock on $D_{INx±}$ and applied ripple of 100 kHz, 100 mV_{PP} on a 2.5V supply to V_{DD1} or V_{DD2}		–80		dBc
|CMTI|	Common mode transient immunity [3]	$\|V_{CM}\|$ = 1000V, transient magnitude = 800V	25	50		kV/µs

NOTE:

1. Guaranteed by design and characterization.
2. Only for CA-IS303xT.
3. |CMTI| is the maximum common-mode voltage slew rate that can be sustained while maintaining any D_{OUTx+}/D_{OUTx-} pin in the same state as the corresponding D_{INx+}/D_{INx-} pin (no change on output), or producing the expected transition on any D_{OUTx+}/D_{OUTx-} pin if the applied common-mode transient edge is coincident with a data transition on the corresponding D_{INx+}/D_{INx-} pin. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

6.9 Timing Characteristics[1]

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 2.5V for CA-IS303xT and V_{IN1} = V_{IN2} = 2.5V for CA-IS303xW (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay						
t_{PLH}, t_{PHL}	Propagation Delay	See Figure 7-4, from any D_{INx+}/D_{INx-} to D_{OUTx+}/D_{OUTx-}		3.5		ns
Skew						
$t_{SK(D)}$	Duty cycle output skew $\lvert t_{PLH} - t_{PHL} \rvert$			70		ps
$t_{SK(CH)}$	Channel-to-channel output skew[2]	CA-IS3030 only		150		ps
				200		
$t_{SK(PP)}$	Part-to-part skew[3]	CA-IS3030 only		300		ps
		CA-IS3030, CA-IS3031, CA-IS3032, or combinations		350		
Jitter[4]						
$t_{RJ(RMS)}$	Random output jitter[4], RMS(1σ)	D_{OUTx+} /D_{OUTx-}		5		ps(RMS)
$t_{DJ(PP)}$	Deterministic output jitter[5]	1.1Gbps, 2^{23} – 1 PRBS		50		ps
$t_{TJ(PP)}$	Total jitter at BER 1 × 10^{-12}	1.1Gbps, 2^{23} – 1 PRBS[6]		120		ps
t_{ADDJ}	Additive phase jitter	100Hz to 100kHz, f_{OUT} = 10MHz[7]		500		fs(RMS)
		12kHz to 20MHz, f_{OUT} = 550MHz[8]		500		
Other						
t_R, t_F	Output rise/fall time	See Figure 7-4, any D_{OUTx+}/ D_{OUTx-}, 20% to 80%, R_L = 100Ω, C_L = 5pF		300		ps
t_{FSH}, t_{FSL}	Fail-safe delay[9]	Only for CA-IS3031T and CA-IS3032T, See Figure 7-4 and Figure 7-5, R_L = 100Ω		1	1.5	µs
DR_{max}	Maximum data rate[10]		1.1			Gbps

NOTE:

1. Guaranteed by design and characterization.
2. Channel-to-channel or output skew is the difference between the largest and smallest values of t_{PLHx} within a device or the difference between the largest and smallest values of t_{PHLx} within a device, whichever of the two is greater.
3. Part-to-part output skew is the difference between the largest and smallest values of t_{PLHx} across multiple devices or the difference between the largest and smallest values of t_{PHLx} across multiple devices, whichever of the two is greater.
4. Guaranteed by design and characterization.
5. $t_{DJ(PP)}$ includes the jitter caused by $t_{SK(D)}$.
6. Using the formula $t_{TJ(PP)}$ = 14 × $t_{RJ(RMS)}$ + $t_{DJ(PP)}$.
7. With input phase jitter of 250fs(RMS) subtracted.
8. With input phase jitter of 100fs(RMS) subtracted.
9. The fail-safe delay is the delay before $D_{OUTx±}$ is switched high to reflect idle input to $D_{INx±}$ ($\lvert V_{ID} \rvert$ < 100mV, open or short/terminated input condition).
10. Guaranteed by bench.

7 Parameter Measurement Information

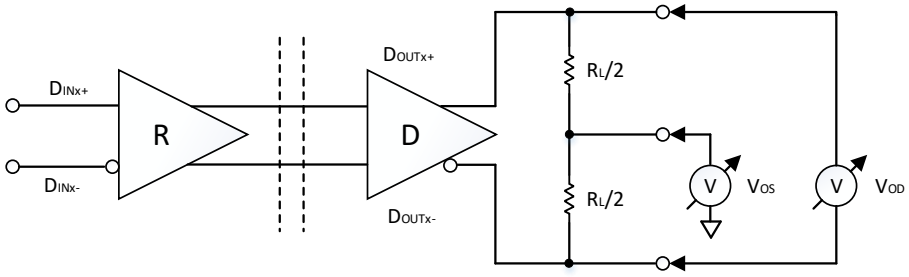


Figure 7-1 Driver Test Circuit

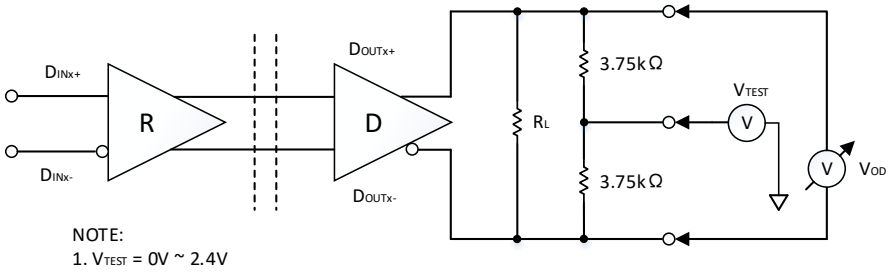


Figure 7-2 Driver Test Circuit With Full Load Across Common-Mode Range

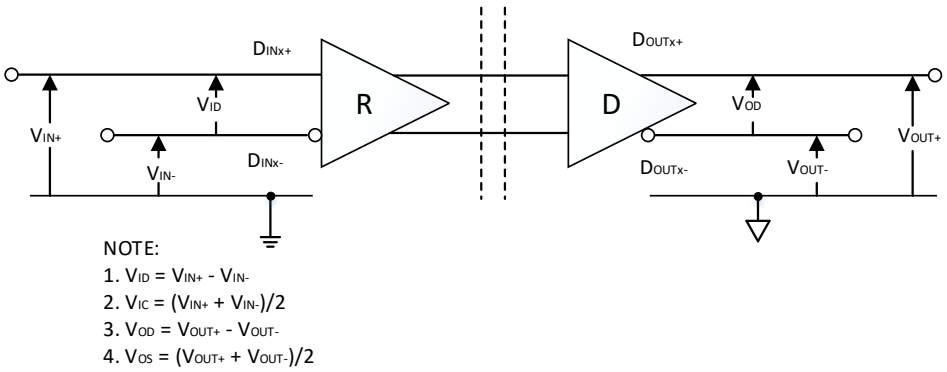
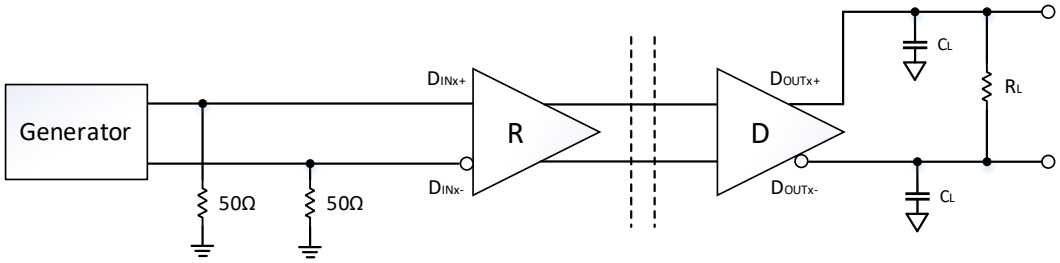


Figure 7-3 Voltage Definition



NOTE:
1. C_L includes probe and stray capacitance.

Figure 7-4 Timing Test Circuit

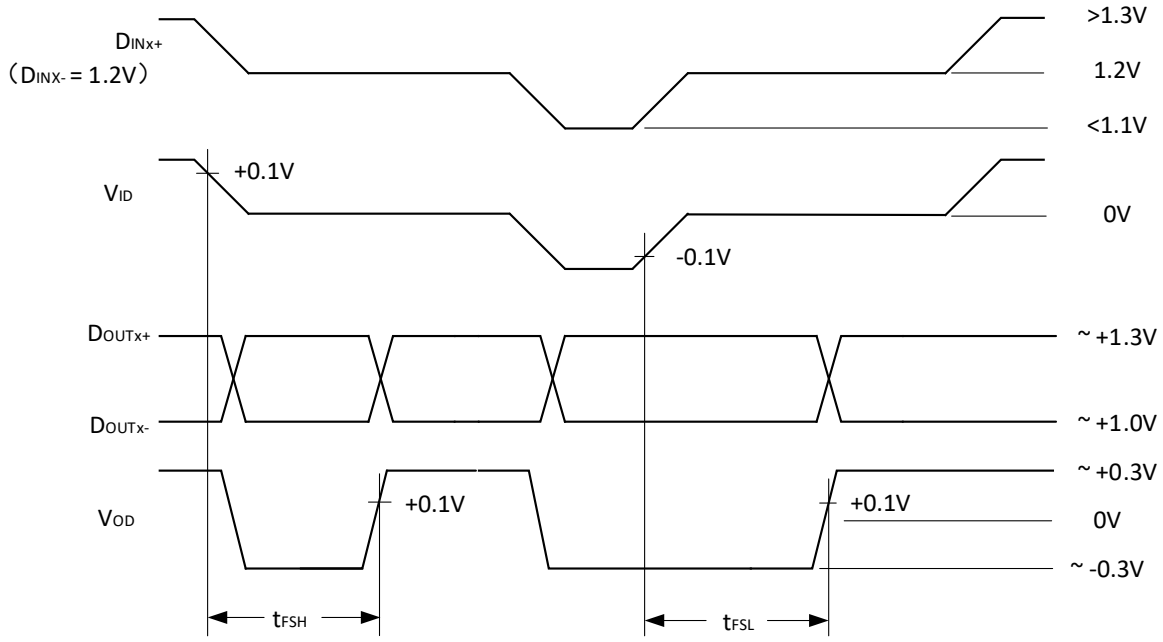


Figure 7-5 Fail-Safe Timing Diagram

8 Detailed Description

8.1 Overview

The CA-IS303x devices are dual-channel, 1.1-Gbps isolated LVDS buffer in 16-pin/20-pin wide-body SOIC packages. These devices are compliant with TIA/EIA-644-A LVDS standard, ideal for high-speed data interconnection applications. The CA-IS303x receivers detect differential signals as low as 100mV and transfer the digital signals across isolation barrier. The isolated driver outputs use a current-steering configuration to generate a ±2.5mA to ±4.5mA (typical 3.3mA) output current. This current-source output requires a resistive load to terminate the signal and complete the transmission loop. The output voltage swing is determined by the value of the termination resistor multiplied by the driver output current. With a typical 100Ω termination resistor (R_T), the isolated driver produces ±250mV to ±450mV output voltage across the R_T. The received voltage is centered around 1.2V.

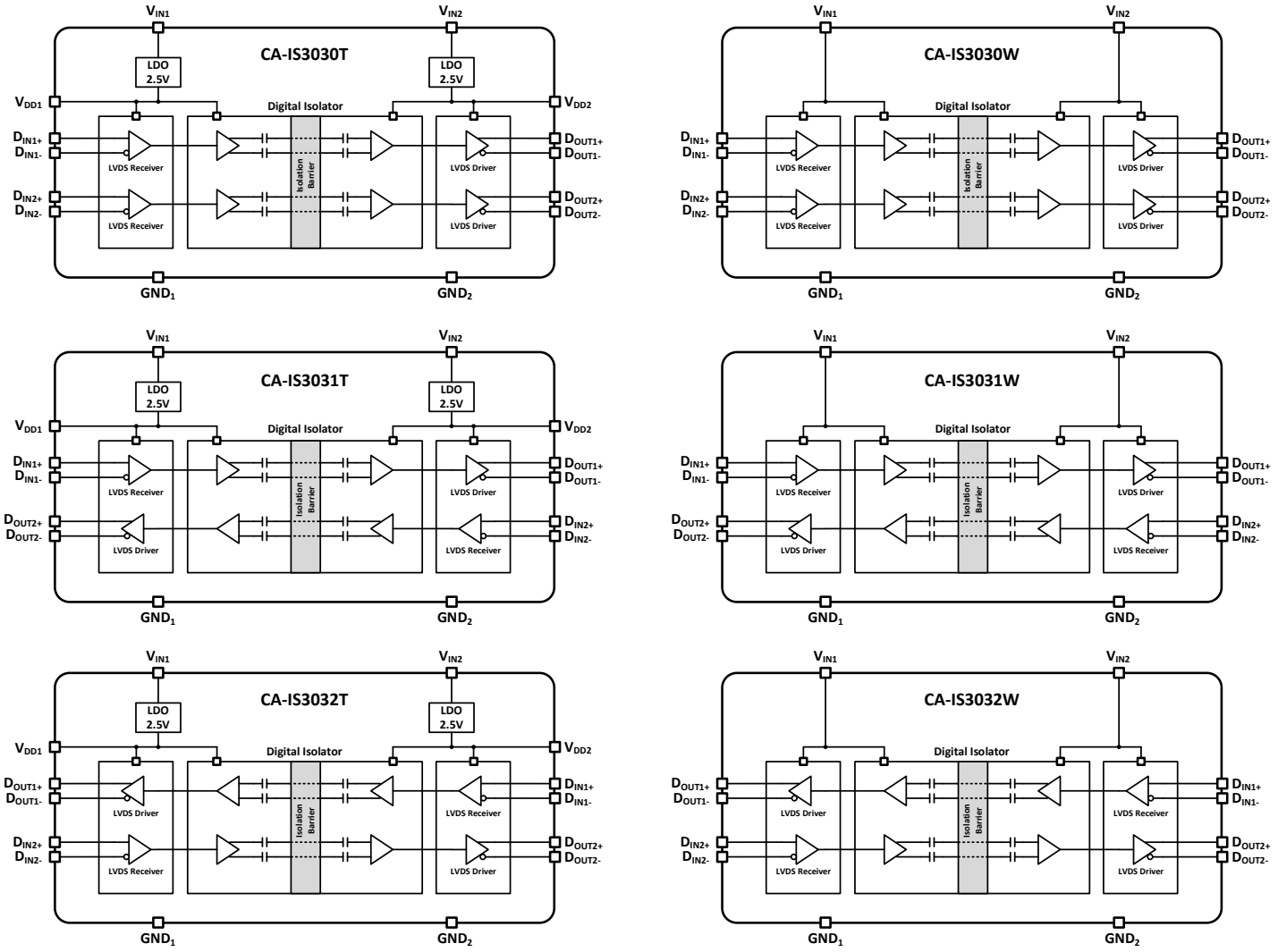


Figure 8-1 Functional Block Diagram of CA-IS303x

The CA-IS303xT devices feature internal LDO. When operating from 3.3V power supply, the integrated LDO generates 2.5V regulated voltage from 3.3V input for LVDS and isolator circuits. The CA-IS303xT LVDS isolator accepts both 2.5V and 3.3V supplies. When operating from 2.5V power supply, connect V_{DDx} to V_{INx} to bypass internal LDO. The CA-IS303xW devices do not have V_{DDx} pins which are powered directly from V_{INx} pins. The CA-IS3031T/CA-IS3032T feature a fail-safe mechanism to ensure a Logic 1 on the corresponding LVDS driver output when the inputs are floating, shorted, or terminated, but not driven. The functional block diagram of CA-IS303x is shown Figure 8-1.

8.2 Device Function Mode

The LVDS standard, TIA/EIA-644-A, defines normal receiver operation under two conditions: an input differential voltage of ≥ +100mV corresponding to logic high, and a voltage of ≤ −100mV for the logic low. With a positive differential voltage of ≥ +100mV across any $D_{INx±}$ pin, the corresponding D_{OUTx+} pin sources current. This current flows across the connected transmission line and termination at the receiver at the far end of the bus, while D_{OUTx-} sinks the return current. With a negative differential voltage of ≤ −100mV across any $D_{INx±}$ pin, the corresponding D_{OUTx+} pin sinks current, with D_{OUTx-} sourcing the current. Table 8-1 and Table 8-2 show the truth table of CA-IS303x.

Table 8-1 Truth Table of CA-IS3030T and CA-IS303xW[1]

Differential Input ($D_{INx±}$)			Differential Output ($D_{OUTx±}$)		
Powered On	V_{ID} (mV)	Logic	Powered On	V_{OD} (mV)	Logic
Yes	≥ 100	H	Yes	≥ 250	H
Yes	≤ –100	L	Yes	≤ –250	L
Yes	–100 < V_{ID} < +100	Indeterminate	Yes	Indeterminate	Indeterminate
No	X	X	Yes	≥ 250	H

NOTE:
1. H = high level, L = low level, X = irrelevant.

Table 8-2 Truth Table of CA-IS3031T/CA-IS3032T[1]

Differential Input ($D_{INx±}$)			Differential Output ($D_{OUTx±}$)		
Powered On	V_{ID} (mV)	Logic	Powered On	V_{OD} (mV)	Logic
Yes	≥ 100	H	Yes	≥ 250	H
Yes	≤ –100	L	Yes	≤ –250	L
Yes	–100 < V_{ID} < +100	Indeterminate	Yes	≥ 250	H
No	X	X	Yes	≥ 250	H

NOTE:
1. H = high level, L = low level, X = irrelevant.

8.3 Fail-Safe Receiver

The CA-IS3031T and CA-IS3032T devices feature a fail-safe mechanism to keep the LVDS output in a known state (logic high) when the receiver inputs are open, shorted or idle (−100mV < V_{ID} < +100 mV). These devices have about 1-µs delay from the fail-safe function active to LVDS buffer output high (V_{OD} ≥ 250mV). During this time, the LVDS buffer output may stay at low (V_{OD} ≤ −250mV).

The fail-safe circuit triggers as soon as the input differential voltage remains between +100 mV and −100 mV for some nanoseconds. This means that very slow rise and fall times on the input signal can potentially trigger the fail-safe circuit on a high to low crossover. So that when the devices operate at very low-speed data rate, we recommend to connect larger termination resistors across D_{INx+} and D_{INx-} to reduce indeterminate time for LVDS input.

9 Application and Implementation

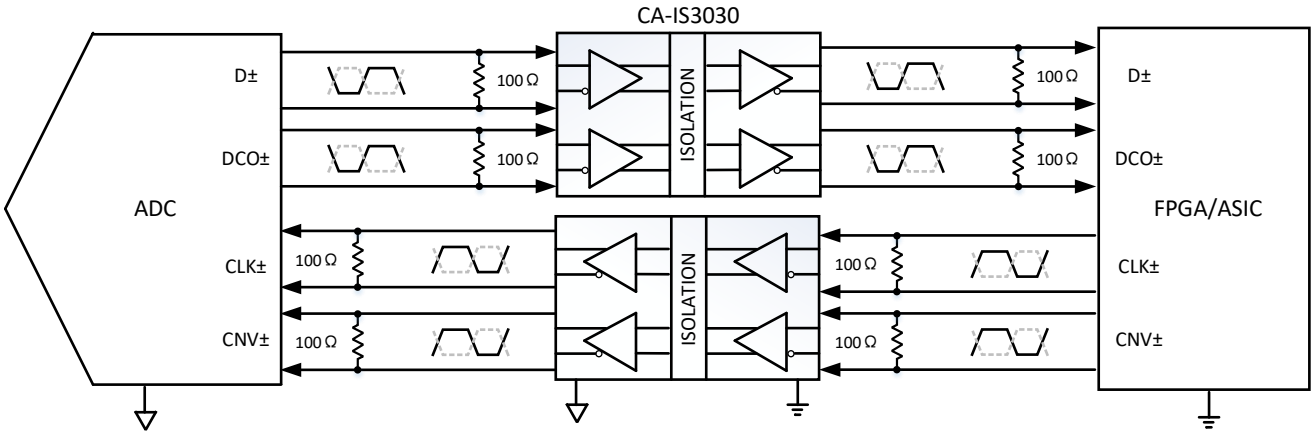


Figure 9-1 Typical Application Circuit for Isolated Analog Front-End Implementation Using CA-IS3030

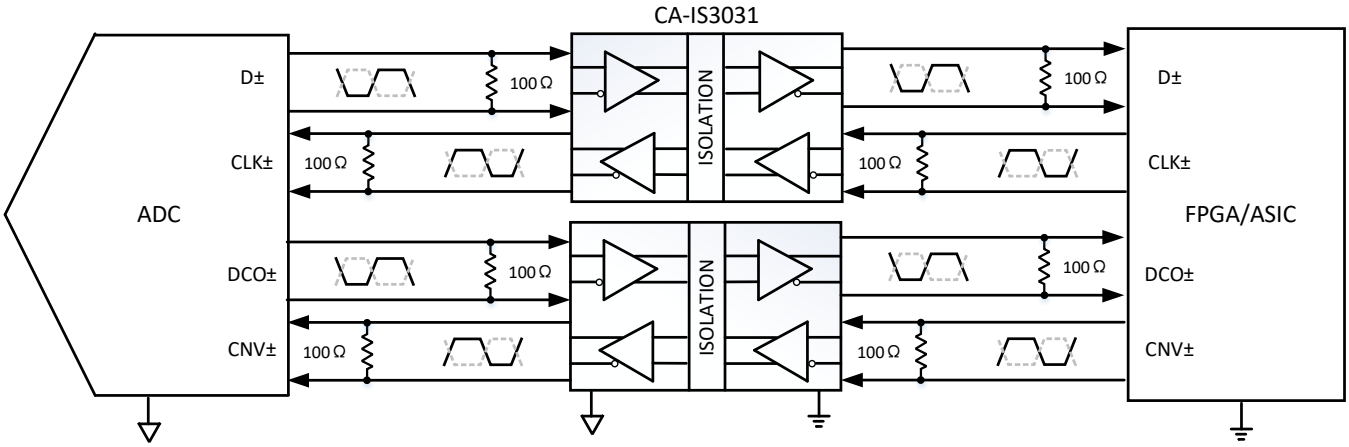


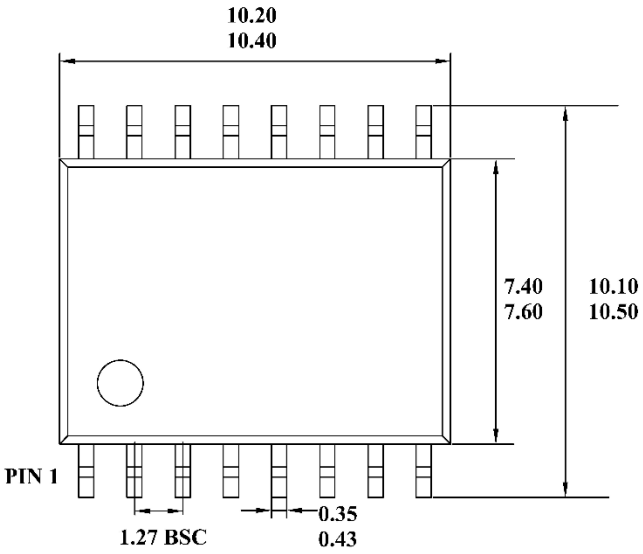
Figure 9-2 Typical Application Circuit for Isolated Analog Front-End Implementation Using CA-IS3031

The typical application circuits of CA-IS303x are shown in Figure 9-1 and Figure 9-2. The CA-IS303x isolated LVDS buffers support up to 1.1-Gbps data rate. For high-speed signal circuit boards, we recommend to use a four-layer PCB that provides separate power, ground, input and output signals to achieve a low EMI PCB design. Use controlled-impedance traces and connectors with matched characteristic impedance, also ensure that noise couples as common mode. Keep the area underneath the LVDS isolator free from ground and signal planes. Place 100-Ω termination resistors as close as possible to the receivers across the D_{INx+} pins and D_{INx-} pins. Bypass 3.3V power supply input V_{INx} to GNDx with 0.1µF and 1µF capacitors in parallel as close to the device as possible, with the smaller value capacitor closest to the device. For the CA-IS303xT, when operating from 2.5-V power supply, connect V_{DDx} to V_{INx} to bypass the internal LDO, and bypass V_{DDx} to GNDx with high-frequency surface mount ceramic 0.1-µF capacitor as close to the device as possible; when operating from 3.3V single power supply input, bypass V_{DDx} to GNDx with 1µF capacitor.

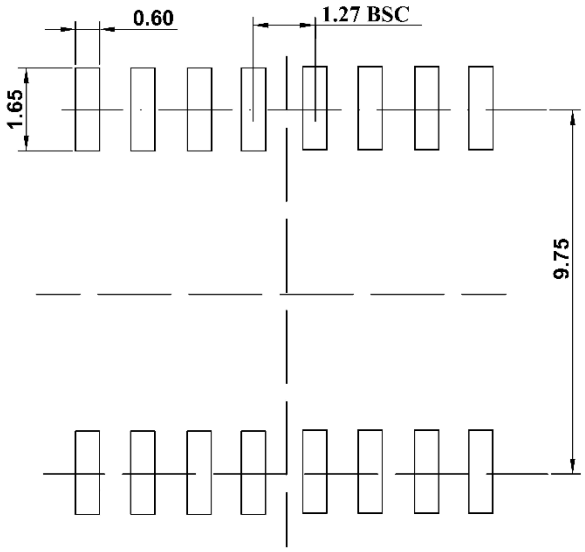
10 Package Information

10.1 SOIC16-WB Package

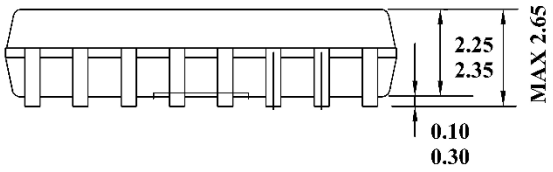
The values for the dimensions are shown in millimeters.



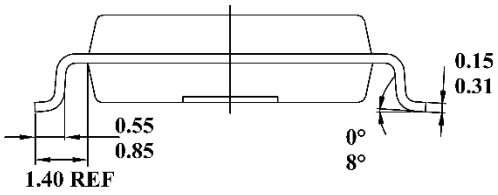
TOP VIEW



RECOMMENDED LAND PATTERN



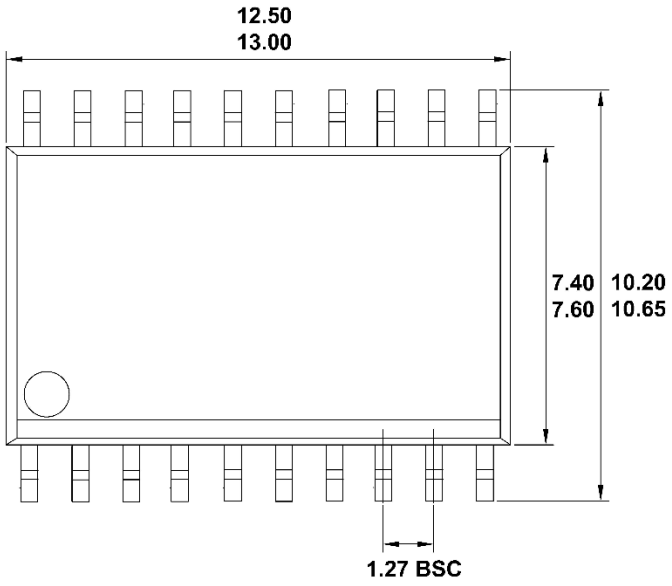
FRONT VIEW



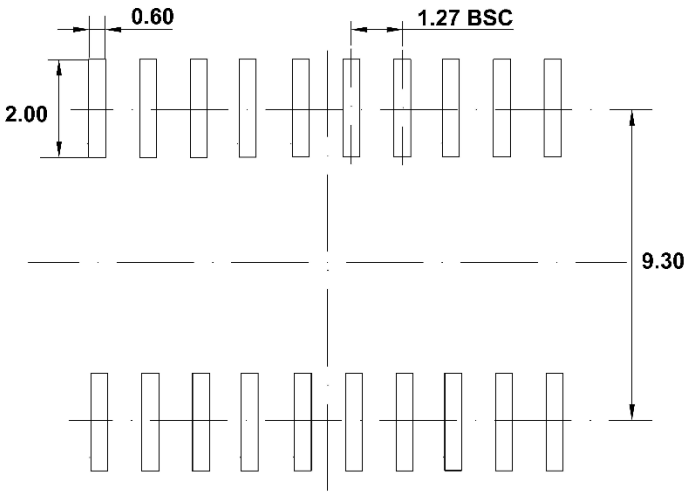
LEFT SIDE VIEW

10.2 SOIC20-WB Package

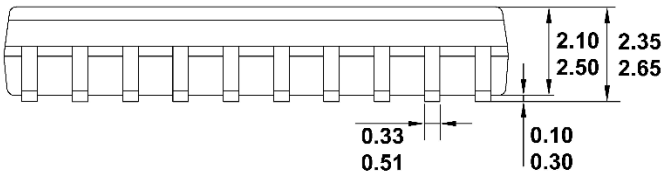
The values for the dimensions are shown in millimeters.



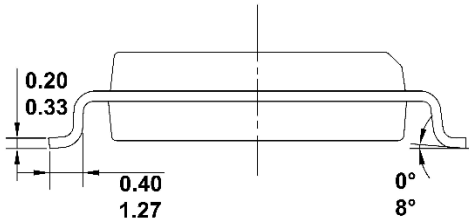
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LFET SIDE VIEW

11 Soldering Information

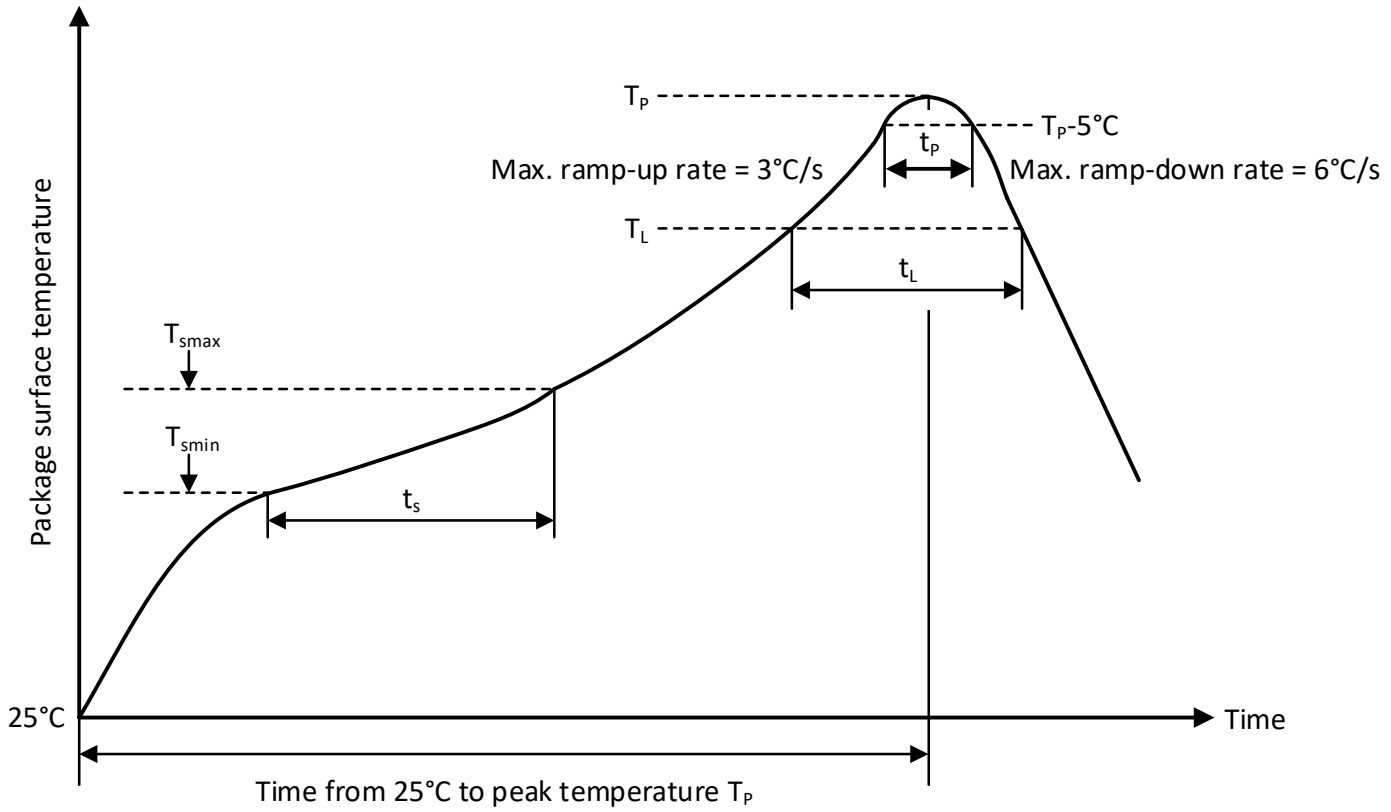


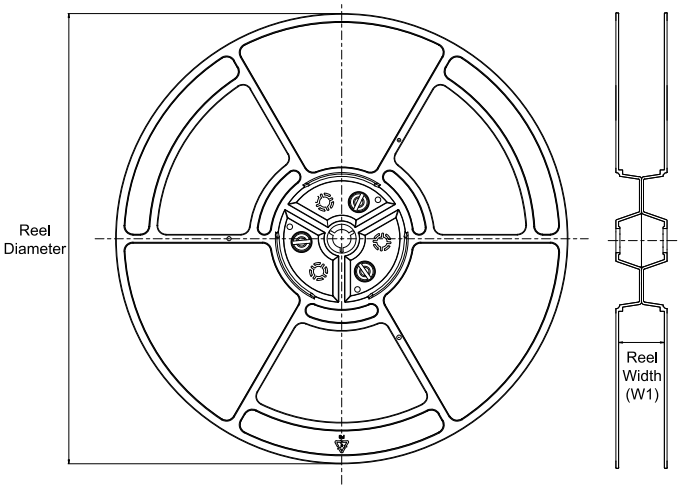
Figure 11-1 Soldering Temperature Curve

Table 11-1 Soldering Temperature Parameters

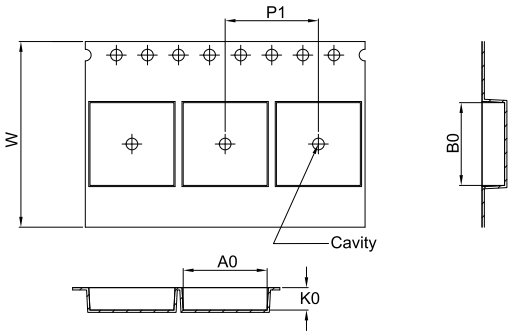
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

12 Tape and Reel Information

REEL DIMENSIONS

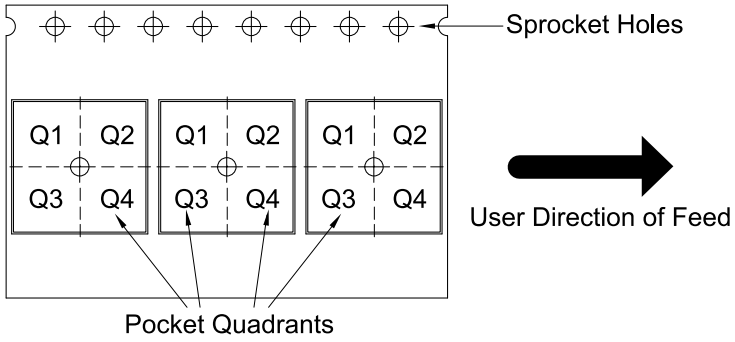


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3030W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3031W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3032W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3030T	SOIC	T	20	1000	330	24.4	10.8	13.3	3.2	16.0	24.0	Q1
CA-IS3031T	SOIC	T	20	1000	330	24.4	10.8	13.3	3.2	16.0	24.0	Q1
CA-IS3032T	SOIC	T	20	1000	330	24.4	10.8	13.3	3.2	16.0	24.0	Q1

13 Revision History

Revision	Description	Date	Page
Version 1.00	NA	2024.12.01	NA
Version 1.01	Added Safety Limiting Values.	2025.02.25	8
Version 1.02	Update ESD rating of HBM: from ±3kV to ±4kV Update ESD rating of contact discharge: from ±7kV to ±6kV	2026.03.30	6 1, 6

14 Important Notice

The above information is for reference only and is used to assist Chipanalog customers in design and development. Chipanalog reserves the right to change the above information due to technological innovation without prior notice.

Chipanalog products are all factory tested. The customers shall be responsible for self-assessment and determine whether it is applicable for their specific application. Chipanalog's authorization to use the resources is limited to the development of related applications that the Chipanalog products involved in. In addition, the resources shall not be copied or displayed. And Chipanalog shall not be liable for any claim, cost, and loss arising from the use of the resources.

Trademark Information

Chipanalog Inc. ®, Chipanalog® are trademarks or registered trademarks of Chipanalog.

http://www.chipanalog.com