CA-IS3212 High CMTI, Single-Channel Isolated Gate Driver for IGBT/SiC/GaN

1. Key Features

- Drive SiC MOSFET and IGBT up to 2121V_{PK}
- 4A Peak Source Current and 5A Peak Sink Current
- CMOS Inputs or TTL Inputs (CA-IS3212TSCG)
- Wide Supply Range:
    - 3.0V to 5.5V Input-Side Supply Voltage (VCC)
    - Up to 33V Output-Drive Supply Voltage (VDD – VEE) With Different UVLO Options:
        - Y Version: 4V
        - A Version: 6V
        - B Version: 8V
        - C Version: 12V
- 40-ns (Typical) Input Glitch Filter
- Matching Propagation Delay
    - 85-ns Propagation Delay (Typical)
    - 15-ns Pulse Width Distortion (Maximum)
    - 15-ns Part to Part Propagation Delay Matching (Maximum)
- Package options
    - 8-Pin Wide-Body SOIC Package With Creepage and Clearance > 8mm and 5.7-kV_{RMS} Isolation Rating
    - 8-Pin Narrow-Body SOIC Package With Creepage and Clearance > 4mm and 3.75-kV_{RMS} Isolation Rating
- High CMTI: > ±150kV/µs
- Isolation Barrier Lifetime: >40 years
- –40°C to 150°C Operating Junction Temperature (T_J) Range
- Safety-Related Certifications (Pending):
    - DIN EN IEC 60747- 17 (VDE 0884-17):2021-10
    - UL Certification According to UL 1577
    - CQC Certification According to GB4943.1-2022
    - TUV Certification According to EN 62368-1 and EN 61010-1

2. Applications

- Motor Inverters
- HEV/EV Battery Charger
- Solar Inverters
- Power Conversion System
- Charging Pile Power Modules
- Servo Drivers
- Frequency Converter
- Uninterruptible Power Supply (UPS)

3. Description

The CA-IS3212 devices are a family of single-channel isolated gate drivers capable of sinking 5A and sourcing 4A peak currents. Excellent dynamic performance and high-reliability make these devices ideal for Si MOSFET, IGBT, GaN and SiC MOSFET driving applications in the inverter, motor control or isolated power supply etc. systems.

All devices have integrated digital galvanic isolation between control-side and driver-side using Chipanalog’s proprietary SiO_2 capacitive isolation technology which features up to 5.7-kV_{RMS} isolation rating for the wide-body package devices and minimum common-mode transient immunity (CMTI) of 150kV/µs, supporting up to 1.5-kV_{RMS} isolation working voltage and 12.8-kV_{PK} surge rating.

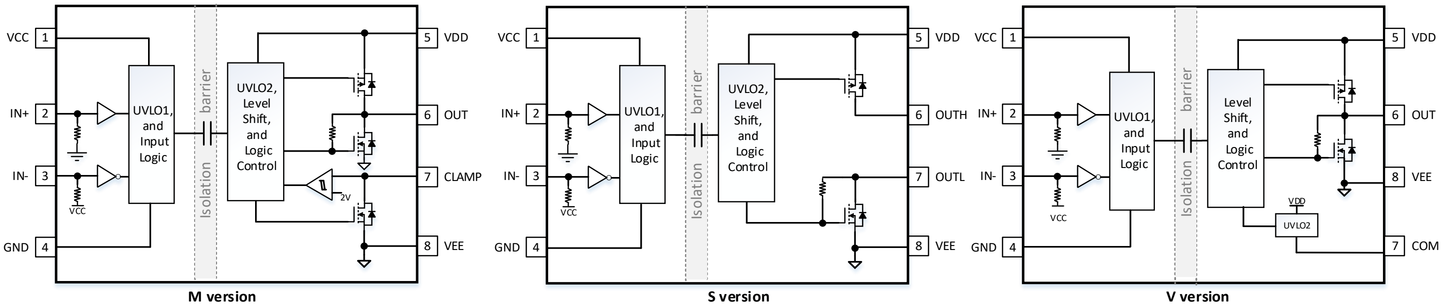
The CA-IS3212 devices are optimized for SiC, GaN and IGBT switching operation to improve system reliability. The CA-IS3212Mxx features 5A internal active miller clamp; The CA-IS3212Vxx offers COM pin to support dual supplies at driver side; The CA-IS3212Sxx provides OUTH and OUTL split outputs. Both control-side supply (VCC) and driver-side supply (VDD – VEE) are internally monitored for undervoltage conditions with different UVLO detection threshold options.

The CA-IS3212 devices are available either in an 8-pin narrow-body SOIC package, or in an 8-pin wide-body SOIC package. All devices are rated for operation at junction temperature range of –40°C to +150°C.

Table 3-1 Device Information

Part Number	Package	Package Size (NOM)
CA-IS3212xxS	SOIC8 (S)	4.90mm x 3.90mm
CA-IS3212xxG	SOIC8-WB (G)	5.85mm x 7.50mm

Figure 3-1 Simplified Schematic



M version S version V version

4. Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Input Logic	Driver-Side UVLO	Output type	Miller Clamp	External COM	Package
CA-IS3212MYS	CMOS	4V	Single	5A	No	SOIC8 (S)
CA-IS3212MBS	CMOS	8V	Single	5A	No	SOIC8 (S)
CA-IS3212MCS	CMOS	12V	Single	5A	No	SOIC8 (S)
CA-IS3212SBS	CMOS	8V	Split	–	No	SOIC8 (S)
CA-IS3212SCS	CMOS	12V	Split	–	No	SOIC8 (S)
CA-IS3212VCS	CMOS	12V	Single	–	Yes	SOIC8 (S)
CA-IS3212MBG	CMOS	8V	Single	5A	No	SOIC8-WB (G)
CA-IS3212MCG	CMOS	12V	Single	5A	No	SOIC8-WB (G)
CA-IS3212SBG	CMOS	8V	Split	–	No	SOIC8-WB (G)
CA-IS3212SCG	CMOS	12V	Split	–	No	SOIC8-WB (G)
CA-IS3212VCG	CMOS	12V	Single	–	Yes	SOIC8-WB (G)
CA-IS3212TSCG	TTL	12V	Split	–	No	SOIC8-WB (G)

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5. Pin Configuration and Description

5.1. CA-IS3212Mxx

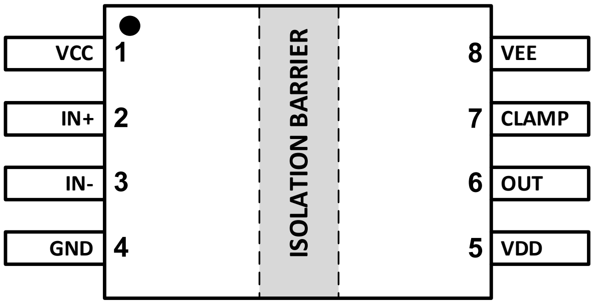


Figure 5-1 CA-IS3212Mxx Pin Configuration

Table 5-1 CA-IS3212Mxx Pin Description

Pin Name	Pin Number	Type[1]	Description
VCC	1	P	3V to 5.5V power supply for control-side. Bypass VCC to GND with an at least 1µF capacitor as close to the device as possible.
IN+	2	I	Non-inverting gate-driver control input with internal pull-down.
IN–	3	I	Inverting gate-driver control input with internal pull-up.
GND	4	G	Ground reference for control-side supply and logic input.
VDD	5	P	Positive power supply input for driver-side. Bypass VDD to VEE with 0.1µF||10µF capacitors as close as possible to the pin VDD.
OUT	6	O	Gate-driver output.
CLAMP	7	I	Internal active Miller clamp input. Connect CLAMP to the gate of external power transistor.
VEE	8	G	Ground reference for driver-side. Connect VEE to driver-side ground in single power supply configuration. Connect VEE to driver-side negative power supply in dual power supplies configuration.

Note:

1. P = power supply; G = ground; I = input; O = output.

5.2. CA-IS3212(T)Sxx

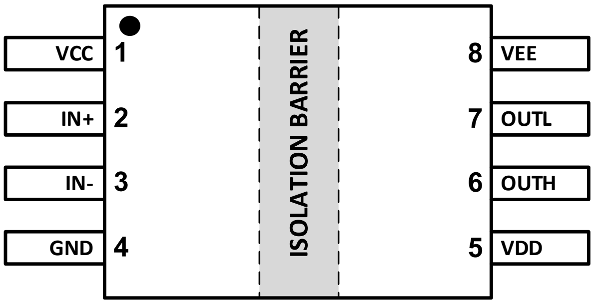


Figure 5-2 CA-IS3212(T)Sxx Pin Configuration

Table 5-2 CA-IS3212(T)Sxx Pin Description

Pin Name	Pin Number	Type[1]	Description
VCC	1	P	3V to 5.5V power supply for control-side. Bypass VCC to GND with an at least 1µF capacitor as close to the device as possible.
IN+	2	I	Non-inverting gate-driver control input with internal pull-down.
IN–	3	I	Inverting gate-driver control input with internal pull-up.
GND	4	G	Ground reference for control-side supply and logic input.
VDD	5	P	Positive power supply input for driver-side. Bypass VDD to VEE with 0.1µF||10µF capacitors as close as possible to the pin VDD.
OUTH	6	O	Positive gate drive output, source current.
OUTL	7	O	Negative gate drive output, sink current.
VEE	8	G	Ground reference for driver-side. Connect VEE to driver-side ground in single power supply configuration. Connect VEE to driver-side negative power supply in dual power supplies configuration.

Note:

1. P = power supply; G = ground; I = input; O = output.

5.3. CA-IS3212Vxx

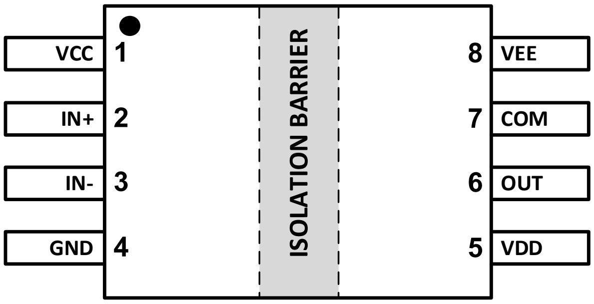


Figure 5-3 CA-IS3212Vxx Pin Configuration

Table 5-3 CA-IS3212Vxx Pin Description

Pin Name	Pin Number	Type[1]	Description
VCC	1	P	3V to 5.5V power supply for control-side. Bypass VCC to GND with an at least 1μF capacitor as close to the device as possible.
IN+	2	I	Non-inverting gate-driver control input with internal pull-down.
IN–	3	I	Inverting gate-driver control input with internal pull-up.
GND	4	G	Ground reference for control-side supply and logic input.
VDD	5	P	Positive power supply input for driver-side. Bypass VDD to COM with 0.1μF||10μF capacitors as close as possible to the pin VDD.
OUT	6	O	Gate-driver output.
COM	7	G	Ground reference for driver-side. Connect COM to external IGBT’s emitter or SiC MOSFET’s source.
VEE	8	P	Negative power supply input for gate driver. Bypass VEE to COM with at least 10μF capacitor as close as possible to the pin VEE.

Note:

1. P = power supply; G = ground; I = input; O = output.

6. Specifications

6.1. Absolute Maximum Ratings[1]

Over operating free-air temperature range unless otherwise specified.

Symbol	Parameters	Minimum	Maximum	Unit
VCC	VCC – GND	–0.3	6	V
VDD	VDD – COM	–0.3	36	V
VEE	VEE – COM	–17.5	0.3	V
V_{MAX}	VDD – VEE	–0.3	36	V
IN+, IN–	DC	GND – 0.3	VCC + 0.3	V
OUTH, OUTL, CLAMP	DC	VEE – 0.3	VDD + 0.3	V
T_J[2]	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

Notes:

1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. To maintain the recommended operating junction temperature conditions, see Thermal Information.

6.2. ESD Ratings

Symbol	Parameters	Value	Unit
V_{ESD} Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins, only for CA-IS3212TSCG	±3000	V
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins, other devices	±4000	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±2000	

6.3. Recommended Operating Conditions

Over operating free-air temperature range unless otherwise specified.

Symbol	Parameters		Minimum	Maximum	Unit
VCC	VCC – GND		3.0	5.5	V
T_A	Ambient temperature		–40	125	°C
T_J	Junction temperature		–40	150	°C
Devices Except for CA-IS3212Vxx					
VDD	VDD – VEE	CA-IS3212xYx	5	33	V
		CA-IS3212xAx	7	33	
		CA-IS3212xBx	9	33	
		CA-IS3212xCx	13.2	33	
CA-IS3212Vxx					
VDD	VDD – VEE	CA-IS3212Vxx	--	33	V
	VDD – COM	CA-IS3212VAx	7	33	
		CA-IS3212VBx	9	33	
		CA-IS3212VCx	13.2	33	
VEE	VEE – COM	CA-IS3212Vxx	–16	0	
Input Logic for Devices Except for CA-IS3212TSCG (CMOS)					
IN+, IN–	Referenced to GND	Logic high-level input voltage	0.7 × VCC	VCC	V
		Logic low-level input voltage	0	0.3 × VCC	
Input Logic for CA-IS3212TSCG (TTL)					
IN+, IN–	Referenced to GND	Logic high-level input voltage	2.0	VCC	V
		Logic low-level input voltage	0	0.8	

6.4. Thermal Information

Symbol	Thermal Metric	Package		Unit
		SOIC8 (S)	SOIC8-WB (G)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.5	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.2	51.7	°C/W

6.5. Power Ratings

Symbol	Parameters	Test Conditions	Minimum	Typical	Maximum	Unit
P_D	Maximum input and output power dissipation	VCC = 5V, VDD – COM = 20V, COM – VEE = 5V, IN+/– = 5V, 150kHz, 50% duty cycle square wave, C_L = 2.2nF, T_A = 25°C			1.05	W
P_{D1}	Maximum input power dissipation				0.05	W
P_{D2}	Maximum output power dissipation				1	W

6.6. Insulation Specifications

Parameters		Test Conditions	Value (S)	Value (G)	Unit
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	> 4	> 8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	> 4	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 24	> 24	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	> 600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ $150V_{RMS}$	I-IV	I-IV	
		Rated mains voltage ≤ $300V_{RMS}$	I-IV	I-IV	
		Rated mains voltage ≤ $600V_{RMS}$	I-III	I-IV	
		Rated mains voltage ≤ $1000V_{RMS}$	NA	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	990	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	700	1500	V_{RMS}
		DC voltage	990	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	5300	8000	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	5000	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	6500	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s (S) $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s (G)	≤ 5	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.5 \times V_{IORM}$， t_m = 1s (S) $V_{pd(m)} = 1.875 \times V_{IORM}$， t_m = 1s (G)	≤ 5	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1MHz	~ 1.2	~ 1.2	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500V, T_A = 25°C	$> 10^{12}$	$> 10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	$> 10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$> 10^{9}$	$> 10^{9}$	
	Pollution degree		2	2	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	3750	5700	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

6.7. Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Recognized under UL 1577 Component Recognition Program and CSA Component Acceptance Service Notice No. 5A	Certified according to GB4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
Basic Insulation (SOIC8): V_{IORM}: 990V_{PK} V_{IOTM}: 5300V_{PK} V_{IOSM}: 6500V_{PK} Reinforced Insulation (SOIC8-WB): V_{IORM}: 2121V_{PK} V_{IOTM}: 8000V_{PK} V_{IOSM}: 12800V_{PK}	Single protection SOIC8: 3750V_{RMS} SOIC8-WB: 5700V_{RMS}	SOIC8: Basic insulation SOIC8-WB: Reinforced insulation (Altitude ≤ 5000m)	EN 61010-1 SOIC8: 3750V_{RMS} SOIC8-WB: 5700V_{RMS} EN 62368-1 SOIC8: 3750V_{RMS} SOIC8-WB: 5700V_{RMS}
Certification Number: Pending	Certification Number: E511334	Certificate number: SOIC8: CQC24001452685 SOIC8-WB: CQC24001434134	Client reference number: 2253313

6.8. Safety Limits

Symbol	Parameters	Test Conditions		Minimum	Typical	Maximum	Unit
SOIC8 (S)							
I_S	Safety output supply current	$R_{\theta JA}$ = 104.5°C/W, VDD – VEE = 15V, T_J = 150°C, T_A = 25°C	Output side			76	mA
		$R_{\theta JA}$ = 104.5°C/W, VDD – VEE = 15V, T_J = 150°C, T_A = 25°C	Output side			38	
P_S	Safety input, output or total power	$R_{\theta JA}$ = 104.5°C/W, T_J = 150°C, T_A = 25°C	Input side			50	mW
			Output side			1146	
			Total			1196	
T_S	Maximum safety temperature					150	°C
SOIC8-WB (G)							
I_S	Safety output supply current	$R_{\theta JA}$ = 110°C/W, VDD – VEE = 15V, T_J = 150°C, T_A = 25°C	Output side			72	mA
		$R_{\theta JA}$ = 110°C/W, VDD – VEE = 15V, T_J = 150°C, T_A = 25°C	Output side			36	
P_S	Safety input, output or total power	$R_{\theta JA}$ = 110°C/W, T_J = 150°C, T_A = 25°C	Input side			50	mW
			Output side			1086	
			Total			1136	
T_S	Maximum safety temperature					150	°C

6.9. Electrical Characteristics

All typical specifications are at VCC = 3.3V, T_A = 25°C, VDD – COM = 15V, COM – VEE = 5V (unless otherwise noted). All minimum and maximum specifications apply from VCC = 3.3V or 5V, VDD – COM = 15V~30V, COM – VEE = 5V~15V, –40°C < T_J <150°C.[1, 2]

Symbol	Parameters	Test Conditions	Minimum	Typical	Maximum	Unit
VCC UVLO and Delay Time						
V_{VCC_ON}	VCC UVLO		2.55	2.7	2.85	V
V_{VCC_OFF}			2.35	2.5	2.65	
V_{VCC_HYS}				0.2		
t_{VCCFIL}	VCC UVLO deglitch time			5		µs
$t_{VCC+\text{ to OUT}}$	VCC power up delay to output high	IN+ = VCC, IN– = GND		22	60	
$t_{VCC-\text{ to OUT}}$	VCC power down delay to output low, VCC falls from 3.3V to 2.2V			7	15	
VDD UVLO						
V_{VDD_ON}	VDD UVLO (Y Version)		4	4.4	4.8	V
V_{VDD_OFF}			3.8	4.1	4.5	
V_{VDD_HYS}			0.2	0.3	0.5	
VDD UVLO						
V_{VDD_ON}	VDD UVLO (A Version)		5.4	6.0	6.6	V
V_{VDD_OFF}			4.9	5.5	6.1	
V_{VDD_HYS}				0.5		
VDD UVLO						
V_{VDD_ON}	VDD UVLO (B Version)		7.3	8.1	8.9	V
V_{VDD_OFF}			6.7	7.4	8.2	
V_{VDD_HYS}				0.7		
VDD UVLO						
V_{VDD_ON}	VDD UVLO (C Version)		11.0	12.0	13.0	V
V_{VDD_OFF}			10.0	11.0	12.0	
V_{VDD_HYS}				1.0		
t_{VDDFIL}	VDD UVLO deglitch time			9		µs
$t_{VDD+\text{ to OUT}}$	VDD power up delay to output high	IN+ = VCC, IN– = GND		8.5	15	
$t_{VDD-\text{ to OUT}}$	VDD power down delay to output low, VDD falls from 15V to (V_{VDD_OFF} – 2V)			8.5	15	
VCC, VDD, VEE Supply Current						
I_{VCCQ}	VCC quiescent current	OUTH = High		1.15	2.0	mA
		OUTL = Low		0.55	1.0	
I_{VDDQ}	VDD quiescent current	OUT = High/Low		1.45	2.5	
I_{VEEQ}	VEE quiescent current	OUT = High/Low, only for CA-IS3212Vxx		1.51	2.5	
Logic Inputs (IN+ and IN–)						
V_{INH}	Logic-high input threshold voltage	VCC = 3.3V, except for CA-IS3212TSCG		1.85	2.31	V
V_{INL}	Logic-low input threshold voltage		0.99	1.52		
V_{INHYS}	Input threshold hysteresis			0.5		
V_{INH}	Logic-high input threshold voltage	only for CA-IS3212TSCG		1.53	2.0	V
V_{INL}	Logic-low input threshold voltage		0.8	1.17		
V_{INHYS}	Input threshold hysteresis			0.36		
R_{IND}	Input pull-down resistance	IN+ = VCC	27	33	39	kΩ
R_{INU}	Input pull-up resistance	IN– = GND	144	180	216	kΩ
t_{INFIL}	Input deglitch filter time (ON and OFF)	f = 50kHz, see Figure 7-3	20	40	60	ns

Electrical Characteristics (continued)

All typical specifications are at VCC = 3.3V, T_A = 25°C, VDD – COM = 15V, COM – VEE = 5V (unless otherwise noted). All minimum and maximum specifications apply from VCC = 3.3V or 5V, VDD – COM = 15V~30V, COM – VEE = 5V~15V, –40°C < T_J <150°C.[1, 2]

Symbol	Parameters	Test Conditions	Minimum	Typical	Maximum	Unit
Gate Driver						
I_{OUTH}	Peak source current	C_{VDD} = 10µF, C_L = 0.18µF, f_S = 1kHz		4		A
I_{OUTL}	Peak sink current	C_{VEE} = 10µF, C_L = 0.18µF, f_S = 1kHz		5		A
R_{OUTH}	Output pull-up resistance	I_{OUT} = –0.2A		1.1		Ω
R_{OUTL}	Output pull-down resistance	I_{OUT} = 0.2A		0.6		Ω
V_{OUTH}	Output high voltage	I_{OUT} = –0.2A, VDD = 18V		17.78		V
V_{OUTL}	Output low voltage	I_{OUT} = 0.2A		120		mV
Active Pull-Down						
V_{OUTPD}	Output Active pull-down voltage on OUTL	I_{OUTL} =0.5A, VDD = OPEN, VEE = COM		2.0		V
Internal Active Miller Clamp (CA-IS3212M)						
$V_{CLAMPTH}$	Miller clamp threshold voltage	Referenced to VEE	1.5	2.0	2.5	V
V_{CLAMP}	Low-level output clamp voltage	I_{CLAMP} = 1A		VEE + 0.6		V
I_{CLAMP}	Low-level output clamp current	V_{CLAMP} = 0V, VEE = –4V		5		A
R_{CLAMP}	Miller clamp pull-down resistance	I_{CLAMP} = 0.2A		0.6		Ω
t_{DCLAMP}	Miller clamp ON delay time[3]	C_L = 1.8nF, see Figure 7-4		20	50	ns
Short Circuit Clamp[3]						
$V_{CLP-OUTH}$	V_{OUTH} – VDD	OUT = Low, $I_{OUT(H)}$ = 500mA, t_{CLP} = 10µs		0.75		V
$V_{CLP-OUTL}$	V_{OUTL} – VDD	OUT = High, $I_{OUT(L)}$ = 500mA, t_{CLP} =10µs		1.2		V
$V_{CLP-CLAMP}$	V_{CLAMP} – VDD	OUT = High, I_{CLAMP} = 500mA, t_{CLP} = 10µs		1.2		V

Notes:

1. Inflow current is positive and outflow current is negative.
2. If there is no COM pin, the driver-side power supply voltage is VDD – VEE.
3. Guaranteed by design and bench.

6.10. Switching Characteristics

All typical specifications are at VCC = 3.3V, T_A = 25°C, VDD – COM = 15V, COM – VEE = 5V (unless otherwise noted). All minimum and maximum specifications apply from VCC = 3.3V or 5V, VDD – COM = 15V~30V, COM – VEE = 5V~15V, –40°C < T_J <150°C.

Symbol	Parameters	Test Conditions	Minimum	Typical	Maximum	Unit
t_{PDHL}	Propagation delay, high to low	C_L = 1nF, see Figure 7-1 and Figure 7-2	60	85	125	ns
t_{PDLH}	Propagation delay, low to high		60	85	125	
t_{PWD}	Pulse width distortion $\lvert t_{PDHL} - t_{PDLH} \rvert$				15	
t_{sk-pp}	Part to part skew	Propagation delay (rising or falling)			15	
t_r	Driver output rise time	C_L = 1nF, see Figure 7-1 and Figure 7-2		10		
t_f	Driver output fall time			10		
f_{MAX}	Maximum switching frequency				1	MHz
t_{DEAD}	Dead time for shoot through protection	Devices except for CA-IS3212MYS		200		ns
		CA-IS3212MYS only for GaN application		80		ns
CMTI	Common mode transient immunity	IN+ = High, IN– = Low, see Figure 7-7 to Figure 7-9	150			kV/µs
		IN+ = Low, IN– = Low, see Figure 7-7 to Figure 7-9	150			kV/µs

6.11. Typical Characteristics

Unless otherwise noted, all typical specifications are at VCC = 3.3V, T_A = 25°C, VDD – COM = 15V, COM – VEE = 5V, if there is no COM pin, then VDD – VEE = 20V.

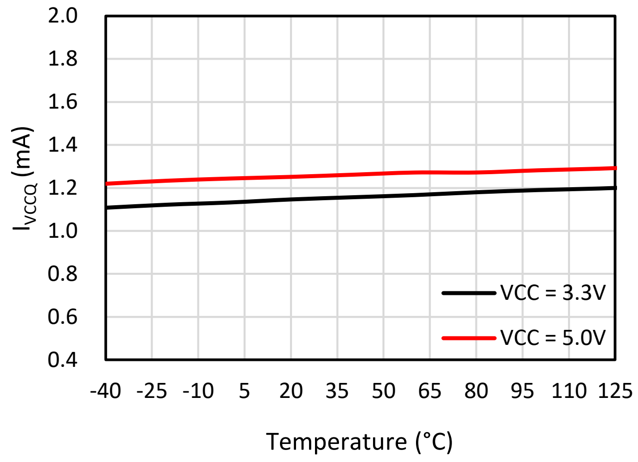


Figure 6-1 VCC Quiescent Current vs. Temperature

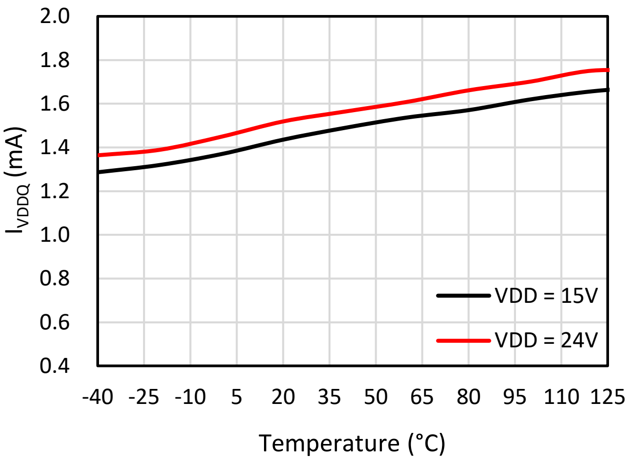


Figure 6-2 VDD Quiescent Current vs. Temperature

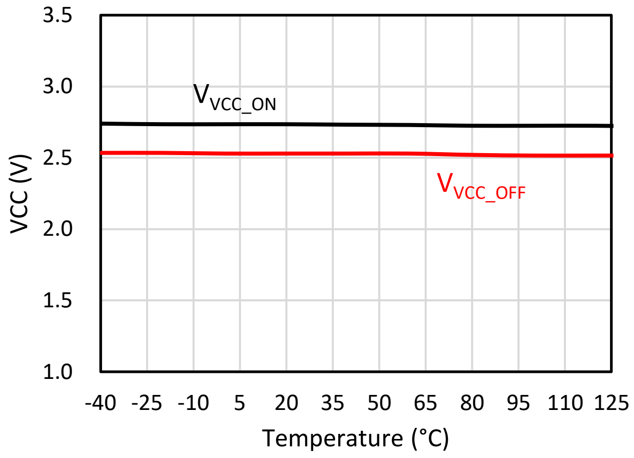


Figure 6-3 VCC UVLO vs. Temperature

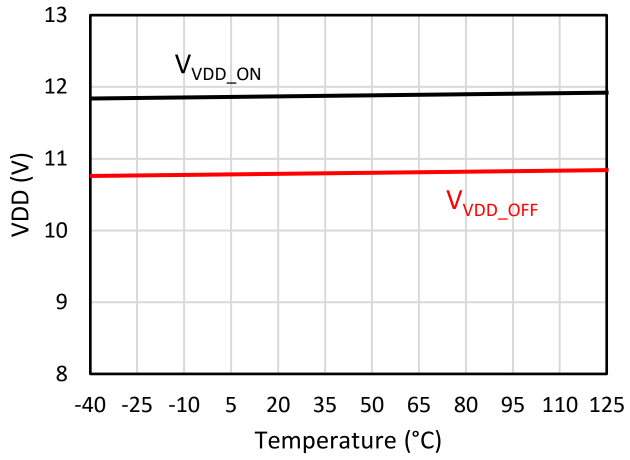


Figure 6-4 VDD UVLO vs. Temperature

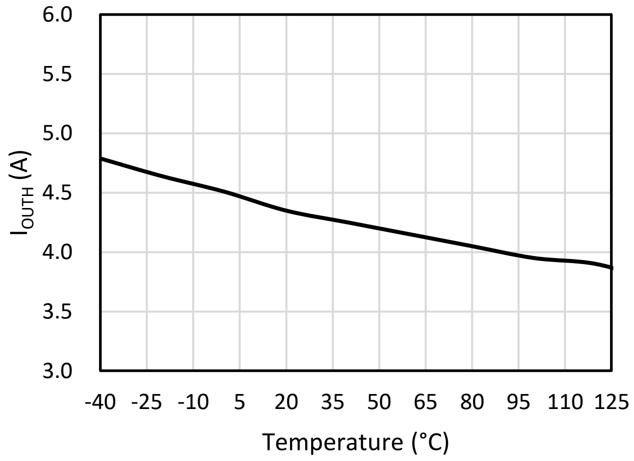


Figure 6-5 Peak Source Current vs. Temperature

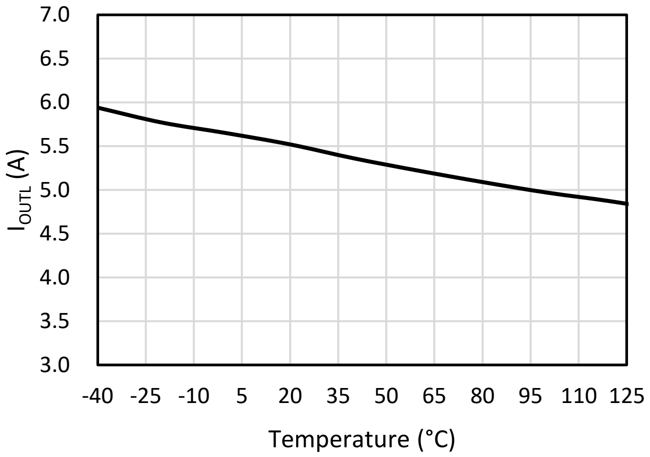


Figure 6-6 Peak Sink Current vs. Temperature

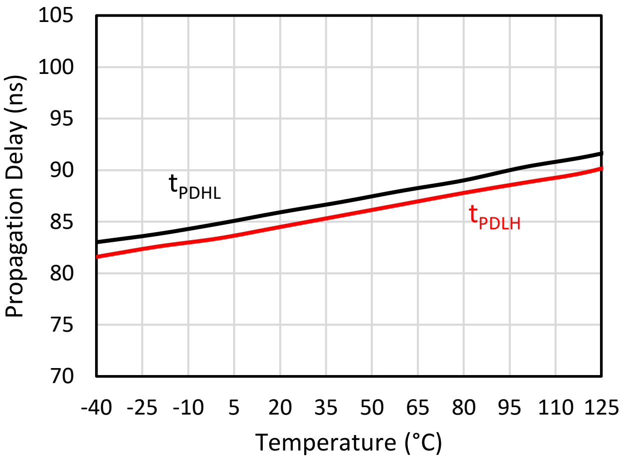


Figure 6-7 Propagation Delay vs. Temperature

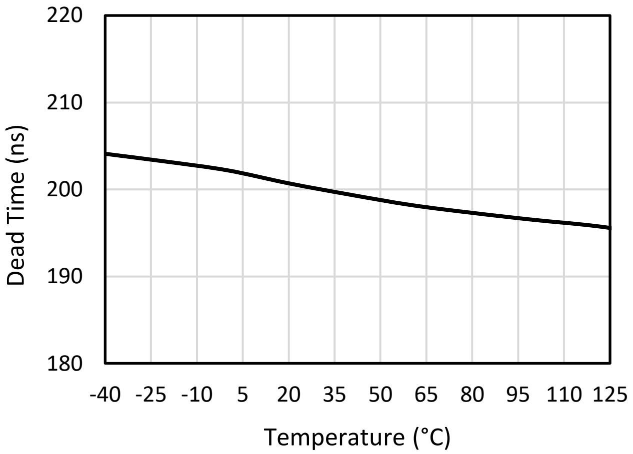


Figure 6-8 Internal Dead Time vs. Temperature

7. Parameter Measurement Information

7.1. Propagation Delay

Figure 7-1 shows the definition and measurement for the non-inverting input propagation delay (t_{PDLH}, t_{PDHL}). Figure 7-2 shows the definition and measurement for the inverting input propagation delay.

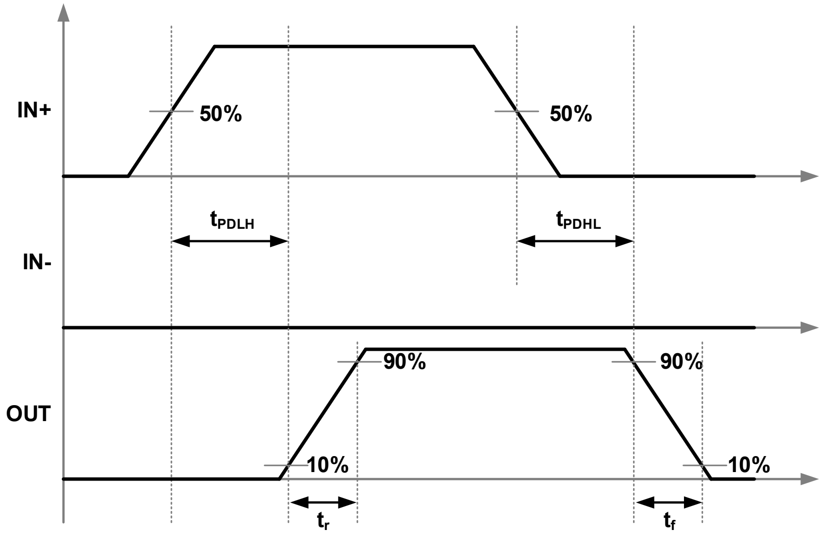


Figure 7-1 Non-inverting Input Propagation Delay Measurement

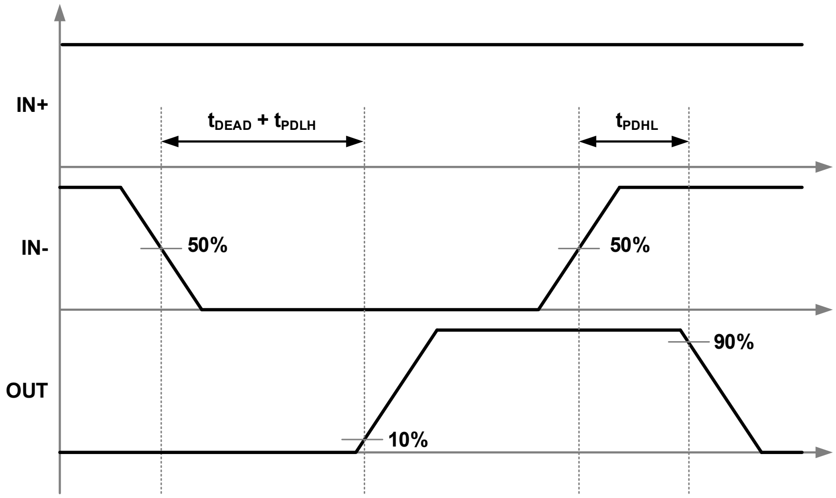


Figure 7-2 Inverting Input Propagation Delay Measurement

7.2. Input Deglitch Filter

Fast common-mode transients and accidental small pulses can inject noise and glitches on the control inputs (IN+ and IN– pins) because of the parasitic coupling. In order to increase the robustness of gate driver, the CA-IS3212 devices feature a 40ns deglitch filter for each control input to reduce glitches and noise at the input, and to avoid wrong output responses or accidental driving operation. For example, if the IN+ PWM pulse width is lease than t_{INFIL}, the input signal will be filtered out and the gate driver output will not respond the input. Figure 7-3 shows the ON/OFF pulse deglitch filter effect on IN+ input;

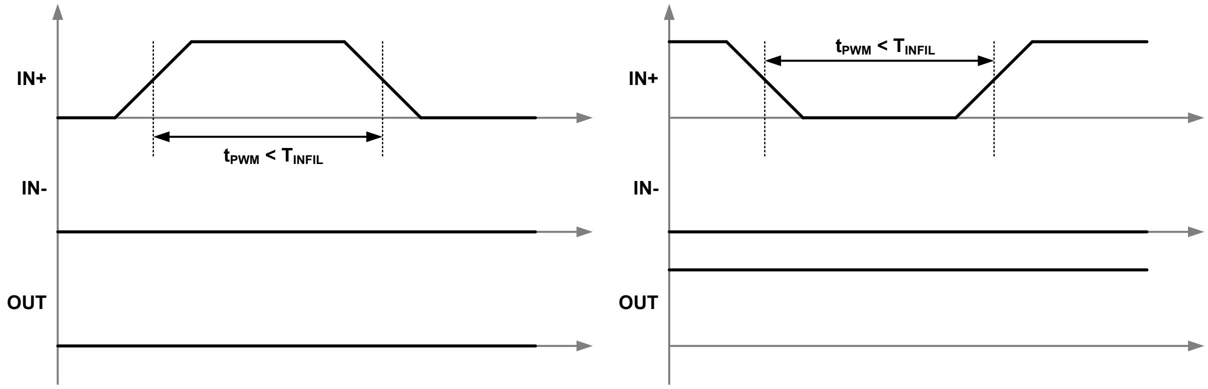


Figure 7-3 IN+ ON/OFF Deglitch Filter

7.3. Active Miller Clamp (CA-IS3212Mxx)

For the gate driver with single supply or dual supplies with small negative turn-off voltage on driver-side, the active Miller clamp circuit provides a very low-impedance path to direct the Miller current. This configuration can prevent the power transistors from unintentionally turning-on because of high dv/dt current induced from the Miller effect, see Figure 7-4 for a Miller clamp timing diagram.

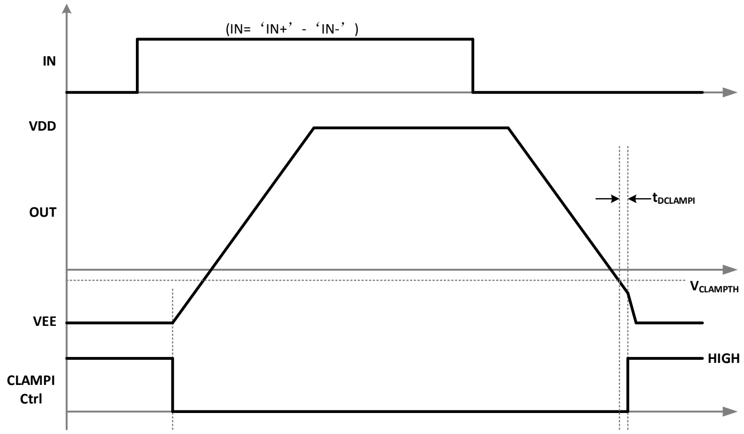


Figure 7-4 Internal Active Miller Clamp Timing Diagram

7.4. Undervoltage Lockout (UVLO)

The VCC and VDD supplies are both internally monitored for undervoltage conditions. UVLO is a key protection function for gate drivers. It can prevent the power transistors from unintentionally turning-on when control-side or driver-side supply is in UVLO condition during power-up, power-down, or during normal operation due to a sagging supply voltage.

7.4.1. VCC UVLO

Figure 7-5 shows the behavior of the driver outputs during VCC power-up and power-down, including UVLO ON/OFF threshold, deglitch filter, response timing diagram.

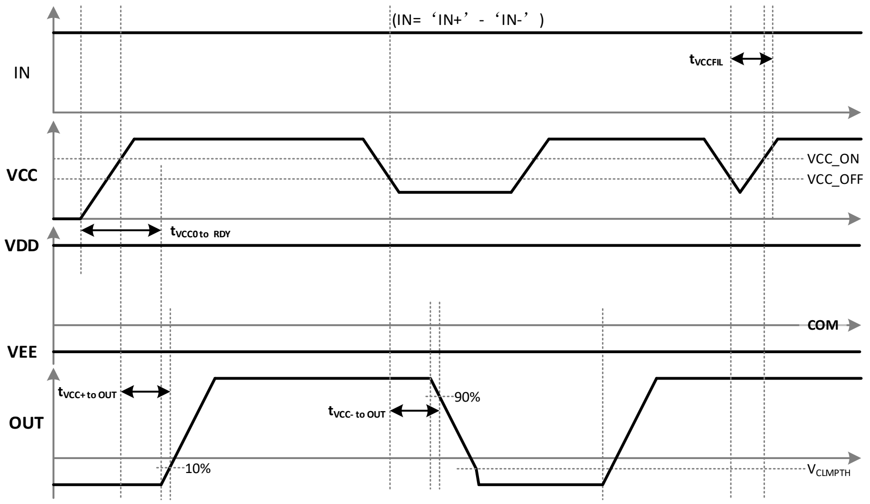


Figure 7-5 VCC UVLO timing diagram

7.4.2. VDD UVLO

Figure 7-6 shows the behavior of the driver outputs during VDD power-up and power-down, including UVLO ON/OFF threshold, deglitch filter, response timing diagram.

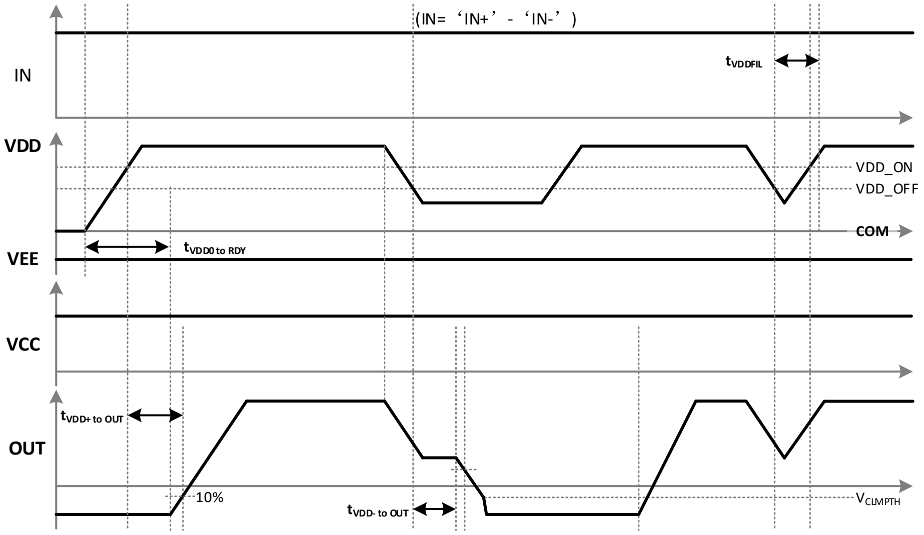


Figure 7-6 VDD UVLO timing diagram

7.5. CMTI Test Circuit

Figure 7-7, Figure 7-8 and Figure 7-9 are the CMTI test circuits for the different versions of CA-IS3212 devices.

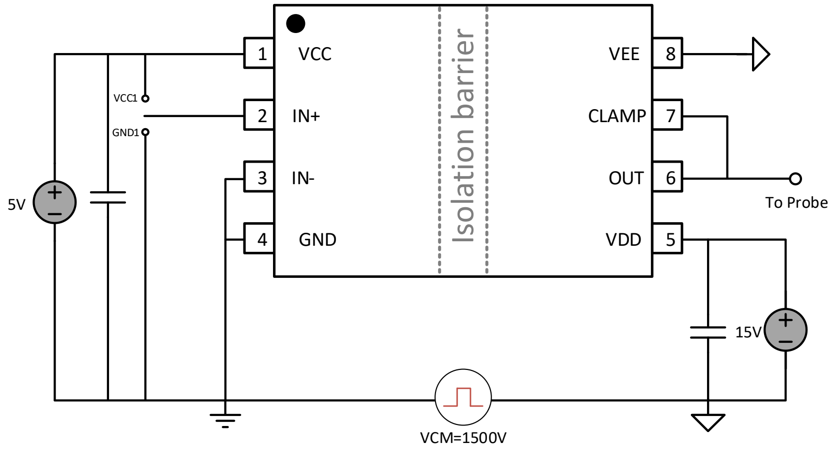


Figure 7-7 CMTI Test Circuit for CA-IS3212Mxx

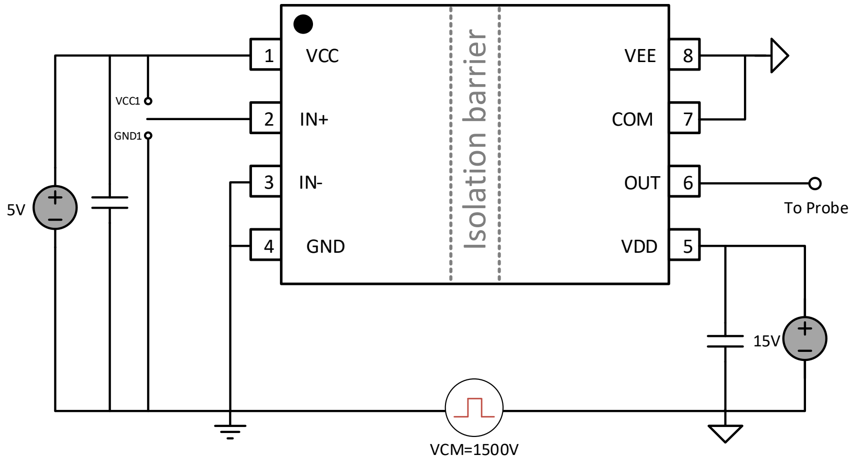


Figure 7-8 CMTI Test Circuit for CA-IS3212Vxx

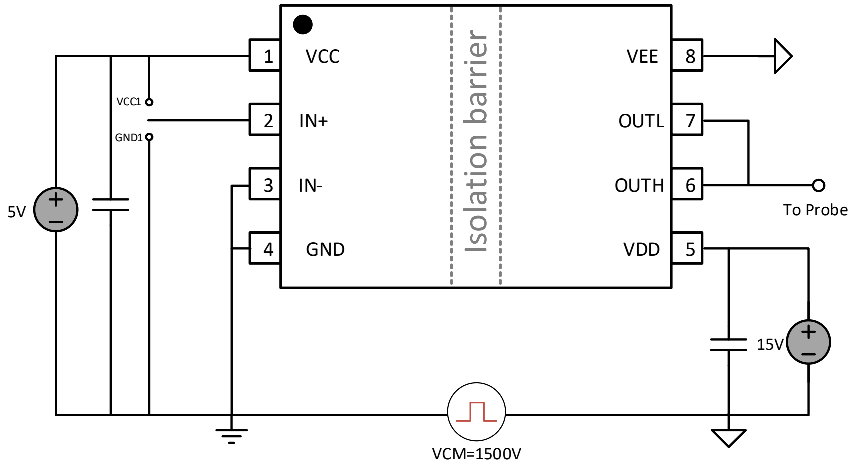


Figure 7-9 CMTI Test Circuit for CA-IS3212Sxx and CA-IS3212TSxx

8. Detailed Description

8.1. Overview

The CA-IS3212 devices are a family of single-channel isolated gate drivers capable of sinking 5A and sourcing 4A peak currents. Excellent dynamic performance and high-reliability make these devices ideal for Si MOSFET, IGBT, GaN and SiC MOSFET driving applications in the inverter, motor control or isolated power supply etc. systems. All devices have integrated digital galvanic isolation between control-side and driver-side using Chipanalog's proprietary SiO_2 capacitive isolation technology which features up to 5.7-kV_{RMS} isolation rating for the wide-body package devices and minimum common-mode transient immunity (CMTI) of 150kV/µs, supporting up to 1.5-kV_{RMS} isolation working voltage and 12.8-kV_{PK} surge rating.

The CA-IS3212 devices are optimized for SiC, GaN and IGBT switching operation to improve system reliability. The CA-IS3212Mxx features 5A internal active miller clamp; The CA-IS3212Vxx offers COM pin to support dual supplies at driver side; The CA-IS3212Sxx provides OUTH and OUTL split outputs. Both control-side supply (VCC) and driver-side supply (VDD – VEE) are internally monitored for undervoltage conditions with different UVLO detection threshold options, see Electrical Characteristics for more details.

8.2. Functional Block Diagram

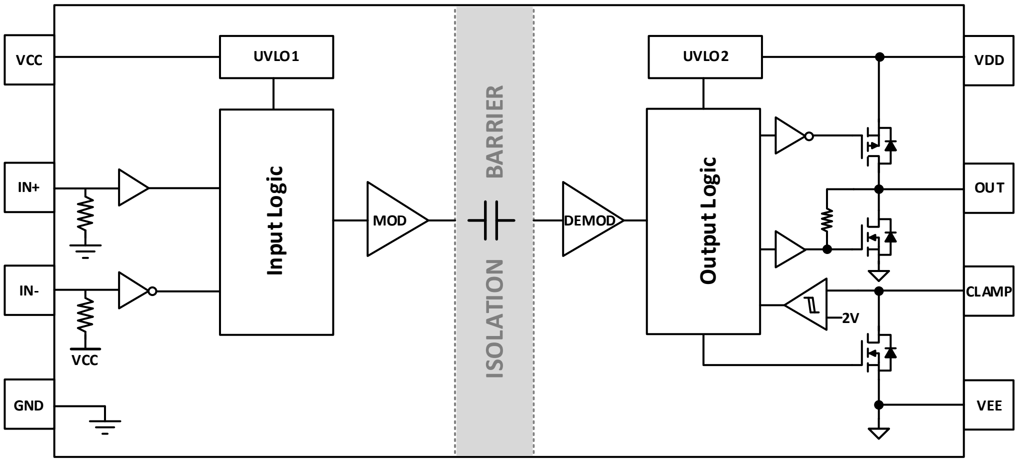


Figure 8-1 Simplified Block Diagram for CA-IS3212Mxx

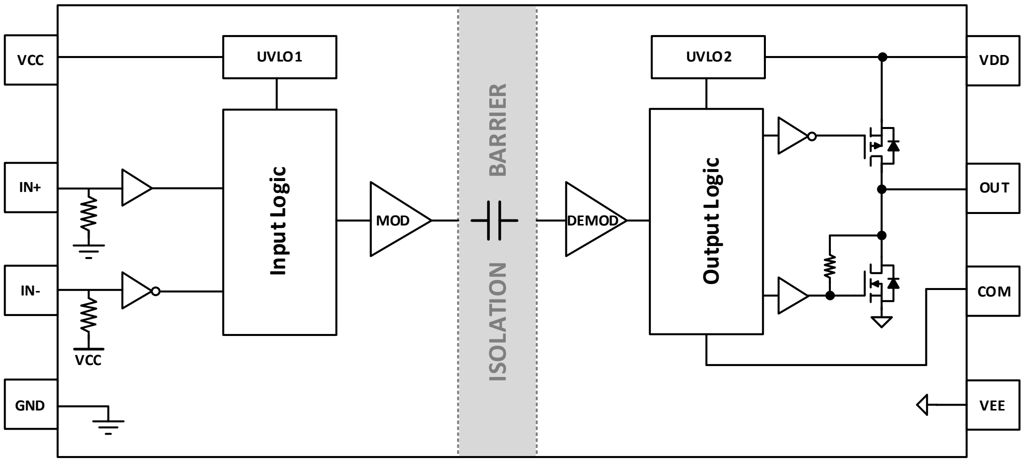


Figure 8-2 Simplified Block Diagram for CA-IS3212Vxx

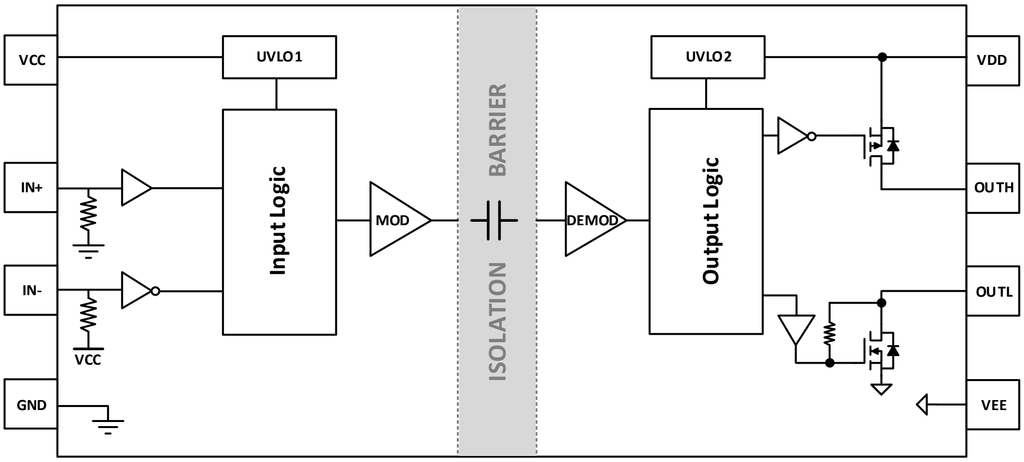


Figure 8-3 Simplified Block Diagram for CA-IS3212(T)Sxx

8.3. Power Supply

The CA-IS3212 devices accept 3.0V o 5.5V power supply input for control-side (VCC). On driver-side, the CA-IS3212 can operate with dual supplies or a single supply of wide voltage range of VDD – VEE up to 33V. For the operation with dual supplies, the power transistors are turned off with a negative voltage on their gate with respect to the emitter/source. This prevents the power transistors from unintentionally turning on because of current induced from the collector/drain to the gate due to Miller effect to improve system reliability.

8.4. Driver Output Stage

The driver output stage of the CA-IS3212 integrates a pull-up structure and a pull-down structure. They have distinct current sourcing/sinking (4A/5A) capabilities to drive the external transistors (GaN, SiC MOSFET and IGBT modules) directly. Figure 8-4 and Figure 8-5 show the output stage circuits, the pull-up circuit is only a P-channel MOSFET, R_{OUTH} is the on-resistance of the PMOS; The pull-down circuit is simply composed of an n-channel MOSFET. R_{OUTL} is the on-resistance of the NMOS.

The voltage of OUT (CA-IS3212Mxx, CA-IS3212Vxx) or OUTL for CA-IS3212(T)Sxx is pulled to VEE through the pull-down NMOS to turn off external power transistor. This very low pull-down resistance R_{OUTL} not only achieves high sinking current, reduces turn-off time, but also improves noise immunity considering Miller effect.

Because of the very low turn-on impedance of the output stage MOSFETs, the CA-IS3212 isolated gate drivers can provide rail-to-rail outputs (output voltage swings between VDD and VEE).

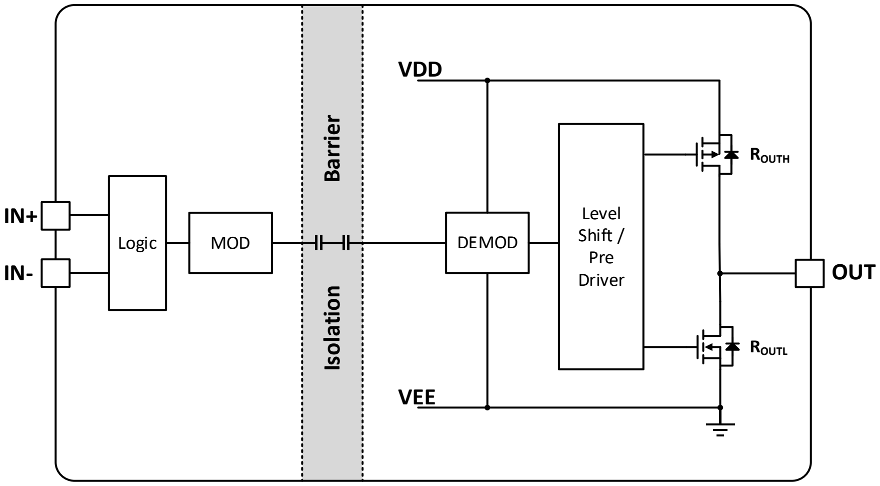


Figure 8-4 Gate-driver Output Stage of CA-IS3212Mxx and CA-IS3212Vxx

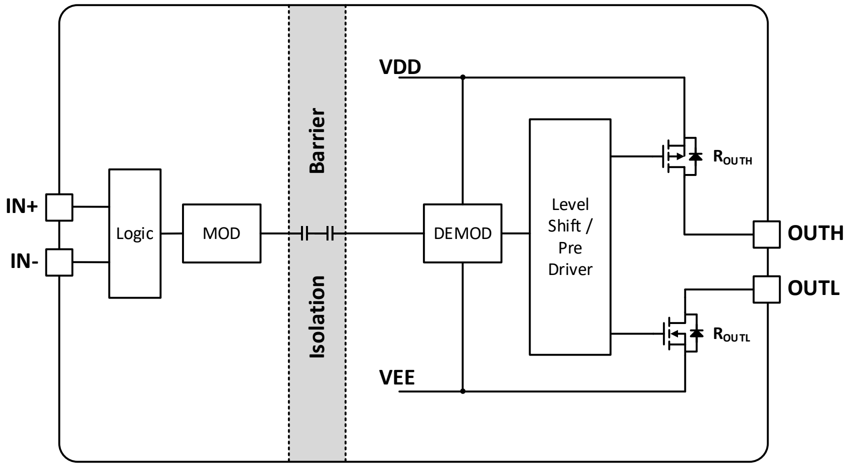


Figure 8-5 Gate-driver Output Stage of CA-IS3212(T)Sxx

8.5. Protection Functions

8.5.1. VCC and VDD Undervoltage Lockout (UVLO)

The CA-IS3212 devices feature undervoltage detection for both VCC and VDD supplies. The VDD UVLO is referenced to VEE (CA-IS3212Mxx, CA-IS3212(T)Sxx) or COM (CA-IS3212Vxx). Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. Once an undervoltage condition is detected on either supply, the output is set to logic-low to turn off the external power transistor, regardless of the IN+/IN– inputs state.

The CA-IS3212 devices integrate deglitch filter for both VCC UVLO and VDD UVLO detection to reject glitches and noise on the power supply, see Figure 7-5 and Figure 7-6 UVLO timing diagram for more details.

8.5.2. Active Pull-down

The CA-IS3212 device has an active pull-down function to turn-off the external power transistor when VDD is open, this prevents the external power transistor from wrong turning-on before the device gets back control normally. See Figure 8-6, when the driver output stage is powered off or VDD is open, the OUT pin will be set to high-impedance and clamped to VEE.

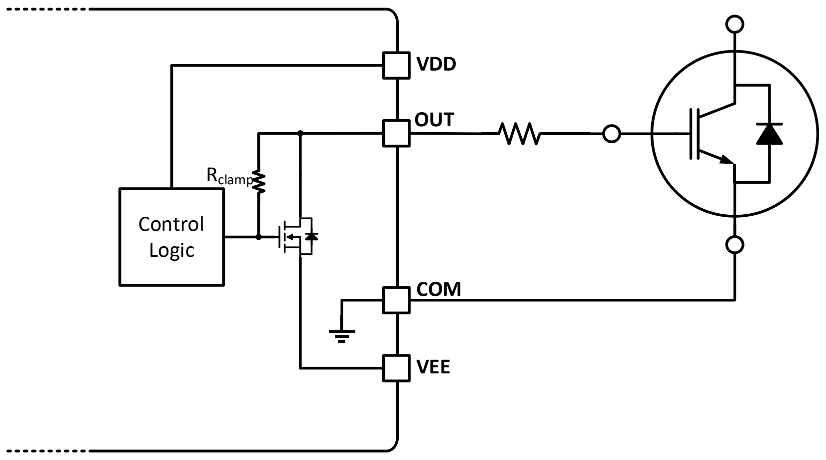


Figure 8-6 Active Pull-down

8.5.3. Short-Circuit Clamping

The output stage of the CA-IS3212 features internal short-circuit clamping function that clamps the driver's output (OUTH/OUTL) and CLAMP pin, pulling the OUTH/OUTL and CLAMP voltage slightly higher than VDD supply during short-circuit conditions. This functional circuit protects external transistors from gate-source or gate-emitter overvoltage breakdown. The internal diode between OUTH/OUTL/CLAMP and VDD can be used to provide larger current conduction capability at short time and ensure system reliability, see Figure 8-7 for more detail.

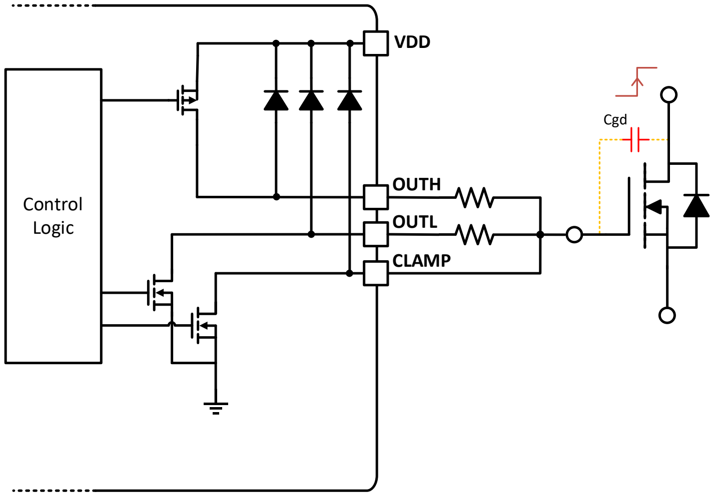


Figure 8-7 Short-Circuit Clamping

8.5.4. Internal Active Miller Clamp (CA-IS3212Mxx)

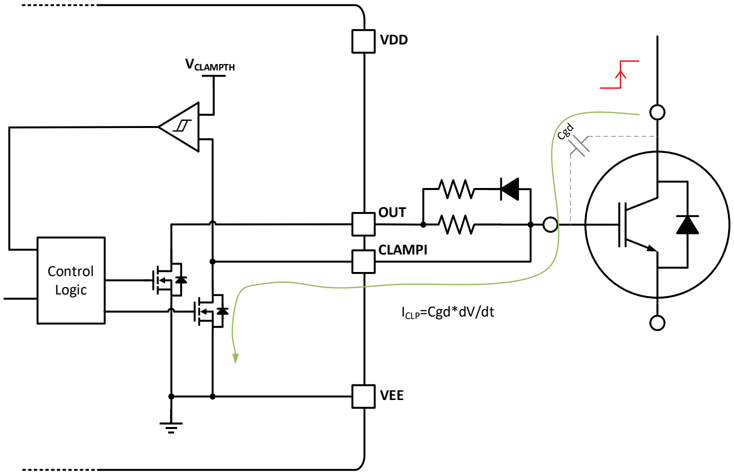


Figure 8-8 Active Miller Clamp

The CA-IS3212Mxx features internal active Miller clamp protection as shown in Figure 8-8 to prevent the false turn-on while the gate-driver is off. In the synchronous rectifier operation, the body diode conducts the current during deadtime while a power transistor is off, the drain-source or collector-emitter voltage remains the same. High dv/dt occurs when another power transistor turns on. The low internal pull-down resistance of the CA-IS3212Mxx offers strong pull-down which keeps OUT to low-level, close to VEE voltage. However, in the typical application circuit, an external gate resistor is used to limit the dv/dt current. During turn-on transient of other power transistor, Miller effect can cause a voltage drop on the external gate resistor, which boost the collector-emitter voltage or gate-source voltage. Once this voltage reaches or is higher than the turn-on threshold voltage of power transistor, will cause shoot through and damage the external power devices. In this case, the internal Miller clamp of CA-IS3212Mxx can provide effective protection. For example, when the high-side power transistor turns on after the low-side transistor is off, the internal Miller clamp MOSFET starts to engage when the Miller clamp pin voltage drops below

V$_{CLAMPTH}$ (2V referenced to VEE) threshold, providing a low-impedance path to direct the Miller current to VEE. Refer to Figure 8-8 for the internal Miller clamp timing diagram.

8.5.5. Shoot Through Protection (STP)

The CA-IS3212 isolated gate drivers feature shoot through protection, which prevents shoot-through conditions caused by the simultaneous conduction of the high-side and low-side switches in the typical application. The CA-IS3212MYS has 80ns fixed dead time, while other devices have 200ns fixed dead time. Connect IN– pin to GND could disable STP function. If input's "dead time" from controller is longer than internal dead time of CA-IS3212, the driver's dead time is the input's dead time. If input's "dead time" from controller is shorter than internal dead time of CA-IS3212, the driver's dead time is the internal dead time. The shoot through protection timing diagram is shown in Figure 8-9. The internal dead time is asserted by input (PWMA or PWMB) signal's falling edge. The PWMA and PWMB in Figure 8-9 are the control signals in the half bridge configuration, please refer to Figure 9-4 for more details.

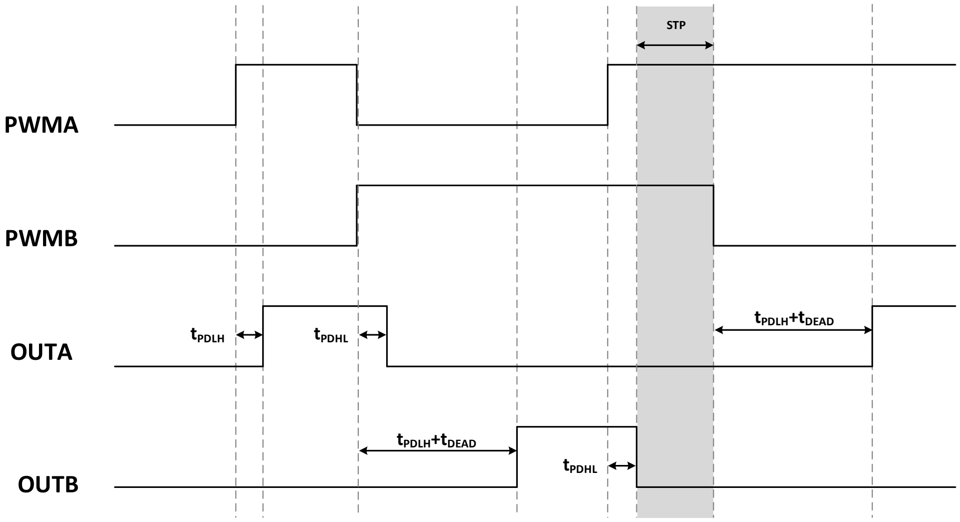


Figure 8-9 Shoot Through Protection Timing Diagram

8.6. Device Functional Modes

Table 8-1 to Table 8-3 show the functional modes for the different versions of the CA-IS3212 devices.

Table 8-1 Inputs vs. Output Truth Table of CA-IS3212(T)Sxx[1]

CONDITION	INPUT		OUTPUT	
	IN+	IN–	OUTH	OUTL
VCC ≥ V_{VCC_ON} and VDD ≥ V_{VDD_ON}	L	X	Hi-Z	L
	X	H	Hi-Z	L
	H	L	H	Hi-Z
VCC < V_{VCC_OFF} or VDD < V_{VDD_OFF}	X	X	Hi-Z	L

Table 8-2 Inputs vs. Output Truth Table of CA-IS3212Mxx[1]

CONDITION	INPUT		OUTPUT	
	IN+	IN–	OUT	CLAMP
VCC ≥ V_{VCC_ON} and VDD ≥ V_{VDD_ON}	L	X	L	OUT < 2V, pull-down
	X	H	L	OUT < 2V, pull-down
	H	L	H	Hi-Z
VCC < V_{VCC_OFF} or VDD < V_{VDD_OFF}	X	X	L	L

Table 8-3 Inputs vs. Output Truth Table of CA-IS3212Vxx[1]

CONDITION	INPUT		OUTPUT
	IN+	IN–	
VCC ≥ V_{VCC_ON} and VDD ≥ V_{VDD_ON}	L	X	L
	X	H	L
	H	L	H
VCC < V_{VCC_OFF} or VDD < V_{VDD_OFF}	X	X	L

Notes:

1. H = High; L = Low; Hi-Z = High Impedance; X = Irrelevant.

9. Application and Implementation

9.1. Typical Application

The CA-IS3212 isolated gate drivers are designed to drive power MOSFET, IGBT, Silicon-Carbide (SiC) transistors in various power supply systems to optimize system cost, size and efficiency. High current-driving capability and reinforced insulation, combined with advanced protection functions, make the CA-IS3212 ideal for the industrial applications, such as HEV/EV inverter, motor drivers, solar inverters, UPS and industrial power modules etc. The typical application of CA-IS3212Mxx is shown in Figure 9-1. The typical application of CA-IS3212(T)Sxx is shown in Figure 9-2. The typical application of CA-IS3212Vxx is shown in Figure 9-3.

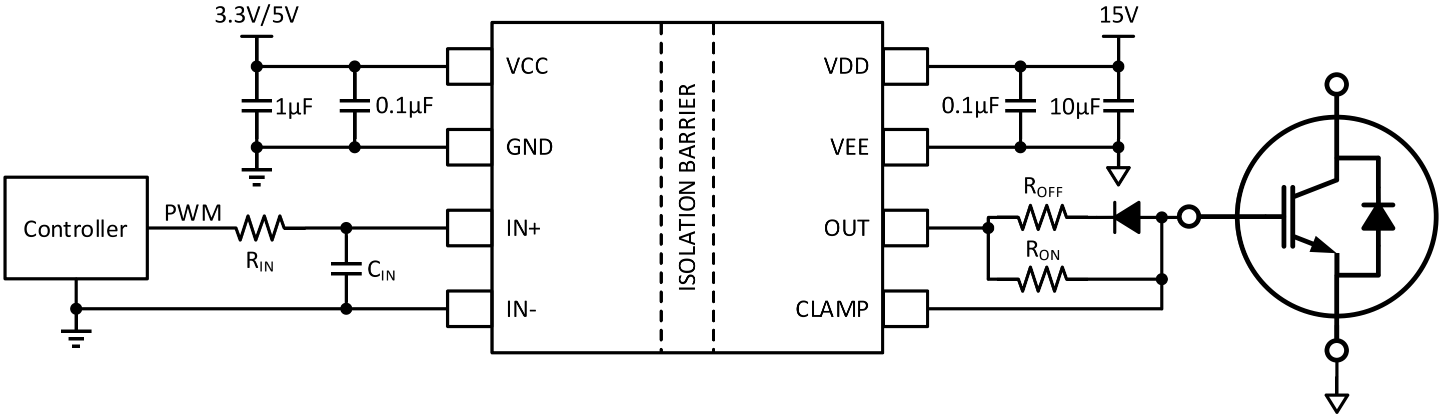


Figure 9-1 Typical Application of CA-IS3212Mxx

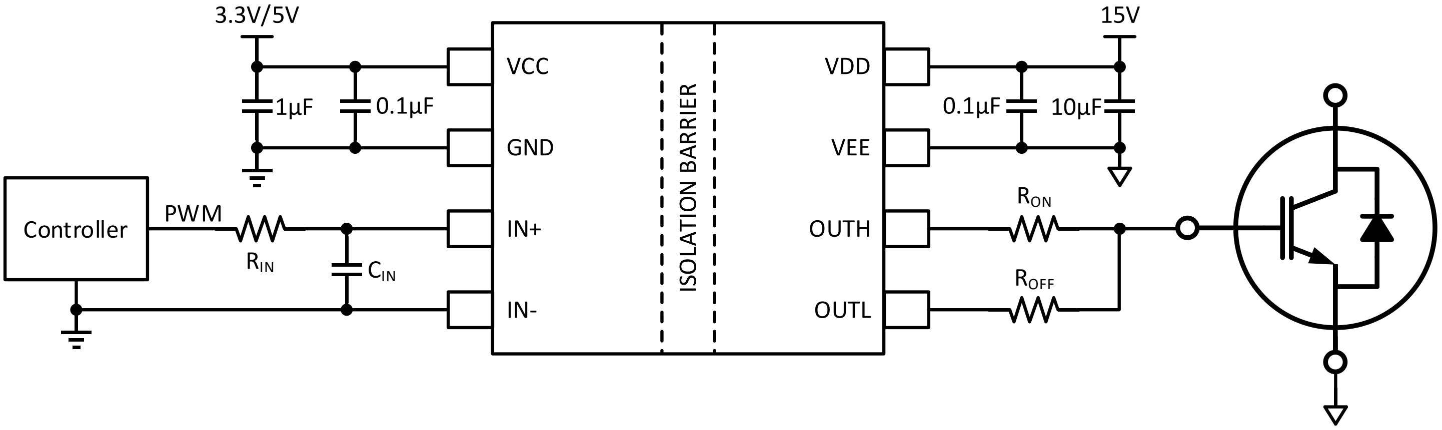


Figure 9-2 Typical Application of CA-IS3212(T)Sxx

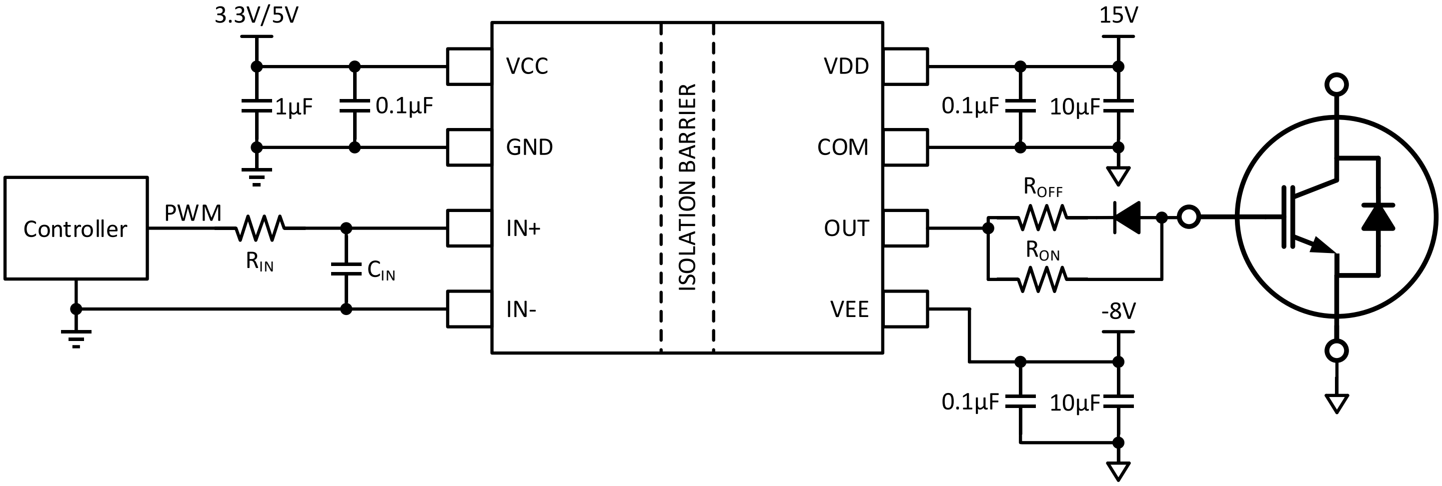


Figure 9-3 Typical Application of CA-IS3212Vxx

9.2. Power Supply Design

The VDD and VEE supplies provide gate-driver peak current driving support. We recommend to bypass VDD to VEE (or COM for CA-IS3212Vxx) with at least 10µF/50V capacitor, for the CA-IS3212Vxx, also bypass VEE to COM with a 10µF/50V capacitor to sink 5-A peak current and source 4-A peak current. On the control-side, bypass VCC to GND with at least 1µF capacitor. It is recommended to add an additional 0.1µF bypass capacitor for each power supply to reject high-frequency noise. Low ESR and ESL capacitors should be selected to avoid high-frequency noise, and this small capacitor should be placed as close as possible to the VCC, VDD and VEE pins to reduce parasitic coupling noise.

9.3. Input Filters

The CA-IS3212 has a built-in 40ns deglitch filter on the IN+ pin, so any signal less than 40ns (typical) can be filtered out of the input pin. For noisy motor driver or traction inverter systems, additional RC low-pass filters can be added externally to the input pins, effectively increasing noise immunity and signal integrity. The IN+ and IN– pins should not be left open when not in use. If IN+ is used only for in-phase input control in the configuration, IN– should be shorted to GND. The purpose of the low-pass filter is to filter out high-frequency noise generated by PCB parasitics. When selecting low-pass filter resistors and capacitors, the noise suppression effect and added delay time should be considered according to the system requirements.

9.4. PWM Interlock Configuration

In the typical applications, the gate drivers are used to drive high-side and low-side power transistors. External controller (DSP/MCU) generates complementary PWM pulses during normal operation. However, the controller failures or software faults can cause both the high-side and low-side PWM signals to be latched high. Interlock configuration can be used to prevent the output from being high at same time even both high-side and low-side inputs are pulled high. As shown in Figure 9-4, PWMA is high-side PWM control signal and PWMB is low-side PWM control signal. Apply PWMA signal to high-side IN+ pin and low-side IN– pin; Apply PWMB signal to high-side IN– pin and low-side IN+ pin. When PWMA and PWMB are pulled to high level at same time, both gate drivers’ outputs will be placed to low level to turn off external transistors. This architecture prevents both low-side and high-side gate-driver inputs from being "high" at the same time, preventing shoot through in half bridge configuration.

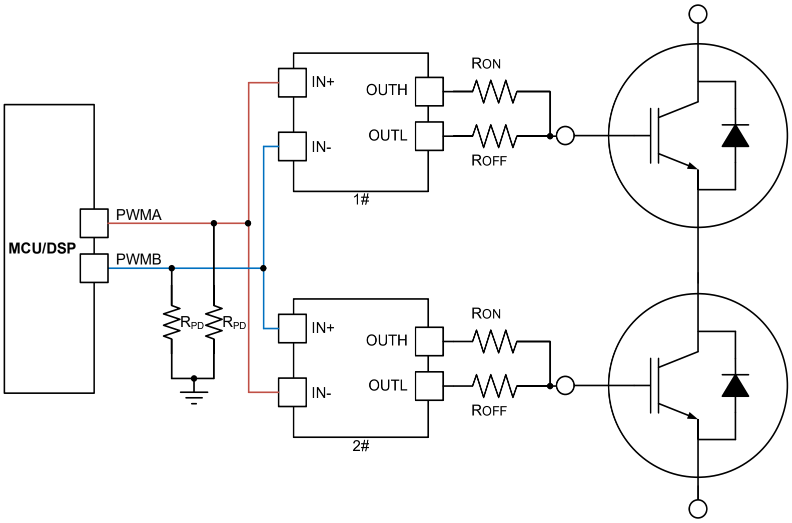


Figure 9-4 Half-bridge PWM Interlock Configuration for CA-IS3212(T)Sxx

9.5. Gate Driver Resistors Selection

Take CA-IS3212(T)Sxx as an example, there are two external gate driver resistors (R_{ON} and R_{OFF}, see Figure 9-2) in the typical application, where R_{OFF} is the external turn-off resistor and R_{ON} is the external turn-on resistor. These two resistors are chosen to limit the current ringing caused by fast switching and parasitic inductances and capacitances, and to reduce EMI. Also, R_{ON} and R_{OFF} can be used to fine-tune gate driving capability and optimize the switching loss. The selection of gate drive resistor is mainly based on three factors: driving current, switch loss, rise and fall time. The peak-current of gate driving is calculated as follows.

I_{OUTH} peak source current:

$$I_{OUTH} = \min\left[4A, \frac{VDD - VEE}{(R_{OUTH} + R_{GON} + R_{GFETint})}\right]$$

I_{OUTL} peak sink current:

$$I_{OUTL} = \min\left[5A, \frac{VDD - VEE}{(R_{OUTL} + R_{GOFF} + R_{GFETint})}\right]$$

Where:

- R_{OUTH} is internal pull-up resistance (about 1.1Ω);
- R_{OUTL} is internal pull-down resistance (about 0.6Ω);
- R_{GON} is the external turn-on resistor;
- R_{GOFF} is the external turn-off resistor;
- $R_{GEFTInt}$ is the gate resistance of the external power transistor, which is available from power transistor’s datasheet.

9.6. Power Supply and PCB Layout

9.6.1. Power Supply Decoupling

The CA-IS3212 devices operate in wide supply range. The control-side (VCC) accepts 3V to 5.5V supply range, and the driver-side (VDD) supports both unipolar and bipolar power supply up to 33V (VDD – VEE). For operation with bipolar supplies, the power transistors are turned off with a negative voltage on their gate with respect to the emitter/source. This prevents the power transistors from unintentionally turning on because of the current induced from the collector/drain to the gate due to Miller effect. These devices do not require special power-supply sequencing. However, enough supply bypassing and device grounding are extremely important.

During external power transistors' turn on or turn off, higher peak current may cause voltage drop at VDD or VEE. To reduce power supply ripple and ensure the normal operation of gate driver, bypass VDD to VEE (or COM for CA-IS3212Vxx) with at least a 10-µF and a 0.1-µF low-ESR, low-ESL capacitors with sufficient voltage rating in parallel. For the CA-IS3212Vxx application circuit, also bypass VEE to COM with at least a 10-µF and 0.1-µF capacitors with sufficient voltage rating in parallel. To ensure the best performance, place the bypass capacitors as close to the power-supply pins as possible. On the control-side, it is recommended to bypass VCC to GND with a 0.1-µF and a 1-µF capacitors in parallel.

9.6.2. PCB Layout Guidelines

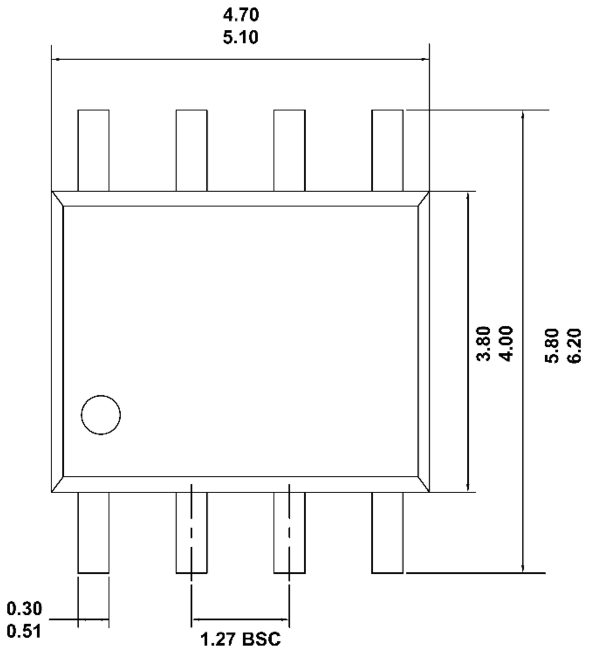
Due to the strong drive strength of the CA-IS3212, proper PCB layout is essential. The PCB designer should follow some critical recommendations as below in order to get the best performance.

- Place the external transistor as close to the gate driver as possible to decrease the trace inductance and avoid output ringing.
- To ensure the best performance, provide maximum peak current driving and keep lower supply ripple, place the decoupling capacitors as close to the power-supply pins (VCC, VDD, VEE) as possible. The peak current generated at each switching transient can cause high di/dt and voltage spike on the parasitic inductance of PCB traces. We recommend to use low ESR and low ESL capacitors.
- The Kelvin method is recommended to connect VEE (or COM for CA-IS3212Vxx) to the source of SiC MOSFET or emitter of IGBT. If the power transistor does not have a split Kelvin source or emitter, connect VEE (or COM) as close as possible to the source or emitter terminal of the power device and separate the gate loop from the high power switching loop.
- If the gate driver is used for the low-side driving which the VEE (or COM for CA-IS3212Vxx) pin is connected to the negative supply of power bus. Use a solid ground plane on driver-side to shield the output signals from the noise generated by the switching-node; if the gate driver is used for the high-side driving which the VEE or COM pin is connected to the switching-node, ground plane is not recommended.
- Keep the control input traces as short as possible. To maintain low signal-path inductance, vias should be avoided. Have a solid ground plane on the control-side to shield the input signals.
- To ensure isolation performance between the control-side and driver-side, on the top layer and bottom layer keep enough space under the CA-IS3212 devices.

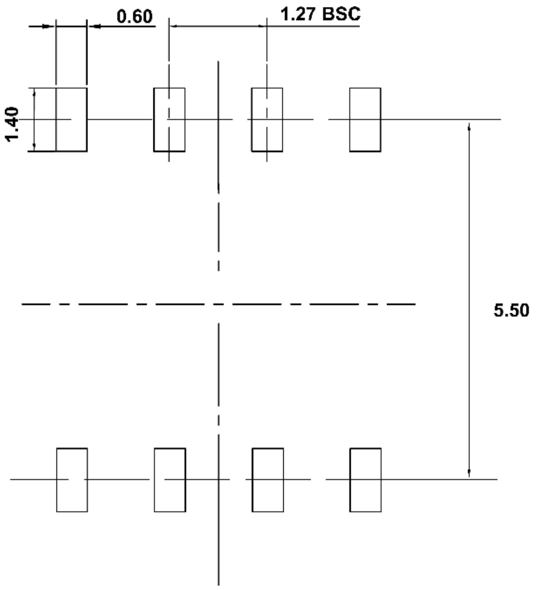
10. Package Information

10.1. SOIC8 Package

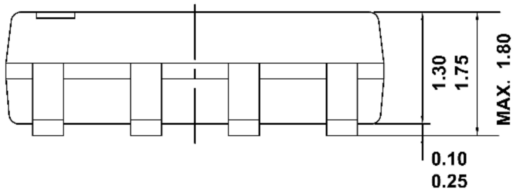
All values for the dimensions are shown in millimeters, angles are in degrees.

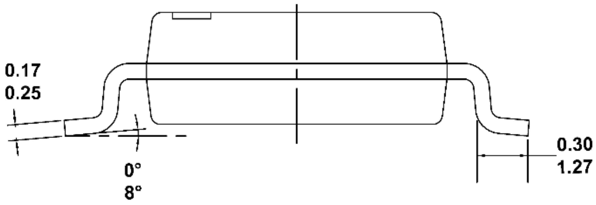


TOP VIEW



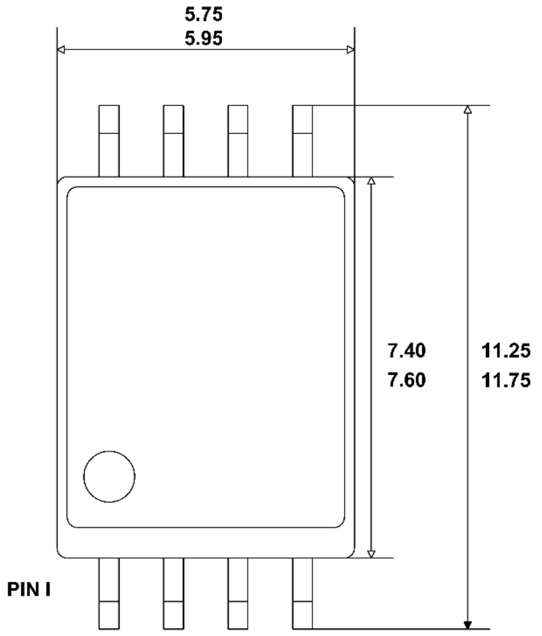
RECOMMENDED LAND PATTERN



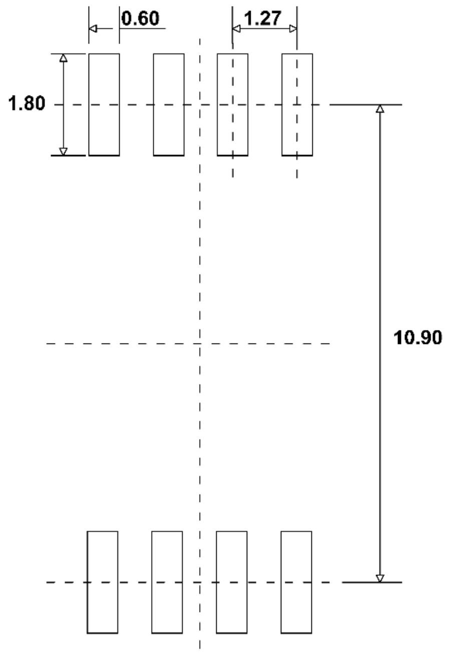


10.2. SOIC8-WB Package

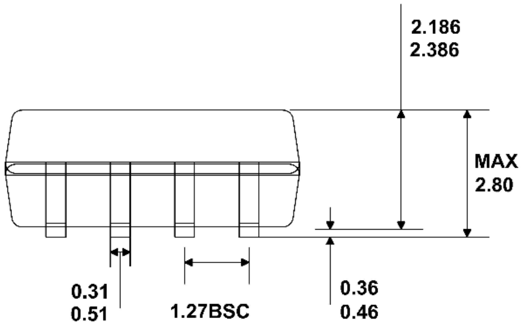
All values for the dimensions are shown in millimeters, angles are in degrees.



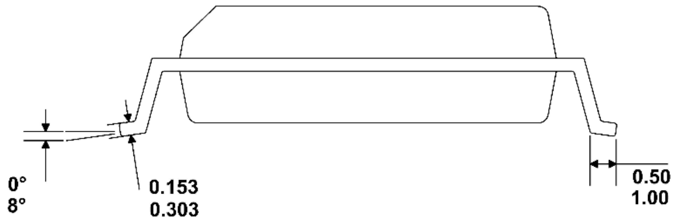
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

11. Soldering Information

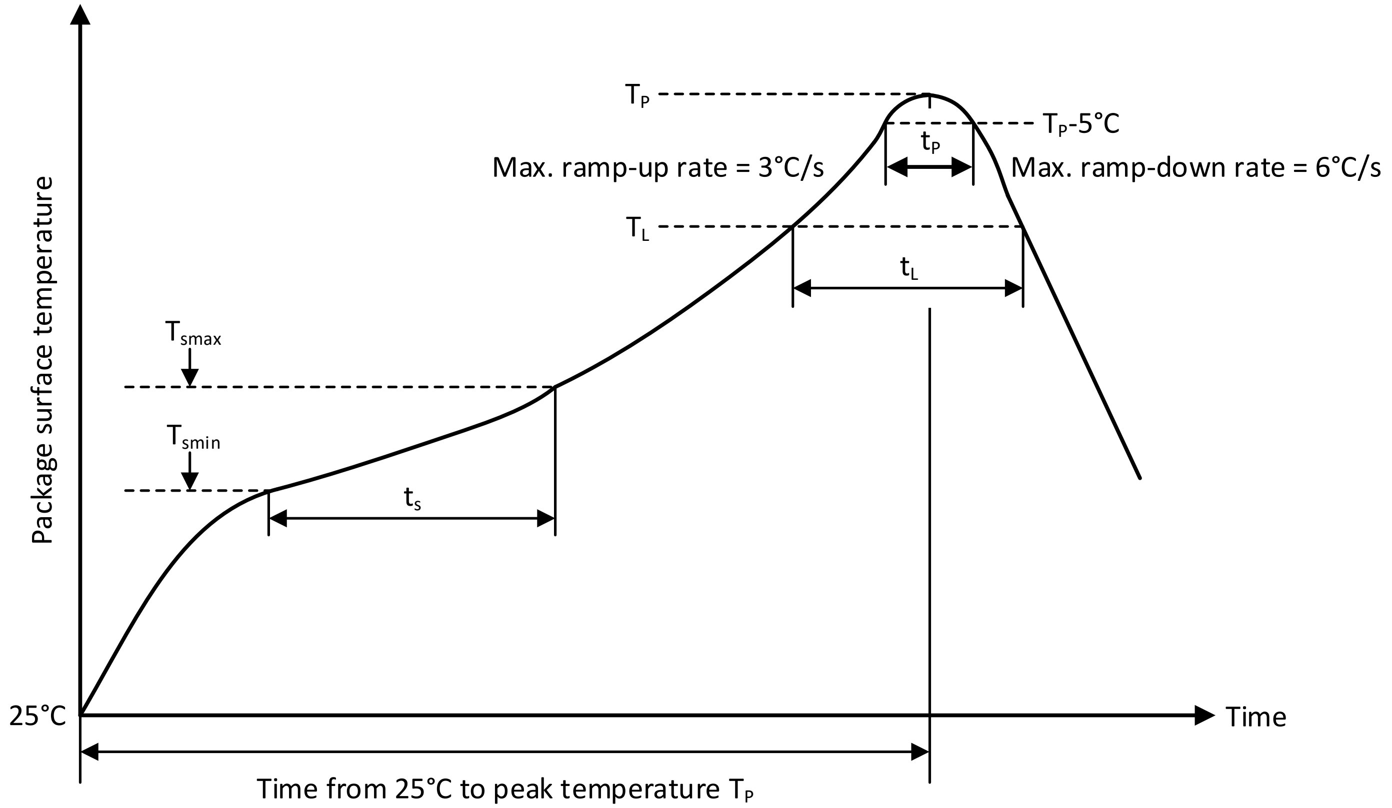


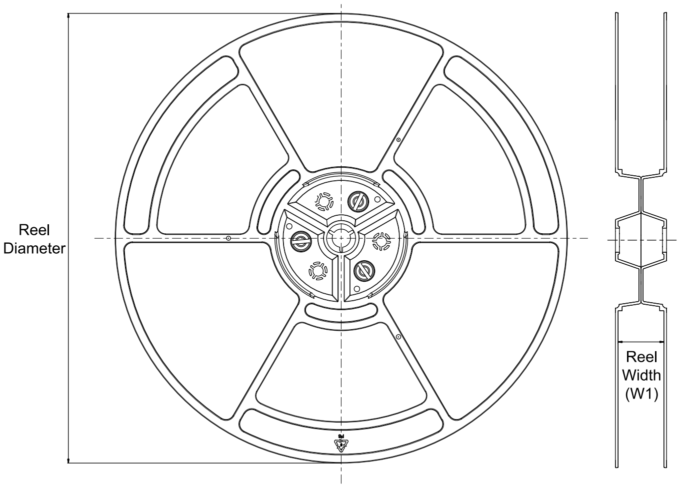
Figure 11-1 Soldering Temperature Profile (Reflow)

Table 11-1 Soldering Temperature Parameters

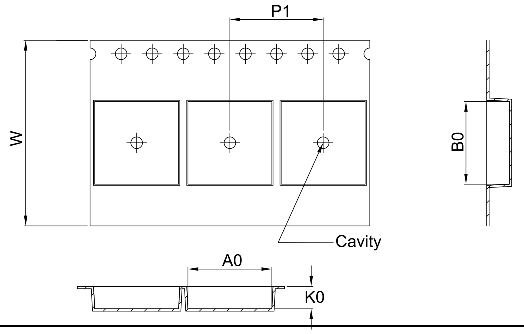
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

12. Tape and Reel Information

REEL DIMENSIONS

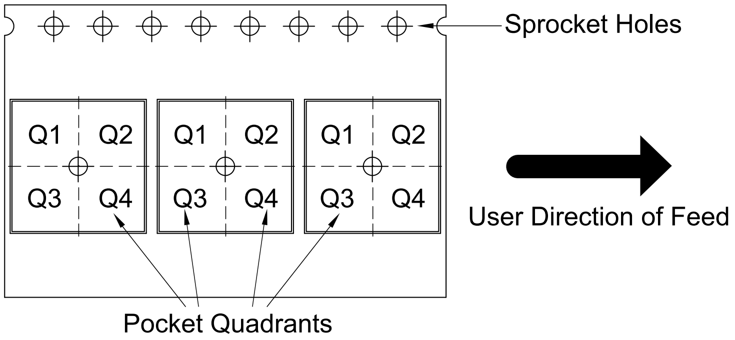


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3212MYS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3212MBS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3212MCS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3212SBS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3212SCS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3212VCS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IS3212MBG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3212MCG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3212SBG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3212SCG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3212VCG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3212TSCG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1

13. Revision History

Revision	Description	Revised Date	Page Changed
Version 1.00	Initial version	2025/03/29	NA
Version 1.01	Add new part number: CA-IS3212TSCG Update Recommended Operating Conditions Update Safety-Related Certifications: UL completed	2026/06/04	1, 2, 7, 11, 32 7 10

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