CA-IS3211MxG 5A Source/Sink Current, 5.7-kV$_{RMS}$ Built-in Miller Clamp, Opto-Compatible Single-Channel Isolated Gate Driver

1. Key Features

- 5.7-kV$_{RMS}$ Opto-Compatible Single-Channel Isolated Gate Driver
- Output Peak Current: 5A Source / 5A Sink
- Built-in Active Miller Clamp With 5A Peak Current
- Maximum 33V Output Drive Power Supply Voltage
- 8V or 12V V_{CC} Undervoltage Lockout Threshold Options
- Rail-to-Rail Output
- Timing Characteristics:
  - 75ns (Typ) Propagation Delay
  - 25ns (Max) Part-to-Part Propagation Delay mismatch
  - 35ns (Max) Pulse Width Distortion
- High Common-Mode Transient Immunity (CMTI): ±150kV/μs (Min)
- Isolation Barrier Lifetime Greater Than 40 Years
- Up to 7V Reverse Voltage on Input-Stage, With Interlock Input Support
- Wide-body SOIC8-WB Package
- Extended Industrial Temperature Range (T_A): –40°C to 125°C
- Safety-Related Certifications:
  - DIN EN IEC 60747- 17 (VDE 0884-17):2021-10
  - UL certification per UL 1577
  - CQC certification per GB4943.1-2022
  - TUV certification per EN 62368-1 and EN 61010-1

2. Applications

- Industrial Motor Control Drives
- Industrial Uninterruptible Power Supplies (UPS)
- Solar Inverters
- Energy Storage Converter
- Charging Pile

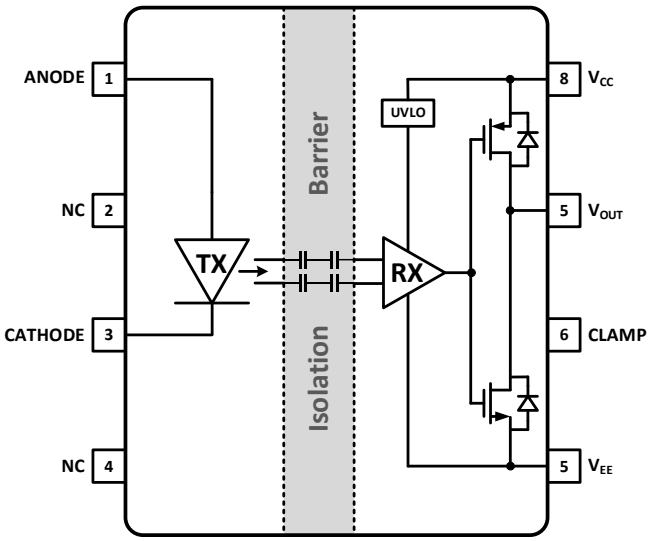
3. Description

CA-IS3211M is a single-channel isolated gate driver with built-in Miller clamp and opto-compatible input, which can be used to drive MOSFET, IGBT, and SiC power devices. The device features an isolation voltage rating of 5.7kV$_{RMS}$, meets with reinforced insulation, and provides 5A source and 5A sink peak output current capability. It also integrates an active Miller clamp with 5A peak current, making it particularly suitable for driving SiC power transistors. The wide power supply voltage range of up to 33V allows the use of bipolar supplies to effectively drive IGBT and SiC power devices. Performance highlights of the device include: high common-mode transient immunity (CMTI), low propagation delay, and low pulse width distortion. Strict process control ensures excellent device consistency. The device input stage uses a diode emulator, which, compared to the LED in traditional optocoupler isolated gate drivers, has no light degradation effect, offering better long-term reliability and stability, while supporting an extended industrial temperature range from –40°C to 125°C. The high performance and high reliability make the device suitable for motor drives, solar inverters, industrial power supplies, and charging piles. CA-IS3211M can drive power transistors on both the high-side and low-side, fully compatible with traditional optocoupler isolated gate drivers while significantly improve drive performance.

Device Information

Part Number	Package	Body Size (Nom)
CA-IS3211MBG	SOIC8-WB (G)	5.85mm x 7.50mm
CA-IS3211MCG	SOIC8-WB (G)	5.85mm x 7.50mm

Simplified Functional Block Diagram



4. Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Output Mode	UVLO Voltage (V)	Miller Clamp Current (A)	Isolation Rating (V_{RMS})	Package
CA-IS3211MBG	Single Vout Pin	8	5	5700	SOIC8-WB (G)
CA-IS3211MCG	Single Vout Pin	12	5	5700	SOIC8-WB (G)

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5. Pin Descriptions and Functions

Figure 5-1 Pin Configuration

Table 5-1 Pin Descriptions and Functions

Pin Name	Pin Number	Type [1]	Description
ANODE	1	I	Anode
NC	2	--	No internal connection, can be left floating or connected to ANODE or CATHODE
CATHODE	3	I	Cathode
NC*	4	--	Internally connected to CATHODE, can be left floating or connected to CATHODE
VEE	5	P	Negative output stage power rail
CLAMP	6	I	Miller clamp input, connect this pin directly to the gate of the power transistor
VOUT	7	O	Gate drive output
VCC	8	P	Positive output stage power rail

Note:
1. P = power, I = input, O = output.

6. Specifications

6.1. Absolute Maximum Ratings[1]

Over operating free-air temperature range unless otherwise specified.

Parameter		Min	Max	Unit
$I_{F(AVG)}$	Average Input Current	–	25	mA
$I_{F(TRAN)}$ < 1us pulse, 300pps	Transient Peak Input Current		1	A
$V_{R(MAX)}$	Reverse Input Voltage		7	V
V_{CC} – V_{EE}	Output Power Supply Voltage	–0.3	36	V
V_{OUT}	Output Signal Voltage	V_{EE} – 0.3	V_{CC} + 0.3	V
T_{J2}	Junction Temperature	–40	150	°C
T_{stg}	Storage Temperature	–65	150	°C

Note:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. To maintain the recommended operating junction temperature conditions, see Thermal Information.

6.2. ESD Ratings

Parameter			Value	Unit
V_{ESD}	Electrostatic Discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	±3500	V
		Charged Device Model (CDM), per JEDEC Standard JESD22-C101	±2000	

6.3. Recommended Operating Conditions

Parameter			Min	Typ	Max	Unit
V_{CC}	Output Power Supply Voltage (V_{CC} – V_{EE})	CA-IS3211MCG	14		33	V
		CA-IS3211MBG	10		33	V
$I_{F(ON)}$	Input Diode Forward Current (Diode "On")		7		16	mA
$V_{F(OFF)}$	Positive Voltage - Negative Voltage (Diode "Off")		–5.5		0.9	V
T_J	Junction Temperature		–40		150	°C
T_A	Ambient Temperature		–40		125	°C

6.4. Thermal Information

Thermal Parameter		SOIC8-WB (G)	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	110.1	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	51.7	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance	66.4	°C/W

6.5. Power Dissipation Rating

Parameter		Test Conditions	Min	Typ	Max	Unit
P_D	Maximum Input and Output Power Dissipation[1]	V_{CC} = 20V, I_F = 10mA 10-kHz, 50% duty cycle, square wave, 180nF load, T_A = 25°C			750	mW
P_{D1}	Max Input Power Dissipation[2]				10	mW
P_{D2}	Max Output Power Dissipation				740	mW

Notes:

1. Derate at 6mW/°C above 25°C ambient temperature;
2. The maximum P_{D1} = 40mW and the absolute maximum rating of P_{D1} is 55mW.

6.6. Safety Limits

Parameter		Test Conditions	Min	Typ	Max	Unit
I_S	Safety Input, Output, or Total Supply Current	$R_{\theta JA}$ = 110.1°C/W, V_I = 15V, T_J = 150°C, T_A = 25°C			75	mA
		$R_{\theta JA}$ = 110.1°C/W, V_I = 30V, T_J = 150°C, T_A = 25°C			37	
P_S	Safety Input, Output, or Total Power	$R_{\theta JA}$ = 110.1°C/W, T_J = 150°C, T_A = 25°C			1135	mW
T_S	Maximum Safety Temperature[1]				150	°C

Note:

1. $T_{J(max)} = T_S = T_A + R_{\theta JA} * P_S$, where $T_{J(max)}$ is the maximum allowable device junction temperature. $P_S = I_s * V_{IN}$, where V_{IN} is the maximum operating voltage.

6.7. Insulation Specifications

Parameter		Test Conditions	Value	Unit
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	>8.2	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	>8.2	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ $300V_{RMS}$	I-IV	
		Rated mains voltage ≤ $600V_{RMS}$	I-IV	
		Rated mains voltage ≤ $1000V_{RMS}$	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	8000	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin(2πft), f = 1MHz	~ 0.6	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5700	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

6.8. Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021.	Certified according to UL 1577 component recognition program	Certified according to GB4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
Reinforced insulation: V_{IOTM}: 8000V_{PK} V_{IORM}: 2121V_{PK} V_{IOSM}: 12800V_{PK}	Single insulation protection 5700V_{RMS}	Reinforced Insulation (Altitude ≤ 5000m)	EN 62368-1: 5700V_{RMS} EN 61010-1: 5700V_{RMS}
Certificate Number: Pending	Certificate Number: Pending	Certificate Number: COC24001452438	Customer Reference Number: 2253313 (Pending)

6.9. Electrical Characteristics

Unless otherwise specified, all typical values are at T_A = 25°C, V_{CC} = 15V, V_{EE} = GND. All minimum and maximum values are results under recommended operating conditions (T_A = –40 to 125°C, $I_{F(on)}$ = 7mA to 16mA, V_{EE} = GND, V_{CC} = 14V to 33V, $V_{F(off)}$ = –5V to 0.8V).[1]

Parameter		Test Conditions	Min	Typ	Max	Unit
Input						
I_{FLH}	Input Forward Current Threshold (Low to High)	V_{out} > 5V, Cg = 1nF	1.5	2.55	4	mA
V_F	Input Forward Voltage	I_F = 10mA	1.8	2.1	2.4	V
V_{F_HL}	Input Voltage Threshold (High to Low)	V < 5V, Cg = 1nF	0.9			V
$\Delta V_F/\Delta T$	Temperature Coefficient of Input Forward Voltage	I_F = 10mA		1.5	1.8	mV/°C
V_R	Input Reverse Breakdown Voltage	I_R = 10µA	7			V
C_{IN}	Input Capacitance	F = 0.5MHz		15		pF
Output						
I_{OH}	Output Peak Source Current	I_F = 10mA, V_{CC} = 15V, C_{LOAD} = 0.18µF, C_{VDD} = 10µF, Pulse Width < 10µs; See Figure 8-2	3.5	5		A
I_{OL}	Output Peak Sink Current	V_F = 0V, V_{CC} = 15V, C_{LOAD} = 0.18µF, C_{VDD} = 10µF, Pulse Width < 10µs; See Figure 8-2	3.5	5		A
V_{OH}	High-level Output Voltage	I_F = 10mA, I_O = –20mA (relative to V_{CC})	–40	–20		mV
		I_F = 10mA, I_O = 0mA (relative to V_{EE})		V_{CC}		V
V_{OL}	Low-level Output Voltage	V_F = 0V, I_O = 20mA		10	25	mV
I_{CC_H}	Output Power Supply Current (Diode On)	I_F = 10mA, I_O = 0mA		1.4	2.1	mA
I_{CC_L}	Output Power Supply Current (Diode Off)	V_F = 0V, I_O = 0mA		1.3	2	mA
Active Pull-Down						
V_{OUTPD}	Active Pull-Down at V_{OUT}	I_{OUT} = 0.5A, V_{CC} = OPEN		2.0		V
Internal Active Miller Clamp						
$V_{CLAMPTH}$	Miller Clamp Threshold Voltage	Reference V_{EE}	1.5	2.0	2.5	V
V_{CLAMP}	Output Low Clamp Voltage	I_{CLAMP} = 20mA		11		mV
I_{CLAMP}	Output Low Clamp Peak Current	V_{CLAMP} = 0V, VEE = –4V		5		A
R_{CLAMP}	Miller Clamp Pull-Down Resistance	I_{CLAMP} = 0.2A		0.55		Ω
t_{DCLAMP}	Miller Clamp Turn-On Delay Time[2]	C_L = 1.8nF, see Figure 9-3		20	50	ns
Short-Circuit Clamp[2]						
$V_{CLP-OUT}$	V_{OUT} – V_{CC}	OUT = High, I_{OUT} = 500mA, t_{CLP} = 10µs		0.57		V
$V_{CLP-CLAMP}$	V_{CLAMP} – V_{CC}	OUT = High, I_{CLAMP} = 500mA, t_{CLP} = 10µs		1.1		V
Vcc Undervoltage Lockout (CA-IS3211MCG)						
$UVLO_R$	Output Undervoltage Lockout (V_{CC} Rising)	I_F = 10mA	11.0	12.0	13.0	V

Parameter		Test Conditions	Min	Typ	Max	Unit
$UVLO_F$	Output Undervoltage Lockout (V_{CC} Falling)	I_F = 10mA	10.0	11.0	12.0	V
$UVLO_{HYS}$	UVLO Hysteresis			1.0		V
V_{CC} Undervoltage Lockout (CA-IS3211MBG)						
$UVLO_R$	Output Undervoltage Lockout (V_{CC} Rising)	I_F = 10mA	7.3	8.1	8.9	V
$UVLO_F$	Output Undervoltage Lockout (V_{CC} Falling)	I_F = 10mA	6.7	7.4	8.2	V
$UVLO_{HYS}$	UVLO Hysteresis			0.7		V

Note:

1. Current flowing into a device pin is positive, and current flowing out is negative;
2. Guaranteed by design and Bench testing.

6.10. Switching Characteristics

Unless otherwise specified, all typical values are at T_A = 25°C, V_{CC} = 15V, V_{EE} = GND. All minimum and maximum values are results under recommended operating conditions (T_A = –40 to 125°C, $I_{F(on)}$ = 7mA to 16mA, V_{EE} = GND, V_{CC} = 14V to 33V, $V_{F(off)}$ = –5V to 0.8V).

Parameter		Test Conditions	Min	Typ	Max	Unit
t_r	Output Rise Time	Cg = 1nF F_{SW} = 20kHz (50% duty cycle) V_{CC} = 15V See Figure 8-1		10	20	ns
t_f	Output Fall Time			10	20	ns
t_{PDLH}	Propagation Delay, Low-to-High			75	105	ns
t_{PDHL}	Propagation Delay, High-to-Low			75	105	ns
t_{PWD}	Pulse Width Distortion $\lvert t_{PDHL} - t_{PDLH} \rvert$				35	ns
$t_{sk(pp)}$	Part-to-Part Propagation Delay Skew	Cg = 1nF, V_{CC} = 15V, I_F = 10mA, F_{SW} = 20kHz (50% duty cycle)			25	ns
t_{UVLO_rec}	UVLO Recovery Time	V_{CC} rises from 0V to 15V, see Figure 9-4		9	20	µs
$CMTI_H$	CMTI (Output High)	I_F = 10mA, V_{CM} = 1500V, V_{CC} = 30V, T_A = 25°C, see Figure 8-3	150			kV/µs
$CMTI_L$	CMTI (Output Low Level)	V_F = 0V, V_{CM} = 1500V, V_{CC} = 30V, T_A = 25°C, see Figure 8-3	150			kV/µs

7. Typical Parameter Characteristics

Unless otherwise specified, T_A = 25°C, V_{CC} – V_{EE} = 15V, a 1µF capacitor is connected between V_{CC} and V_{EE}, C_{LOAD} = 1nF for timing parameter tests, C_{LOAD} = 180nF for I_{OH} and I_{OL} parameter tests, and all parameters are results under recommended operating conditions (T_A = –40°C to 125°C).

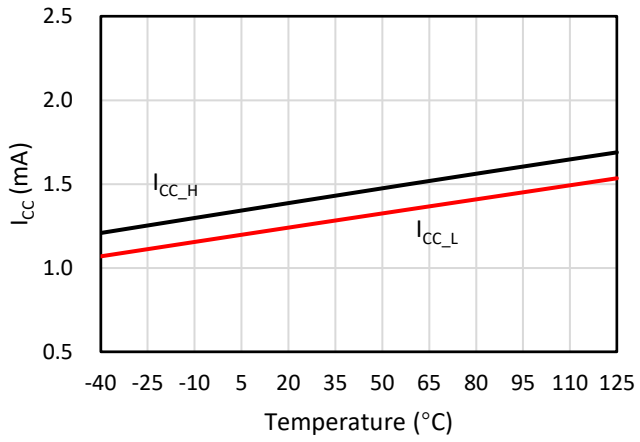


Figure 7-1 Output Power Supply Current vs. Temperature

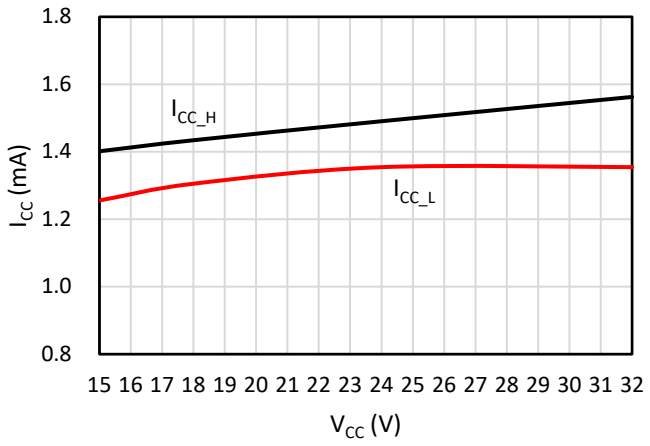


Figure 7-2 Output Power Supply Current vs. Supply Voltage

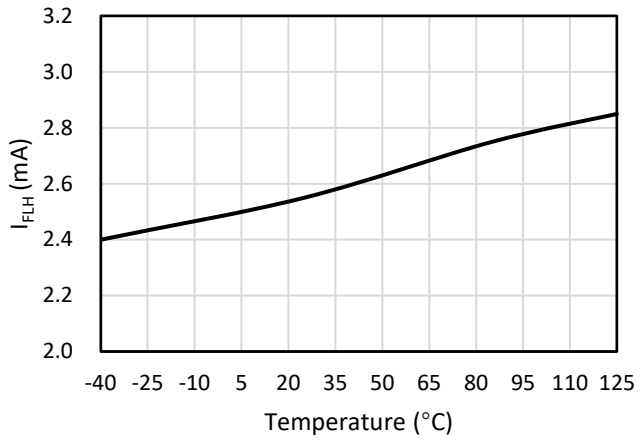


Figure 7-3 Input Forward Current Threshold vs. Temperature

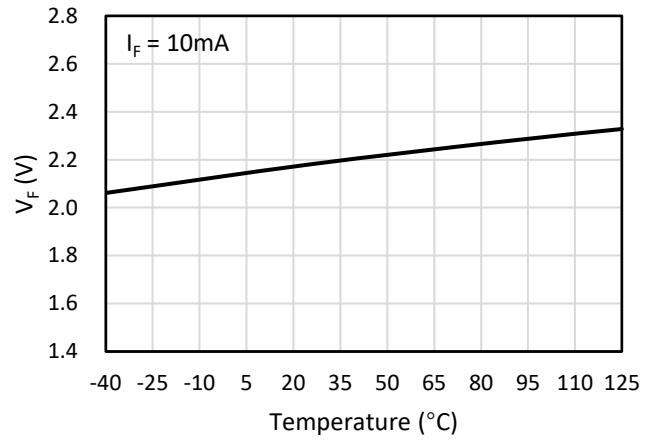


Figure 7-4 Input Forward Voltage vs. Temperature

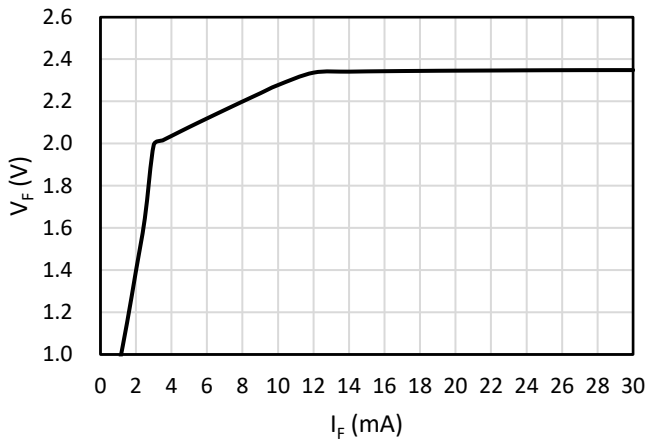


Figure 7-5 Input Forward Voltage vs. Input Forward Current

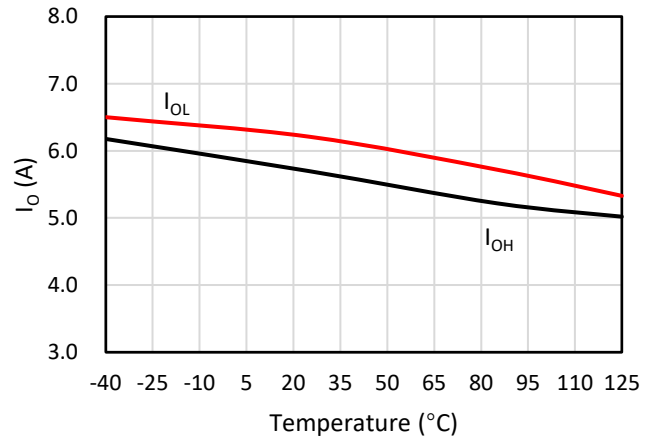


Figure 7-6 Drive Output Peak Current vs. Temperature

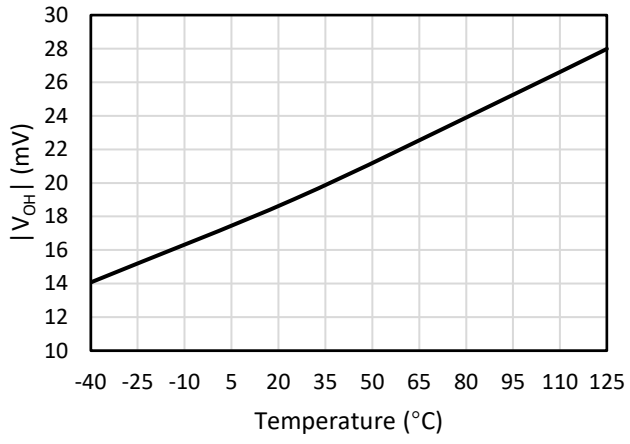


Figure 7-7 High-Level Output Voltage vs. Temperature

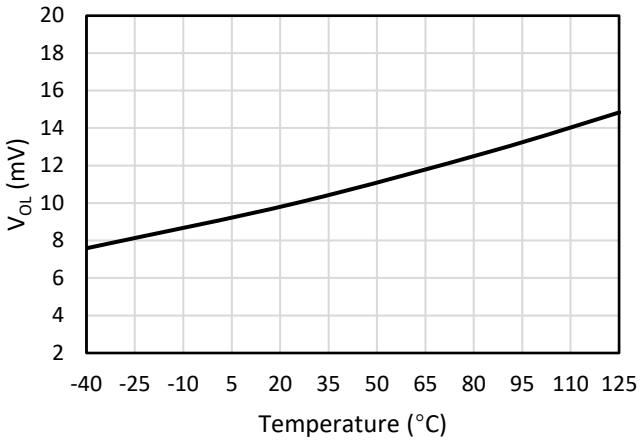


Figure 7-8 Low-Level Output Voltage vs. Temperature

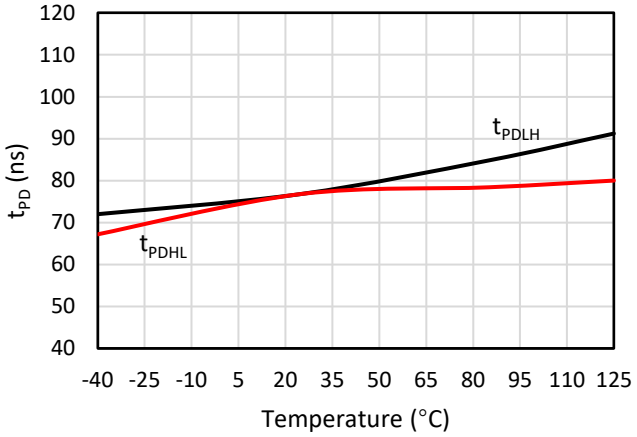


Figure 7-9 Propagation Delay vs. Temperature

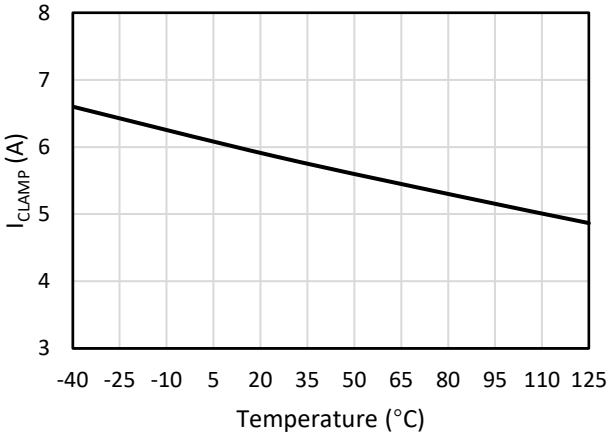


Figure 7-10 Miller Clamp Peak Current vs. Temperature

8. Parameter Measurement Information

8.1. Propagation Delay, Rise Time and Fall Time

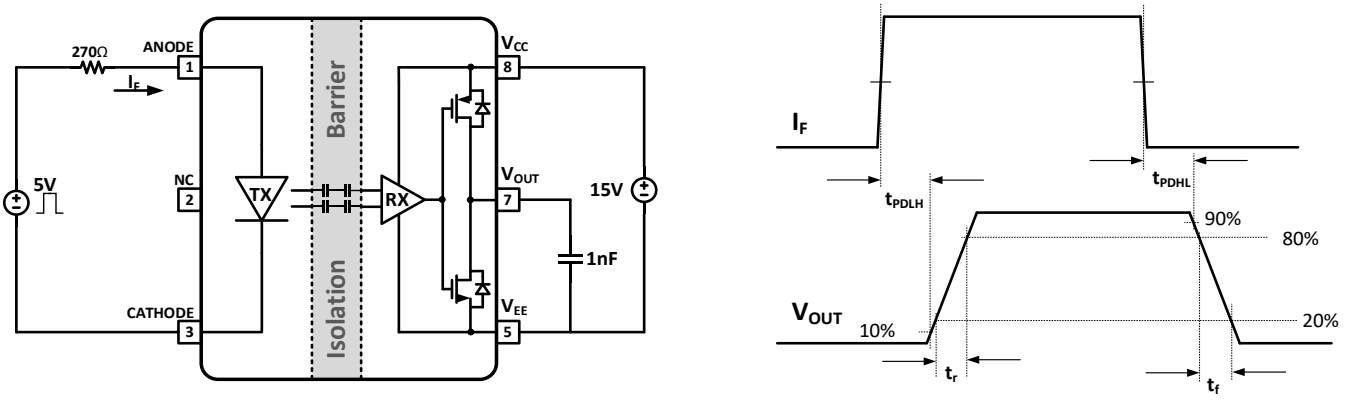


Figure 8-1 Propagation Delay from I_F to V_{OUT}, Rise Time and Fall Time of V_{OUT}

8.2. I_{OH} and I_{OL} Test

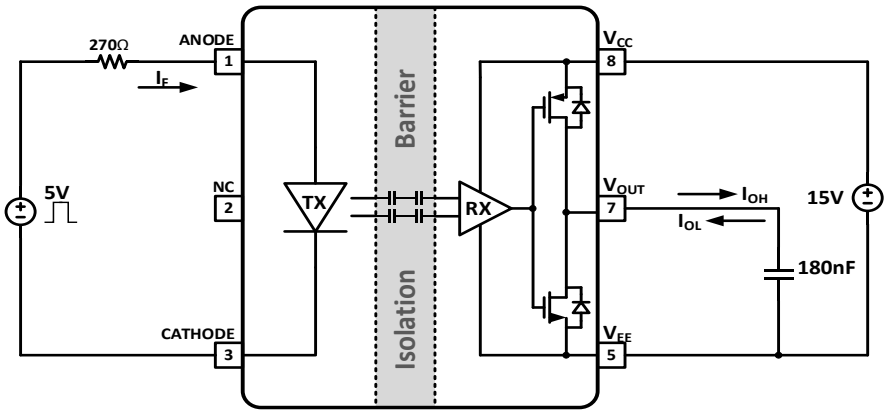


Figure 8-2 I_{OH} and I_{OL} Test Circuit

8.3. CMTI Test

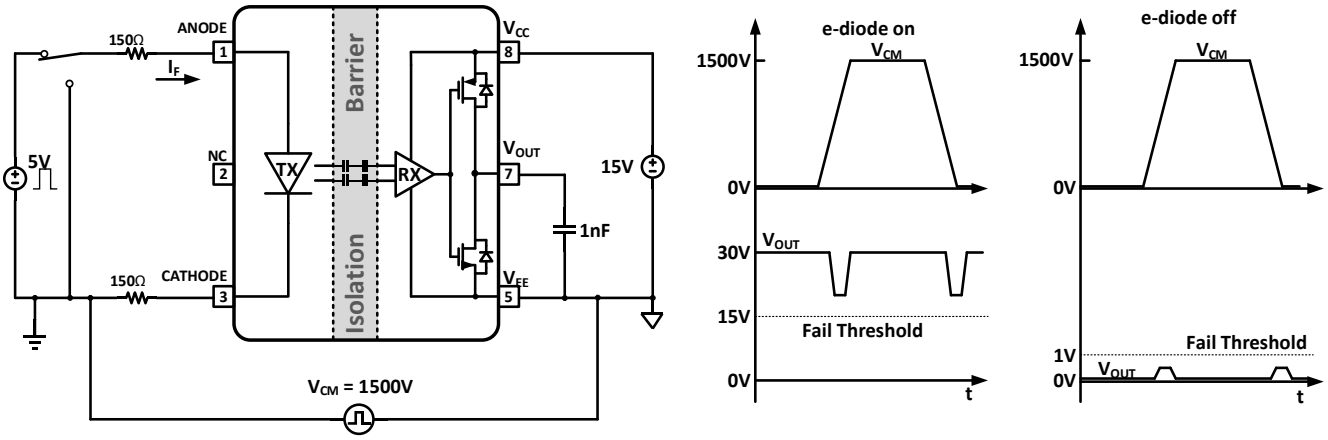


Figure 8-3 CMTI Test Circuit

9. Detailed Description

9.1. Overview

CA-IS3211M is a single-channel isolated gate driver with an opto-compatible input stage, capable of driving MOSFETs, IGBTs, and SiC devices. This device provides 5A source and 5A sink output peak current capability, and features an active Miller clamp with 5A peak current. The maximum output driver power supply voltage is 33V. The input and output employ fully differential dual-series high-voltage SiO_2 capacitive isolation technology. CA-IS3211M is offered in the industry-standard SOIC8-WB package, fully compatible with traditional optocoupler isolated gate drivers.

9.2. Functional Block Diagram

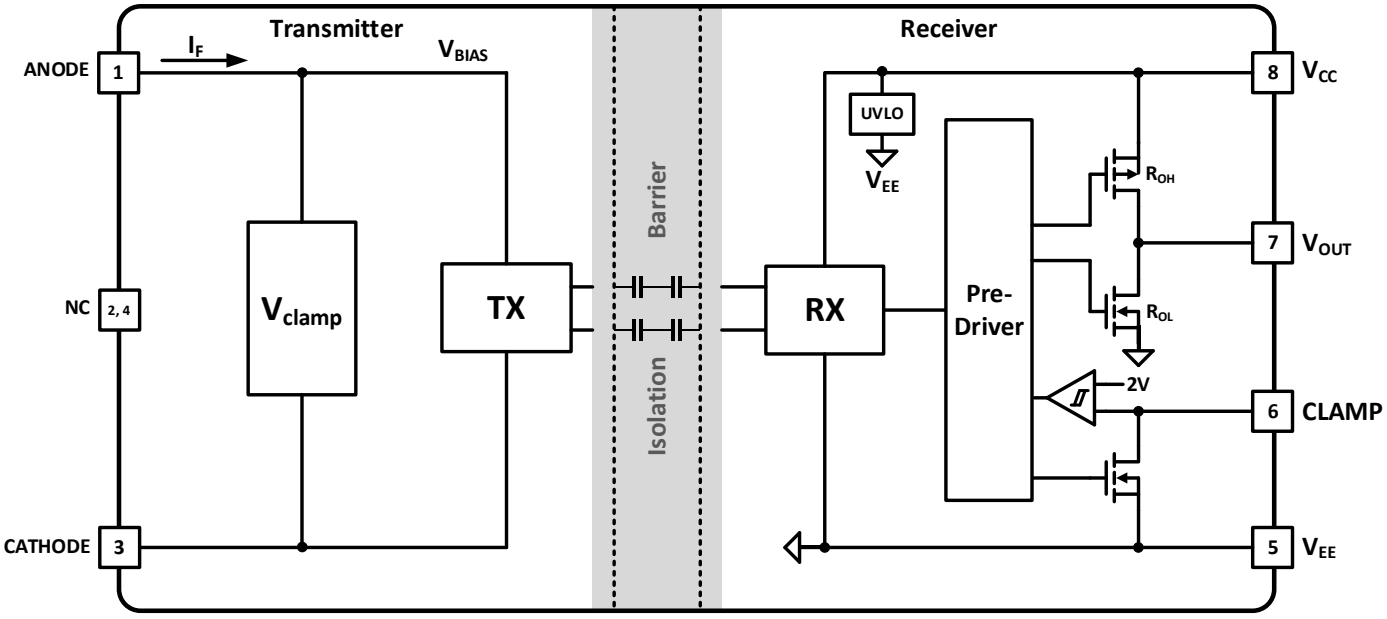


Figure 9-1 Functional Block Diagram

9.3. Power Supply

The output power supply V_{CC} supports a selectable voltage range from 10V to 33V (CA-IS3211MBG) or from 14V to 33V (CA-IS3211MCG). For unipolar power supply applications, V_{CC} is connected to the positive terminal of the power supply, and V_{EE} is connected to the GND of the driver-side power supply. For bipolar power supply applications, V_{CC} is connected to the positive power supply, and V_{EE} is connected to the negative power supply. In IGBT applications, the typical values of V_{CC} and V_{EE} relative to the GND of the driver-side power supply are 15V and –8V, respectively, and in SiC MOSFET applications, they are 18V and –5V, respectively. Power transistors typically require a negative voltage applied to the gate relative to the emitter or source to turn off, thereby preventing false turn-on caused by current injected by the Miller effect.

9.4. Input Stage

The input stage of CA-IS3211M can be simply equivalent to a diode emulator. When a positive voltage is applied to the input diode, the diode is forward-biased, and the forward current I_F flows into the diode emulator. The forward voltage drop of the diode emulator is 2.1V (Typ). An external resistor is required in the application to limit the input forward current. The recommended forward current range is from 7mA to 16mA. When I_F exceeds the input forward current threshold I_{FLH} (Typ 2.55mA), a high-frequency signal is transmitted across the isolation barrier through the high-voltage SiO_2 capacitor. The receiver detects and demodulates this high-frequency signal, driving V_{OUT} to output a high level. If the positive voltage drops below V_{F_HL} or is reverse-biased, the gate driver output goes low.

CA-IS3211M also supports interlock configuration operation (see Figure 10-3). System designers can use appropriate input resistors to flexibly select the 3.3V and 5.0V power supplies to drive the input stage of the device.

9.5. Output Stage

The output stage of the CA-IS3211M series adopts a push-pull structure as shown in Figure 9-2: the output pull-up network uses a single P-channel MOSFET structure, and the pull-down network of CA-IS3211M uses an N-channel MOSFET. Since the MOS output stage can provide a very small voltage drop, the output voltage can achieve rail-to-rail operation between V_{CC} and V_{EE}.

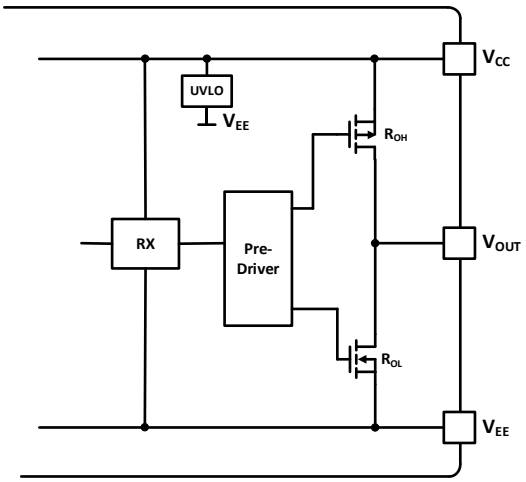


Figure 9-2 Output Stage Structure

9.6. Active Miller Clamp

For gate driver applications with a unipolar bias supply, or a bipolar supply with a small negative turn-off voltage, the active Miller clamp can help add an additional low-impedance path to shunt the Miller current and prevent unintended power transistor turn-on caused by high dv/dt through the Miller capacitance. Figure 9-3 shows the timing diagram of the internal Miller clamp function.

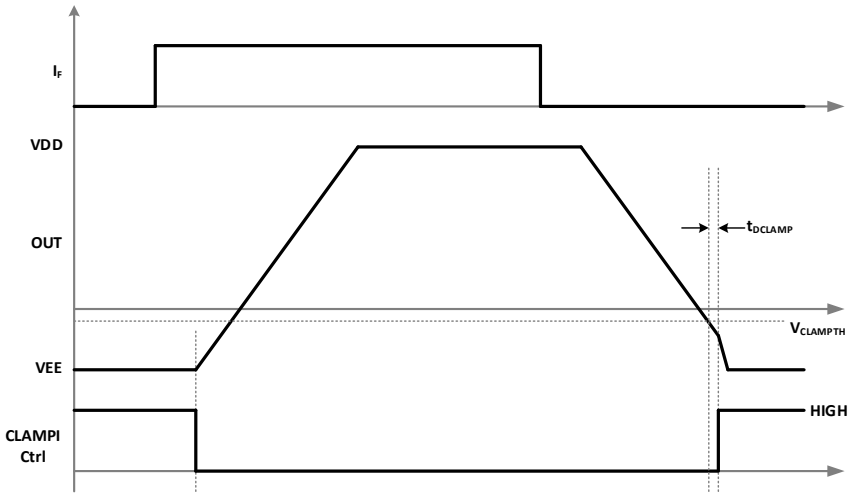


Figure 9-3 Timing Diagram of the Built-in Active Miller Clamp Function

9.7. Undervoltage Lockout (UVLO)

The UVLO function of the device is used to prevent undervoltage driving of IGBTs and MOSFETs. When the V_{CC} voltage is below $UVLO_R$ at startup of the device, or falls below $UVLO_F$ after startup, the VOUT output remains low regardless of the magnitude of the input forward current I_F. The UVLO protection on V_{CC} also features hysteresis ($UVLO_{HYS}$). The hysteresis function is designed to prevent erroneous output caused by power supply voltage fluctuation or noise. The timing diagram of undervoltage lockout is shown in Figure 9-4.

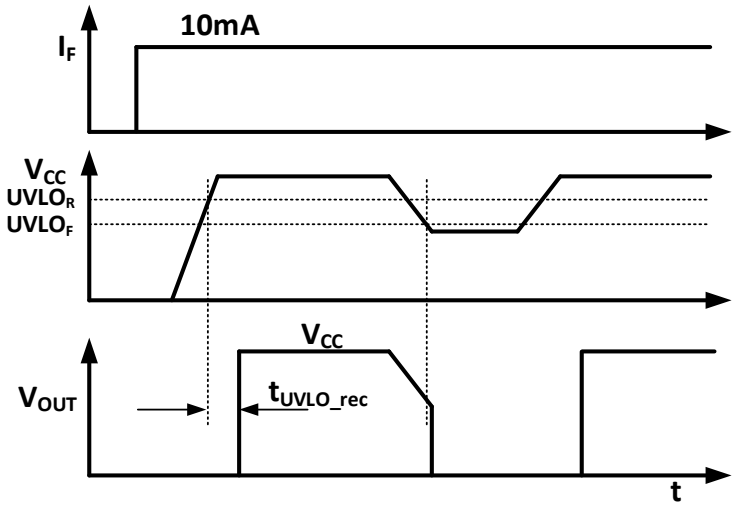


Figure 9-4 UVLO Functional Timing Diagram

9.8. Active Pull-Down

The active pull-down function can pull the gate of the IGBT or MOSFET to a low level after the power supply V_{CC} is disconnected. When the output stage of the driver is in an unbiased state (V_{CC} floating), the output is clamped to a low level by the active clamp circuit. In this case, the pull-up PMOS is turned off, and the gate of the pull-down NMOS is connected to the driver output through a 500kΩ resistor, so the pull-down NMOS can effectively clamp the output voltage V_{OUT} below 2V.

9.9. Short-Circuit Clamp

The short-circuit clamp function is implemented by adding a diode between the V_{OUT} or CLAMP pin and the V_{CC} pin, which pulls the output pin V_{OUT} or pin CLAMP slightly above V_{CC} under short-circuit conditions, thereby clamping the driver's output voltage. The short-circuit protection function is used to prevent overvoltage breakdown or performance degradation of the IGBT's base or MOSFET's gate. The internal diode can withstand a 10μs pulse current of 500mA and a continuous current of 20mA. An external Schottky diode can also be used to enhance current conduction capability as required.

9.10. Truth Table

Table 9-1 lists the functional modes of CA-IS3211M.

Table 9-1 Truth Table of CA-IS3211M[1]

Input Side	Vcc	Vout
Shutdown ($I_F < I_{FLH}$)	$UVLO_R$ ~ 33V	Low
On ($I_F > I_{FLH}$)	$UVLO_R$ ~ 33V	High
X	0V ~ $UVLO_R$, $UVLO_F$ ~ 0V	Low

Note:
1. "X" indicates don't care.

10. Applications Guide

10.1. Applications

Figure 10-1 and Figure 10-2 show the typical applications for driving IGBTs. To achieve better driving performance, the selection of bypass capacitors is critical. Designers are recommended to use 0.1μF/50V ceramic capacitors to reduce high-frequency noise, and 10μF/50V ceramic capacitors to provide higher peak current capability. Additionally, the filter capacitors should be placed as close as possible to the V_{CC} and V_{EE} pins of the device.

During normal operation of the CA-IS3211M, the recommended input forward current design range is from 7mA to 16mA. The MCU cannot drive it directly, so additional circuits or components are required. The following two connection methods are recommended. As shown in Figure 10-1, an NMOS in series with an external resistor is used, and the MCU drives the NMOS switch. As shown in Figure 10-2, a buffer is connected to the device to enhance the MCU's driving capability.

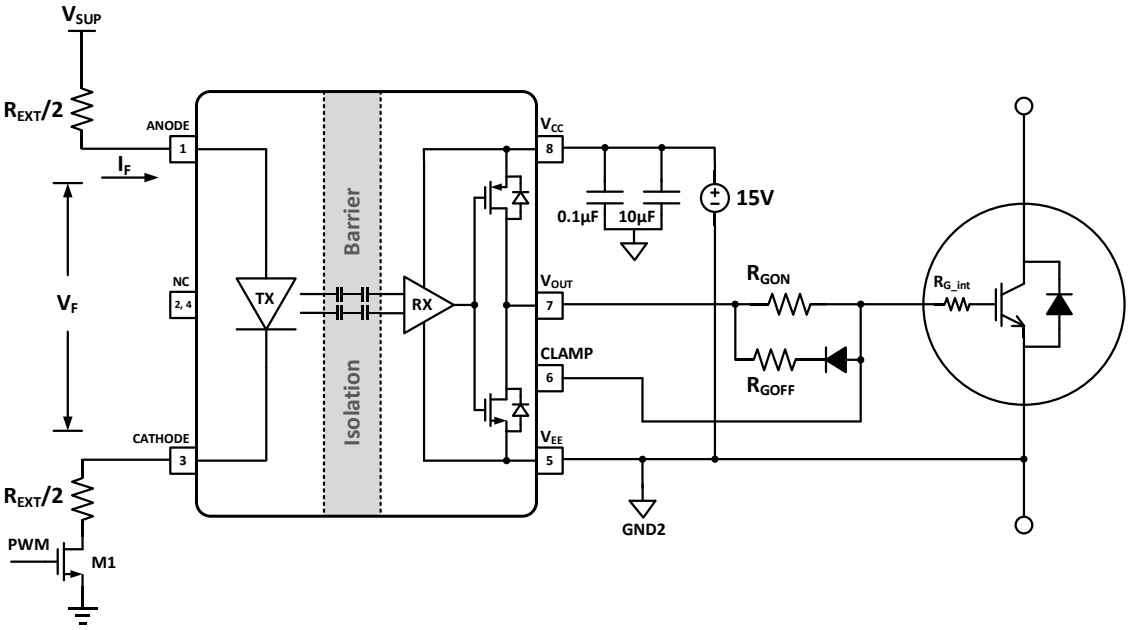


Figure 10-1 Typical Application of NMOS + Resistor at the Input Stage

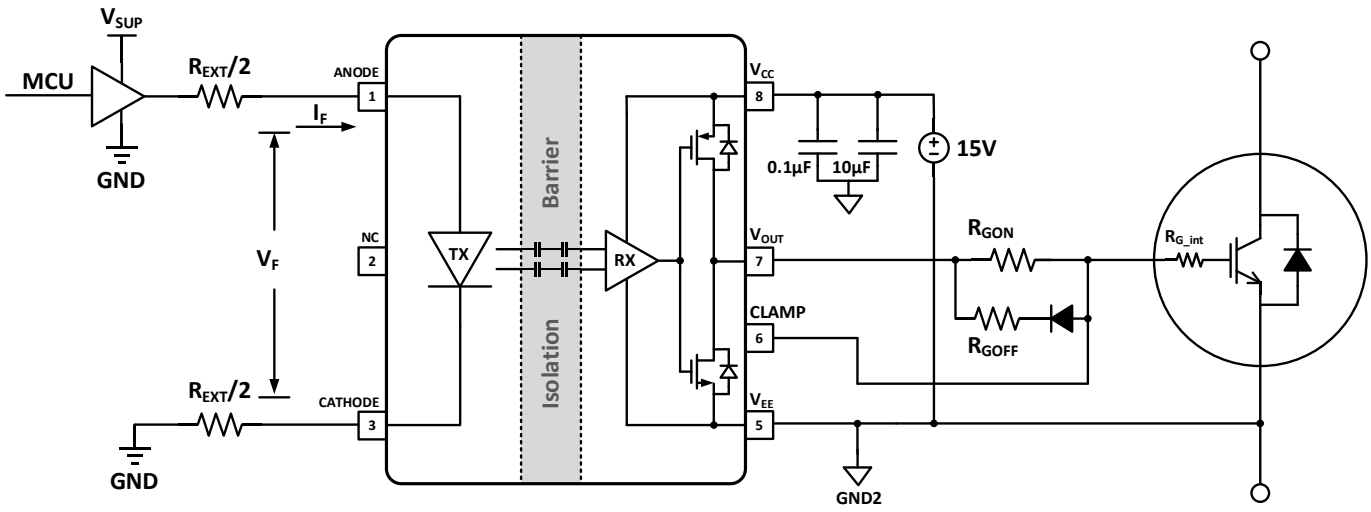


Figure 10-2 Typical Application of Buffer + Resistor at the Input Stage

10.2. Interlock Configuration

In typical system applications, the gate driver is often used to drive a power stage, as shown in Figure 10-3, where two gate drivers are used to drive the high-side and low-side IGBTs, respectively. During normal system operation, the MCU generates a pair of complementary PWM pulse control signals to control the high-side and low-side power switches. When a system fault occurs, MCU failure or software errors may cause the MCU output signals to be simultaneously high, leading to simultaneous conduction of the high-side and low-side power switches, which can damage the device. To avoid this phenomenon, the interlock configuration shown in Figure 10-3 can be adopted, where the anode of the high-side driver diode is connected to the cathode of the low-side driver diode, and the cathode of the high-side driver diode is connected to the anode of the low-side driver diode. If the MCU control signals are erroneously held high (or low) simultaneously, the interlock configuration of the two diode emulators enters the cutoff state at the same time, thereby preventing the high-side and low-side power switches from conducting simultaneously.

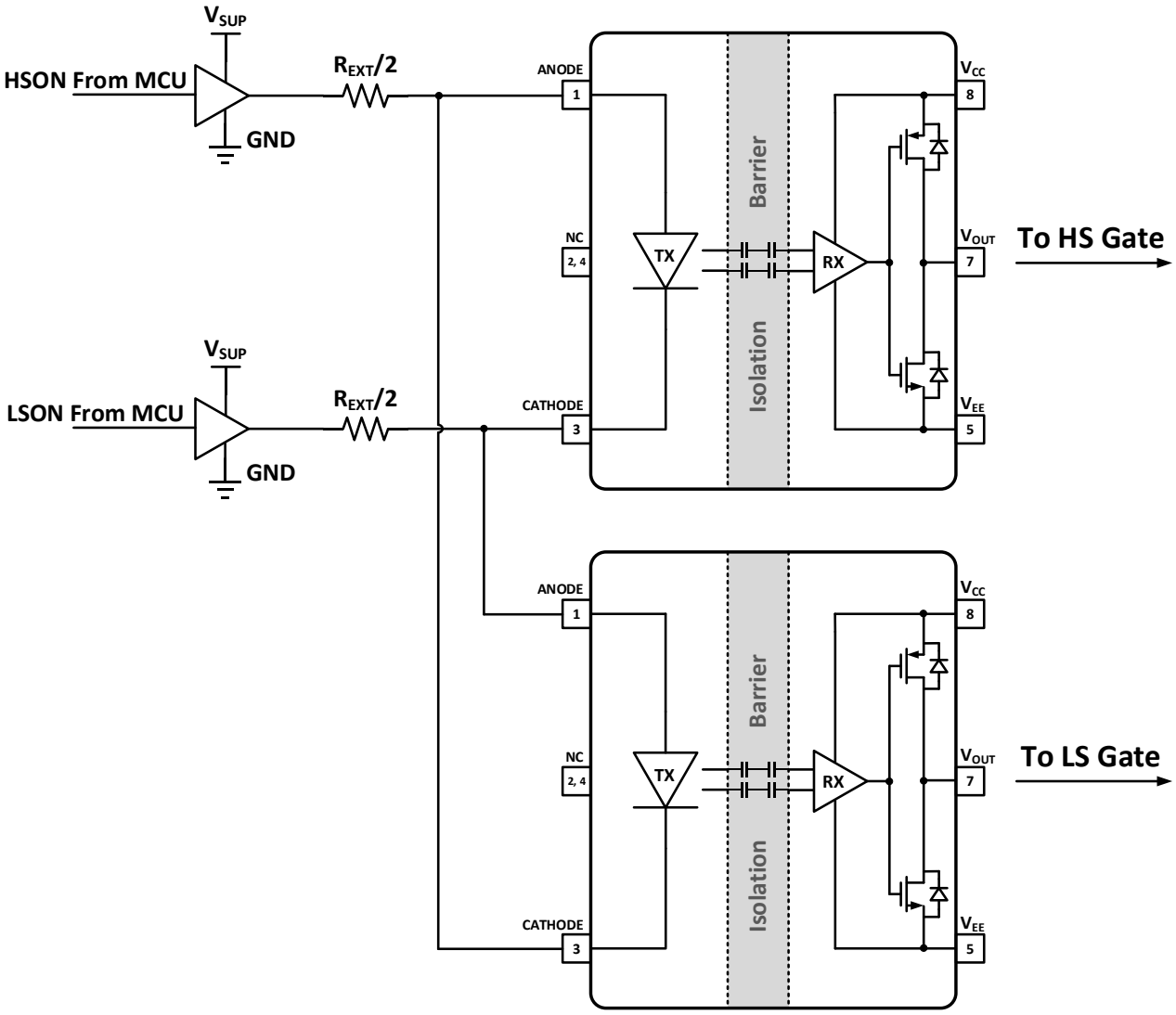


Figure 10-3 Half-Bridge Interlock Configuration

10.3. Input Resistor Design

The input resistor can limit the forward current flowing into the diode emulator. The input forward threshold current I_{FLH} is 2.55mA (Typ), and the recommended forward current operating range is 7mA to 16mA. Taking the typical application in Figure 10-2 as an example, the external input resistor calculation formula is as follows:

$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{OH\_buf}$$

Where,

- Input forward current I_F is 10mA (Typ) (Min = 7mA, Max = 16mA);
- Supply voltage V_{SUP} is 5V (Min = 4.75V, Max = 5.25V);
- Diode emulator's input forward voltage drop V_F is 2.1V (Typ) (Min = 1.8V, Max = 2.4V);
- Buffer's output impedance R_{OH_buf} is 18Ω (Min = 13Ω, Max = 22Ω).

From the above parameters, the external resistor R_{EXT} range can be calculated: Min = 204Ω, Typ = 272Ω, Max = 310Ω.

10.4. Output Driver Resistance Design

The external gate drive resistor is particularly critical for the design of power transistor. When the power transistor switches, parasitic inductance, parasitic capacitance, high dv/dt and di/dt, as well as the diode reverse recovery time, can all lead to undesirable behavior or EMI issues of the power transistor. The gate drive resistor mainly affects the following three aspects: drive current, switching losses, and rise and fall times. Therefore, when actually selecting the drive resistor, the designer needs to balance the comprehensive performance parameters of the solution.

The formula for estimating the peak source current I_{OH} is:

$$I_{OH} = \min\left[5A, \frac{V_{CC} - V_{EE}}{\left(R_{OH} + R_{GON} + R_{GFET_{int}}\right)}\right]$$

In the formula,

- R_{GON} is the external gate turn-on resistance;
- $R_{GFETint}$ is the internal gate resistance of the power transistor (refer to the power transistor's datasheet);
- R_{OH} is approximately 0.95Ω.

The formula for estimating the peak sink current I_{OL} is:

$$I_{OL} = \min\left[5A, \frac{V_{CC} - V_{EE}}{\left(R_{OL} + R_{GOFF} + R_{GFET_{int}}\right)}\right]$$

In the formula,

- R_{GOFF} is the external gate turn-off resistor;
- $R_{GFETint}$ is the internal gate resistance of the power transistor (refer to the power transistor's datasheet);
- R_{OL} is approximately 0.5Ω.

10.5. PCB Layout Guidelines

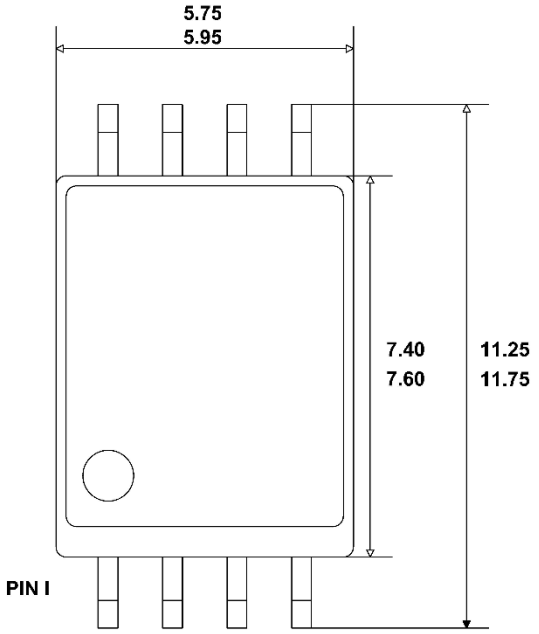
To achieve optimal performance of CA-IS3211M, the following principles should be followed during PCB layout:

- To ensure power supply stability and low noise, the bypass capacitor from V_{CC} to V_{EE} should be placed as close as possible to the V_{CC} and V_{EE} pins of the device, and the use of MLCC capacitors with low ESR and low ESL is recommended.
- When the device drives the power transistor, V_{OUT} exhibits very high di/dt, and the parasitic inductance of the V_{OUT} loop PCB trace can cause EMI and voltage oscillation issues. Therefore, when designing the PCB, the device should be placed as close as possible to the power transistor, the V_{OUT} trace should be as wide as possible, and the loop trace should be as short as possible to reduce the loop parasitic inductance.

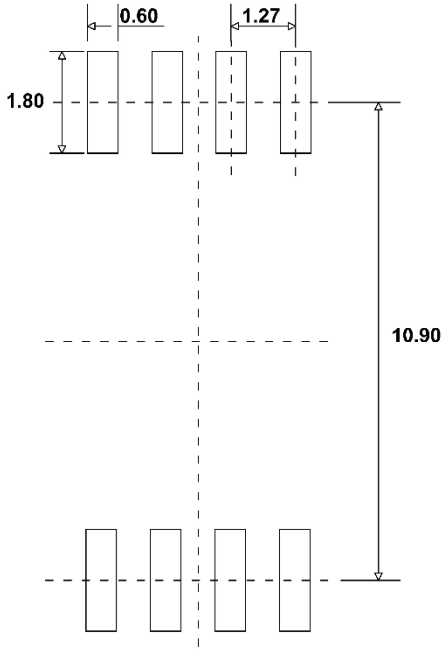
- To ensure the isolation performance between the primary side and the secondary side, please avoid placing any PCB traces, copper pours, pads, and vias underneath the device. A PCB slotting technique can also be adopted to prevent affecting the isolation performance.
- When the load is heavy or the switching frequency is high, the device losses will also increase. The heat can be conducted to the PCB board through proper PCB layout to reduce the device temperature. It is recommended to appropriately increase the PCB copper pour on the V_{CC} and V_{EE} pins, and prioritize maximizing the V_{EE} connection.
- If the system has a multi-layer board design, it is recommended to place a large number of vias in the V_{CC} and V_{EE} layers to reduce parasitic parameters.

11. Package Information

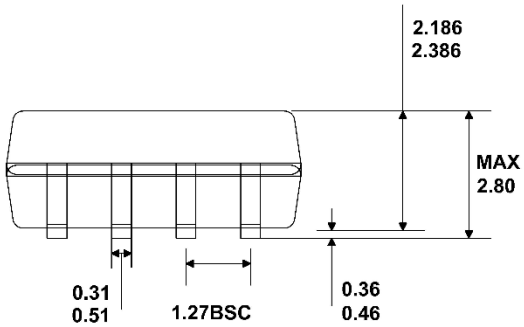
The following figure shows the dimension drawing and recommended land pattern for the SOIC8-WB package. All dimensions are in millimeters unless otherwise specified for angles.



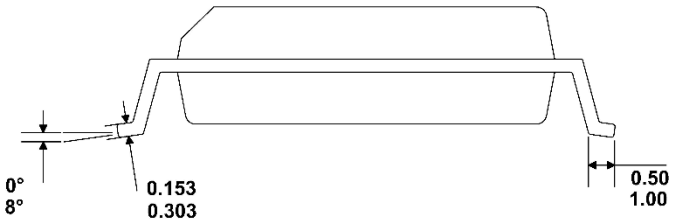
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

12. Soldering Information

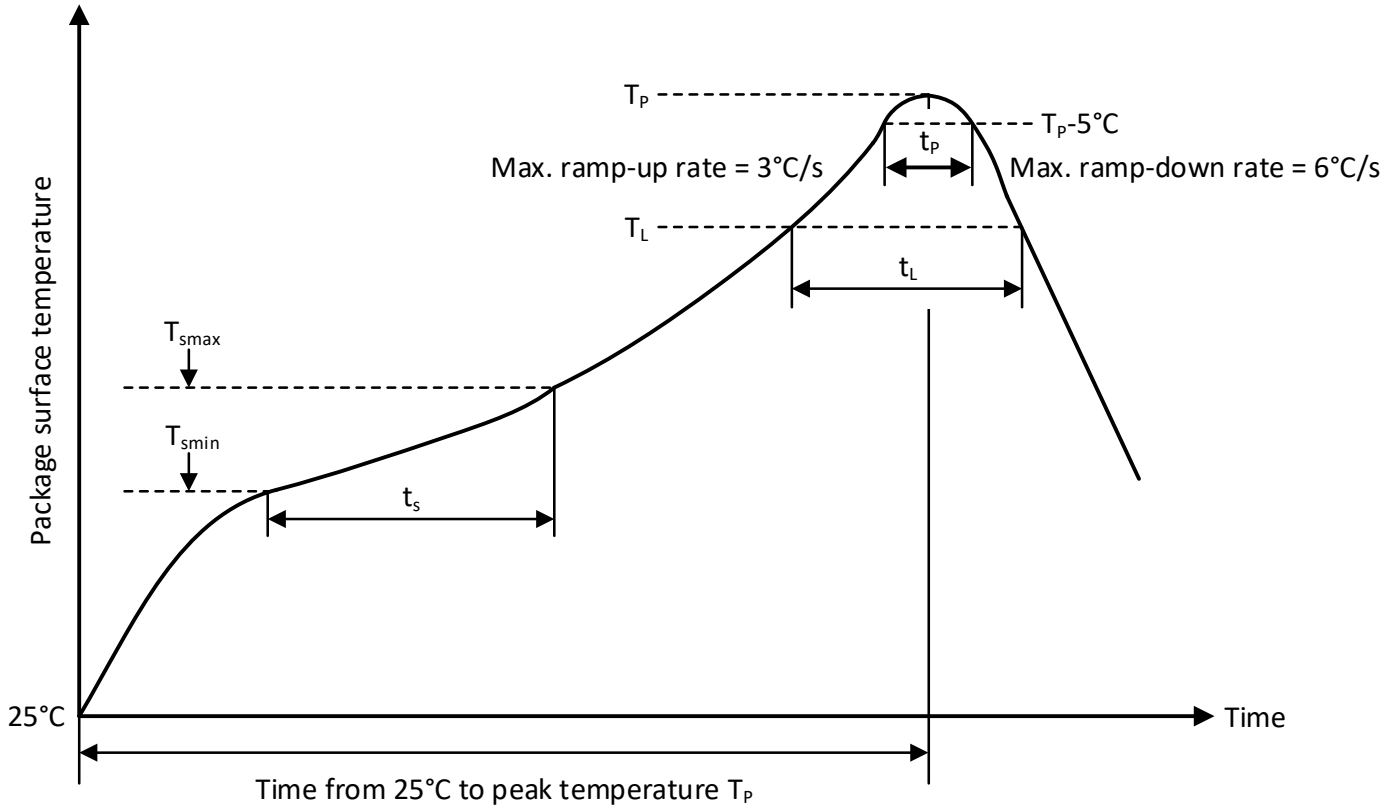


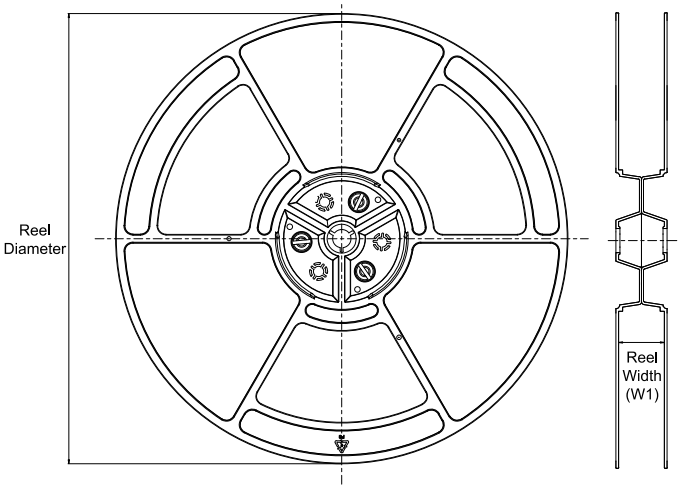
Figure 12-1 Soldering Temperature Profile (Reflow)

Table 12-1 Soldering Temperature Parameters

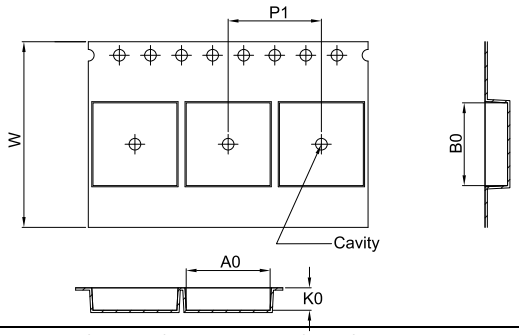
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

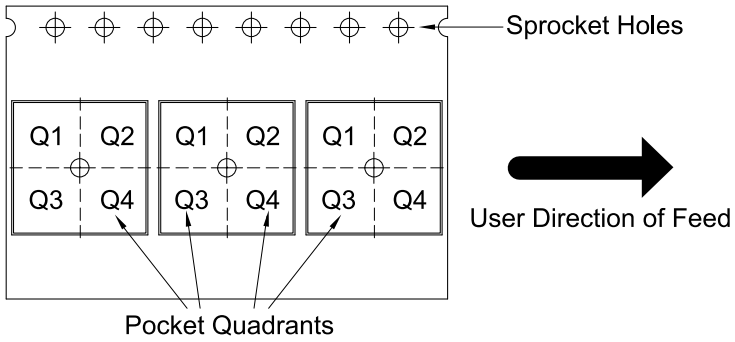


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3211MCG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3211MBG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1

14. Revision History

Revision	Description	Revised Date	Page Changed
Version 1.00	NA	2026/04/30	NA

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