4.7A Source /6A Sink, 5.7kV$_{RMS}$ Opto-Compatible Single-Channel Isolated Gate Driver

1. Features

- **4.7A Peak Source Current and 6A Peak Sink Current**
- **Up to 30V Output Drive Supply Range with 8V and 12V UVLO options**
- **Support Rail to Rail Output**
- **Up to 7V Reverse Voltage on Input-stage, Interlock**
- **Matching Propagation Delay**
  - 80ns Propagation delay (typical)
  - 25ns Part to part propagation delay matching (maximum)
  - 35ns Pulse width distortion (maximum)
- **-40°C to +150°C Operating Junction Temperature Range**
- **Robust Galvanic Isolation**
  - High lifetime: >40 years
  - Up to 5.7kV$_{RMS}$ isolation rating for the wide-body packages and 3.75kV$_{RMS}$ isolation rating for DUB8 package
  - Common-mode transient immunity (CMTI) > ±150kV/µs
- **Package options**
  - 6-pin wide-body SOIC6-WB (J) package
  - 6-pin wide-body TSOIC6-WB (TJ) thin package
  - 8-pin wide-body SOIC8-WB (G) package
  - 8-pin DUB8 (U) package
- **Safety regulatory approvals**
  - VDE Reinforced Isolation and Basic Isolation per DIN EN IEC 60747-17(VDE 0884-17):2021-10
  - UL Certification per UL 1577
  - CQC Certification per GB4943.1-2022
  - TUV Certification per EN 62368-1 EN 61010-1

2. Applications

- Isolated DC-DC and AC-DC Converters
- Motor Control
- Uninterruptible Power Supply (UPS)
- Isolated Gate Driver for Inverters

3. General Description

The CA-IS3211C devices are a family of single-channel, opto-compatible isolated gate driver capable of sourcing 4.7A and sinking 6A currents. These devices operate with dual supplies or a single supply of 10V to 30V (8V UVLO version) or 14V to 30V (12V UVLO version) wide voltage range of V_{CC} - V_{EE}, making them ideal to drive power MOSFET, IGBT or silicon-carbide (SiC) transistors in various inverter, motor control or isolated power supply systems. The CA-IS3211C can be configured as low-side and high-side drivers. The CA-IS3211CVx offers single terminal gate drive output: V_{OUT} and the CA-IS3211CSx offers dual separate output terminals: OUTH and OUTL. The driver output is pulled to low state to turn-off external power transistors when V_{CC} supply input is either not powered, open-circuit or in UVLO.

The CA-IS3211C devices have integrated digital galvanic isolation using Chipanalog's proprietary capacitive isolation technology and feature isolation with a withstand voltage rating of up to 5.7kV$_{RMS}$/3.75kV$_{RMS}$ for 60 seconds and minimum common-mode transient immunity (CMTI) of 150kV/µs. These devices can be used as drop-in replacement for the industry standard optocoupler-based gate drivers while providing high CMTI, low propagation delay, small pulse width distortion and small part-to-part skew. The input stage is an analog diode which means long term reliability and excellent aging characteristics.

The CA-IS3211C devices are available either in a 6-pin or 8-pin wide-body SOIC packages, and 8-pin DUB package. All devices are rated for operation at junction temperatures of -40°C to +150°C.

Device Information

Part Number	Package	Package Size (NOM)
CA-IS3211CVBJ	SOIC6-WB (J)	4.68mm x 7.50mm x 3.18mm
CA-IS3211CVCJ	SOIC6-WB (J)	4.68mm x 7.50mm x 3.18mm
CA-IS3211CVBTJ	TSOIC6-WB (TJ)	4.68mm x 7.50mm x 2.30mm
CA-IS3211CVCTJ	TSOIC6-WB (TJ)	4.68mm x 7.50mm x 2.30mm
CA-IS3211CVBG	SOIC8-WB (G)	5.85mm x 7.50mm
CA-IS3211CVCG	SOIC8-WB (G)	5.85mm x 7.50mm
CA-IS3211CSBG	SOIC8-WB (G)	5.85mm x 7.50mm
CA-IS3211CSCG	SOIC8-WB (G)	5.85mm x 7.50mm
CA-IS3211CVBU	DUB8 (U)	9.20mm x 6.62mm
CA-IS3211CVCU	DUB8 (U)	9.20mm x 6.62mm

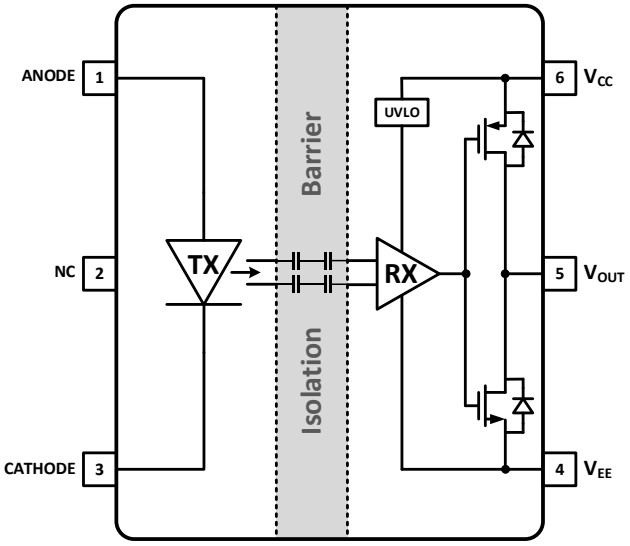

Figure 3-1 Simplified Schematic

4. Ordering Information

Table 4-1 Ordering Information

Part Number	Output Type	UVLO (V)	Isolation Rating (V_{PK})	Package
CA-IS3211CVBJ	Single Vout Pin	8	8000	SOIC6-WB (J)
CA-IS3211CVCJ	Single Vout Pin	12	8000	SOIC6-WB (J)
CA-IS3211CVBTJ	Single Vout Pin	8	8000	TSOIC6-WB (TJ)
CA-IS3211CVCTJ	Single Vout Pin	12	8000	TSOIC6-WB (TJ)
CA-IS3211CVBG	Single Vout Pin	8	8000	SOIC8-WB (G)
CA-IS3211CVCG	Single Vout Pin	12	8000	SOIC8-WB (G)
CA-IS3211CSBG	Split Output	8	8000	SOIC8-WB (G)
CA-IS3211CSCG	Split Output	12	8000	SOIC8-WB (G)
CA-IS3211CVBU	Single Vout Pin	8	5300	DUB8 (U)
CA-IS3211CVCU	Single Vout Pin	12	5300	DUB8 (U)

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5. Pin Configuration and Description

5.1. CA-IS3211CVxJ and CA-IS3211CVxTJ Pin Configuration and Description

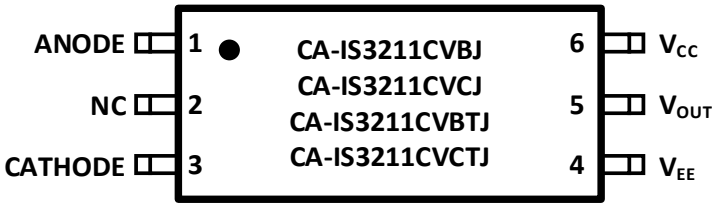


Figure 5-1 The CA-IS3211 CVBJ/CVCJ/CVBTJ/CVCTJ Pin Configuration

Table 5-1 The CA-IS3211CVBJ/CVCJ/CVBTJ/CVCTJ Pin Description

Pin Name	Pin Number	Type	Description
ANODE	1	Input	Driver input, the anode of input diode.
NC	2	---	No internal connection.
CATHODE	3	Input	Driver input, the cathode of input diode.
V_{EE}	4	Power Supply	Negative Power supply input for output-side, it's the negative output supply rail. For bipolar operation, bypass V_{EE} to output-side ground with 0.1μF||10μF capacitors as close as possible to the device. For single supply operation, connect V_{EE} to GND on the output-side.
V_{OUT}	5	Output	Gate driver output.
V_{CC}	6	Power Supply	Positive Power supply input for output-side, it's the positive output supply rail. Bypass V_{CC} to output-side ground with 0.1μF||10μF capacitors as close as possible to the device.

5.2. CA-IS3211CVxG andA-IS3211CVxU Pin Configuration and Description

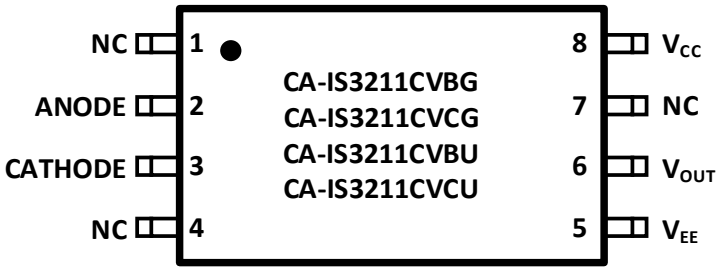


Figure 5-2 The CA-IS3211CVBG/CVCG/CVBU/CVCU Pin Configuration

Table 5-2 The CA-IS3211CVBG/CVCG/CVBU/CVCU Pin Description

Pin Name	Pin Number	Type	Description
NC	1	---	No internal connection.
ANODE	2	Input	Driver input, the anode of input diode.
CATHODE	3	Input	Driver input, the cathode of input diode.
NC	4	---	No internal connection.
V_{EE}	5	Power Supply	Negative Power supply input for output-side, it's the negative output supply rail. For bipolar operation, bypass V_{EE} to output-side ground with 0.1μF||10μF capacitors as close as possible to the device. For single supply operation, connect V_{EE} to GND on the output-side.
V_{OUT}	6	Output	Gate driver output.
NC	7	---	No internal connection.
V_{CC}	8	Power Supply	Positive Power supply input for output-side, it's the positive output supply rail. Bypass V_{CC} to output-side ground with 0.1μF||10μF capacitors as close as possible to the device.

5.3. CA-IS3211CSxG Pin Configuration and Description

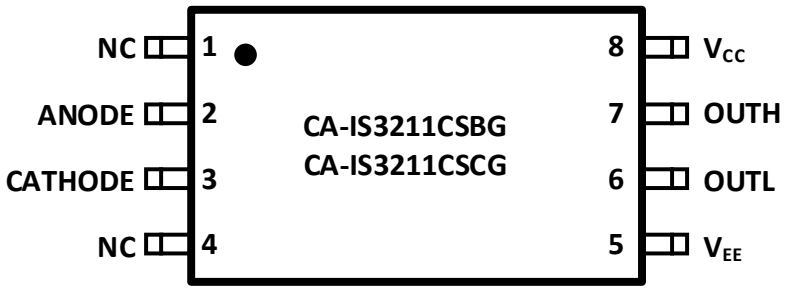


Figure 5-3 The CA-IS3211CSBG/CSCG Pin Configuration

Table 5-3 The CA-IS3211CSBG/CSCG Pin Description

Pin Name	Pin Number	Type	Description
NC	1	---	No internal connection.
ANODE	2	Input	Driver input, the anode of input diode.
CATHODE	3	Input	Driver input, the cathode of input diode
NC	4	---	No internal connection.
V_{EE}	5	Power Supply	Negative Power supply input for output-side, it's the negative output supply rail. For bipolar operation, bypass V_{EE} to output-side ground with 0.1μF||10μF capacitors as close as possible to the device. For single supply operation, connect V_{EE} to GND on the output-side.
OUTL	6	Output	Gate driver pull-down output.
OUTH	7	Output	Gate driver pull-up output.
V_{CC}	8	Power Supply	Positive Power supply input for output-side, it's the positive output supply rail. Bypass V_{CC} to output-side ground with 0.1μF||10μF capacitors as close as possible to the device.

6. Specifications

6.1. Absolute Maximum Ratings[1]

over operating free-air temperature range unless otherwise specified. [1]

Parameters		Minimum	Maximum	Unit
$I_{F(AVG)}$	Average input current	-	25	mA
$I_{F(TRAN)}$ < 1us pulse, 300pps	Peak transient input current		1	A
$V_{R(MAX)}$	Reverse input voltage		7.0	V
V_{CC} - V_{EE}	Output-side supply voltage range	-0.3	32	V
V_{OUT}	Driver output voltage	V_{EE} - 0.3	V_{CC} + 0.3	V
T_J [2]	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. To maintain the recommended operating junction temperature conditions, see Thermal Information.

6.2. ESD Ratings

			Value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001.	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101.	±2000	

6.3. Recommended Operating Conditions

Over operating free-air temperature range unless otherwise specified.

Parameters			Minimum	Typical	Maximum	Unit
V_{CC}	Driver output voltage (V_{CC} - V_{EE})	12V UVLO version	14		30	V
		8V UVLO version	10		30	
$I_{F(ON)}$	Input diode turn-on: diode forward current		7		16	mA
$V_{F(OFF)}$	Input diode turn-off: anode voltage - cathode voltage		-5.5		0.9	V
T_J	Junction temperature		-40		150	°C
T_A	Ambient temperature		-40		125	°C

6.4. Thermal Information

Thermal Metric		SOIC8-WB (G)	SOIC6-WB/TSOIC6-WB (J/TJ)	DUB8 (U)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	126	73.3	°C/W
$R_{\theta JC(top)}$	Junction to Case (top)	51.7	66.1	63.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.4	62.8	43.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.0	29.6	27.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.5	60.8	42.7	°C/W

6.5. Power Ratings

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
P_D	Maximum input and output power dissipation (derate 6mW/°C above +25°C)	V_{CC}= 20V, I_F = 10mA, 10kHz square wave with 50% duty cycle, C_L = 180nF, T_A = 25°C			750	mW
P_{D1}	Maximum input power dissipation[1]				10	mW
P_{D2}	Maximum output power dissipation				740	mW

Note:

1. The maximum P_{D1} = 40mW and the absolute maximum rating of P_{D1} is 55mW.

6.6. Insulation Specifications

Parameters		Test Conditions	Specifications		Unit
			J/TJ/G	U	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	>8.5	>6.1	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	>8.5	>6.8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>28	>28	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	According to IEC 60664-1	I		
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	1414	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1500	1000	V_{RMS}
		DC voltage	2121	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% production test)	8000	5300	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	8000	6250	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification) 1.2/50-µs waveform per IEC 62368-1	12800	8125	V_{PK}
q_{pd}	Apparent charge[4]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5		pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5		
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s; (Reinforced) $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s; (Basic)	≤5		
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	0.5		pF
R_{IO}	Isolation resistance, input to output[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$		
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$		
	Pollution degree		2		
	Climatic category		40/125/21		
UL 1577					
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5700	3750	V_{RMS}

Notes:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

6.7. Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2022	Certified according to EN IEC 62368-1:2020+A11 and EN61010-1:2010+A1
Reinforced insulation (SOIC6-WB/TSOIC6-WB/SOIC8-WB): V_{IOTM}: 8000V_{PK} V_{IORM}: 2121V_{PK} V_{IOSM}: 12800V_{PK} Basic insulation (DUB8): V_{IOTM}: 5300V_{PK} V_{IORM}: 1414V_{PK} V_{IOSM}: 8125V_{PK}	Single Protection SOIC6-WB: 5.7kV_{RMS} TSOIC6-WB: 5.7kV_{RMS} SOIC8-WB: 5.7kV_{RMS} DUB8: 3.75kV_{RMS}	Reinforced insulation: SOIC6-WB, TSOIC6-WB and SOIC8-WB Basic insulation: DUB8 (Altitude ≤ 5000m)	EN IEC 62368-1: SOIC6-WB: 5.7kV_{RMS} TSOIC6-WB: 5.7kV_{RMS} SOIC8-WB: 5.7kV_{RMS} DUB8: 3.75kV_{RMS} EN61010-1: SOIC6-WB: 5.7kV_{RMS} TSOIC6-WB: 5.7kV_{RMS} SOIC8-WB: 5.7kV_{RMS} DUB8: 3.75kV_{RMS}
Certificate number: 40057278 (Reinforced) DUB8: pending TSOIC6-WB: pending	Certificate number: E511334 TSOIC6-WB: pending	Certificate number: SOIC6-WB: CQC24001453026 SOIC8-WB: CQC24001434134 DUB8: CQC24001452683 TSOIC6-WB: pending	Client reference number: 2253313 TSOIC6-WB: pending

6.8. Safety Limits

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Safety output supply current	R_{qJA} = 126°C/W, V_I = 15V, T_J = 150°C, T_A = 25°C			66	mA
		R_{qJA} = 126°C/W, V_I = 30V, T_J = 150°C, T_A = 25°C			33	
P_S	Safety power dissipation	R_{qJA} = 126°C/W, T_J = 150°C, T_A = 25°C			992	mW
T_S	Maximum safety temperature[1]				150	°C

Note:

1. $T_{J(max)} = T_S = T_A + R_{\theta JA} * P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_s * V_{IN}$, where V_{IN} is the maximum supply voltage.

6.9. Electrical Characteristics

All minimum/maximum specs are at T_A = -40°C to +125°C, V_{CC} = 15V to 30V, V_{EE} = GND, $I_{F\ (on)}$ = 7mA to 16mA, $V_{F(off)}$ = -5V to 0.8V, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} – V_{EE} = 15V, V_{EE} = GND, unless otherwise noted.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
Input						
I_{FLH}	Input diode forward threshold: low to high	V_{out} > 5V, Cg = 1nF	1.5	2.8	4	mA
V_F	Input diode forward voltage	I_F = 10mA	1.8	2.1	2.4	V
V_{F_HL}	Input voltage threshold: high to low	V < 5V, Cg = 1nF	0.9			V
$\Delta V_F/\Delta T$	Temp coefficient of V_F	I_F = 10mA		1.5	1.8	mV/°C
V_R	Input reverse breakdown voltage	I_R = 10μA	7			V
C_{IN}	Input Capacitance	F = 0.5MHz		15		pF
Output						
I_{OH}	High level Output Peak current	I_F = 10mA, V_{CC} = 15V, C_{LOAD} = 0.18μF, C_{VDD} = 10μF, Pulse width <10μs, see Figure 7-2	3	4.7		A
I_{OL}	Low level Output Peak current	V_F = 0V, V_{CC} = 15V, C_{LOAD} = 0.18μF, C_{VDD} = 10uF, Pulse width < 10μs, see Figure 7-2	3.5	6		A
V_{OH}	Output high voltage	I_F = 10mA, I_O = -20mA (respect to V_{CC})		15	40	mV
		I_F = 10mA, I_O = 0mA		V_{CC}		V
V_{OL}	Output low voltage	V_F = V, I_O = 20mA		12	25	mV
I_{CC_H}	Output supply current (e-diode turn on)	I_F = 10mA, I_O = 0mA		1.45	2.2	mA
I_{CC_L}	Output supply current (e-diode turn off)	V_F = 0V, I_O = 0mA		1.4	2.1	mA
Undervoltage-Lockout Threshold (12V UVLO)						
$UVLO_R$	UVLO threshold (V_{CC} rising)	I_F = 10mA	11.0	12.0	13.0	V
$UVLO_F$	UVLO threshold (V_{CC} falling)	I_F = 10mA	10.0	11.0	12.0	V
$UVLO_{HYS}$	Undervoltage-lockout threshold hysteresis			1.0		V
Undervoltage-Lockout Threshold (8V UVLO)						
$UVLO_R$	UVLO threshold (V_{CC} rising)	I_F = 10mA	7.3	8.1	8.9	V
$UVLO_F$	UVLO threshold (V_{CC} falling)	I_F = 10mA	6.7	7.4	8.2	V
$UVLO_{HYS}$	Undervoltage-lockout threshold hysteresis			0.7		V

6.10. Switching Characteristics

All minimum/maximum specs are at T_A = -40°C to +125°C, V_{CC} = 15V to 30V, V_{EE} = GND, $I_{F(on)}$ = 7mA to 16mA, $V_{F(off)}$ = -5V to 0.8V, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} – V_{EE} = 15V, V_{EE} = GND, unless otherwise noted.

Parameters		Test Conditions	Minimum	Typical	Maximum	Unit
t_r	Output rise time	Cg = 1nF, F_{SW} = 20kHz with 50% duty-cycle; V_{CC} = 15V, see Figure 8-1		10	28	ns
t_f	Output fall time			9	25	ns
t_{PLH}	Propagation delay, low to high		40	80	115	ns
t_{PHL}	Propagation delay, high to low		40	70	115	ns
t_{PWD}	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			10	35	ns
$t_{sk(pp)}$	Part to part propagation delay matching	Cg = 1nF, F_{SW} = 20kHz with 50% duty-cycle; V_{CC} = 15V, I_F = 10mA			25	ns
t_{UVLO_rec}	UVLO recovery time	V_{CC} rising from 0V to 15V, see Figure 9-3		18	30	μs
$CMTI_H$	CMTI (output high)	I_F = 10mA, V_{CM} = 1500V, V_{CC} = 30V, T_A = 25°C, see Figure 8-3	150			kV/μs
$CMTI_L$	CMTI (output low)	V_F = 0V, V_{CM} = 1500V, V_{CC} = 30V, T_A = 25°C, see Figure 8-3	150			kV/μs

7. Typical Operating Characteristics

All values are at V_{CC} -V_{EE}= 15V, C_{LOAD} = 1nF for timing specs and C_{LOAD} = 180nF for IOH, IOL specs; T_A = -40°C to +125°C, V_{EE} = GND, bypass V_{CC} to V_{EE} with 1µF capacitor, unless otherwise noted.

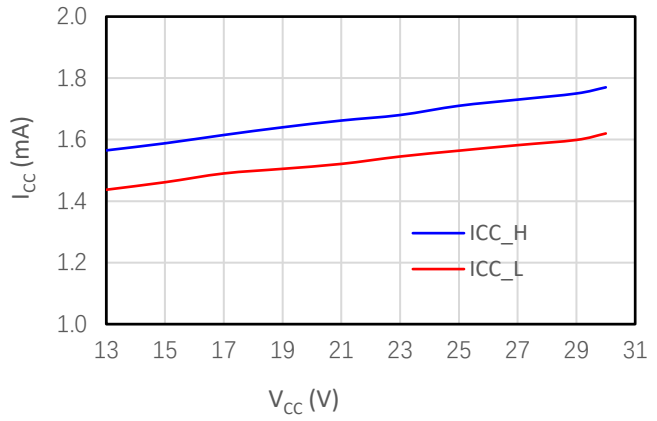


Figure 7-1. V_{CC} supply current vs. VCC supply voltage

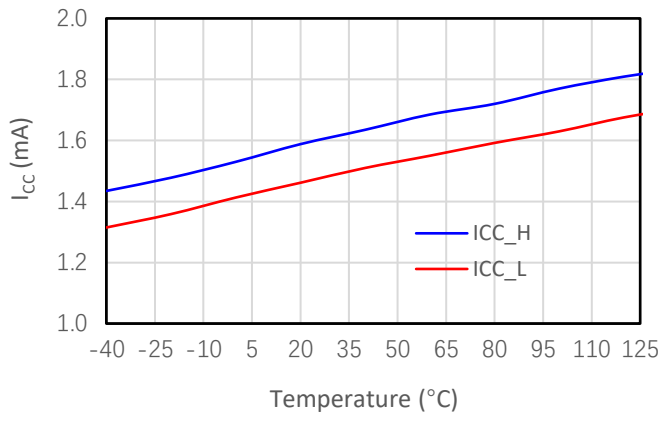


Figure 7-2. V_{CC} supply current vs. Temperature

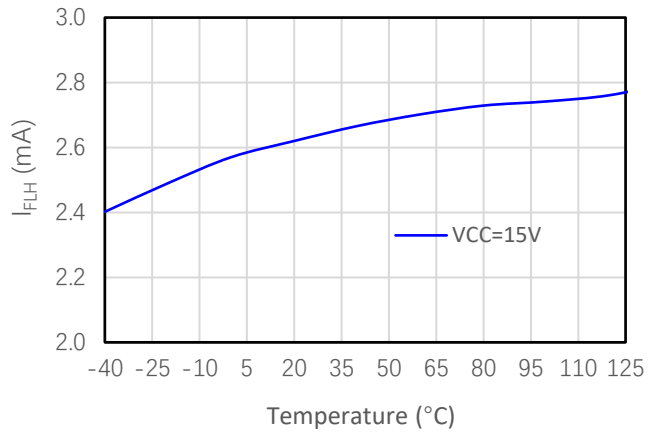


Figure 7-3. Input diode forward threshold vs. Temperature

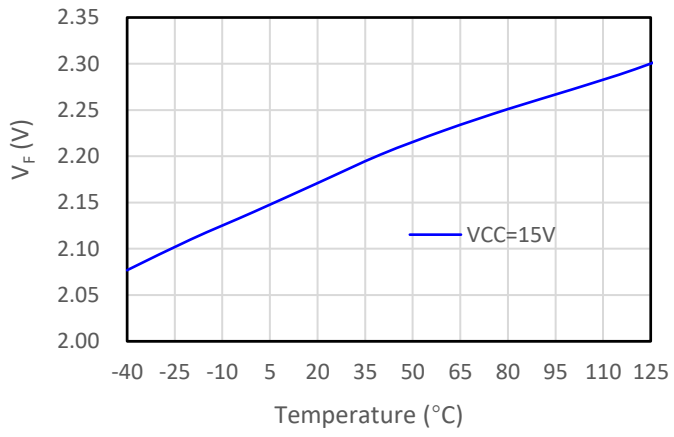


Figure 7-4. Input diode forward voltage vs. Temperature (I_F = 10mA)

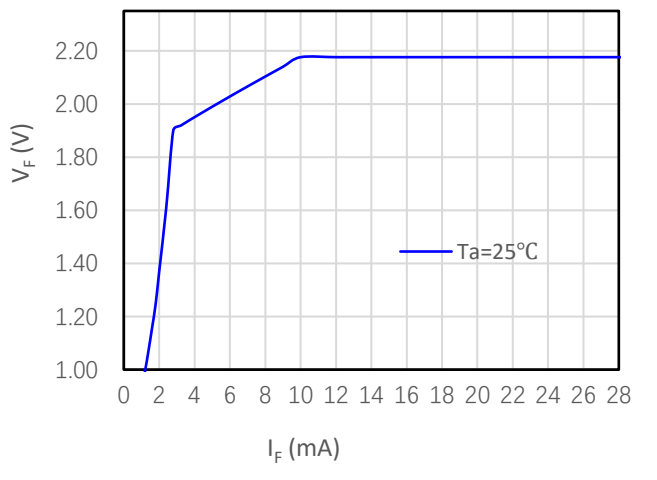


Figure 7-5. Input diode forward voltage vs. Forward current

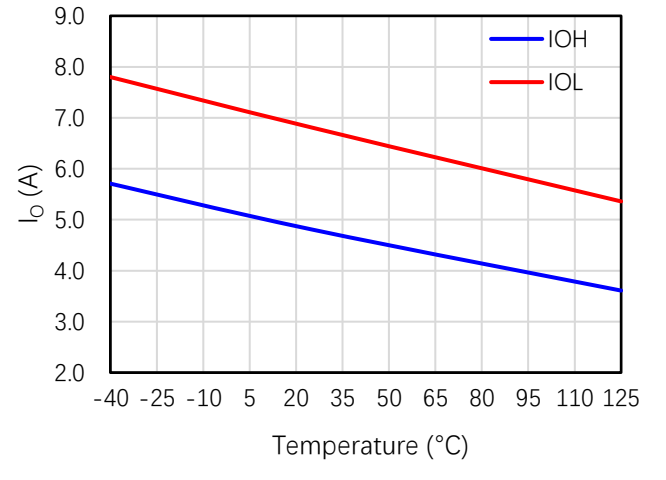


Figure 7-6. Output peak current vs. Temperature

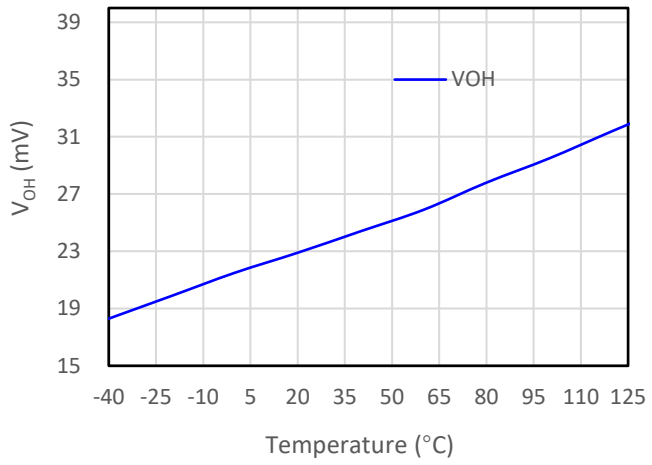


Figure 7-7. V_{OH} vs. Temperature (20mA load current)

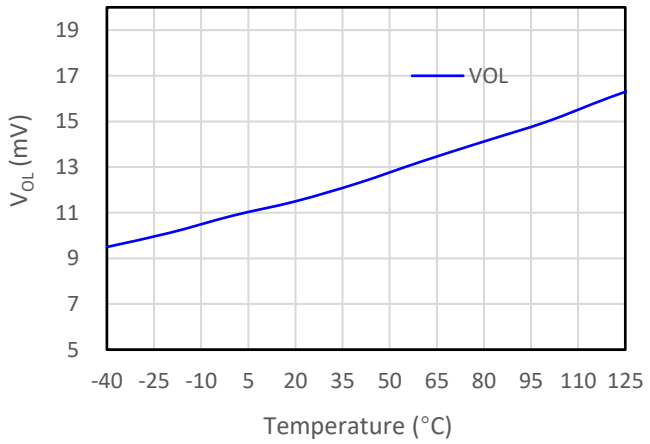


Figure 7-8. V_{OL} vs. Temperature (20mA load current)

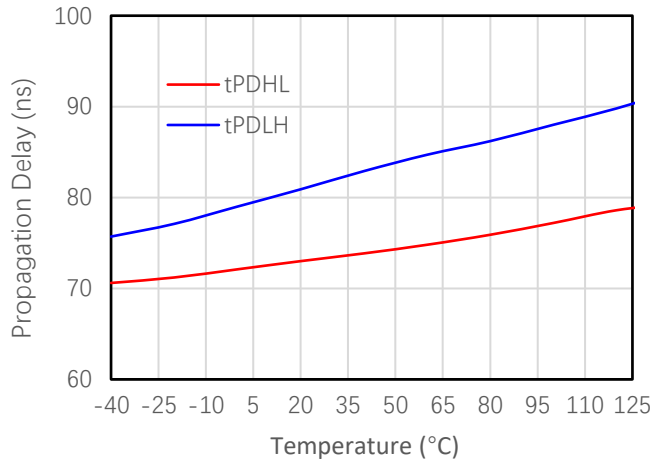


Figure 7-9. Propagation delay vs. Temperature

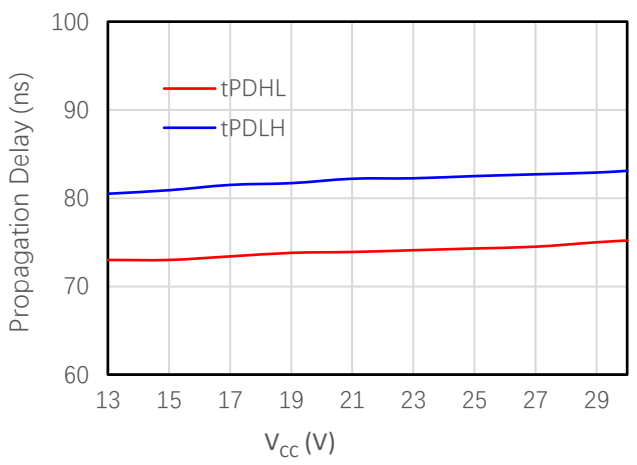


Figure 7-10. Propagation delay vs. V_{CC} supply voltage

8. Parameter Measurement Information

8.1. Propagation Delay and Rising time/Falling time

Figure 8-1 shows the definition and measurement for the propagation delay t_{PLH}, t_{PHL}, and rising time (t_r), falling time (t_f).

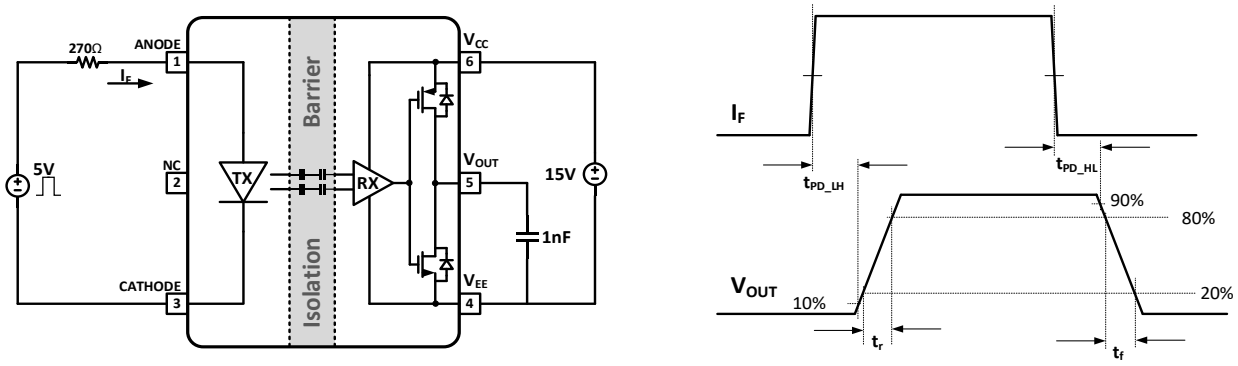


Figure 8-1 Propagation delay and rise time/fall time measurement

8.2. I_{OH} and I_{OL}

Figure 8-2 shows the measurement of output driving current I_{OH} and I_{OL}.

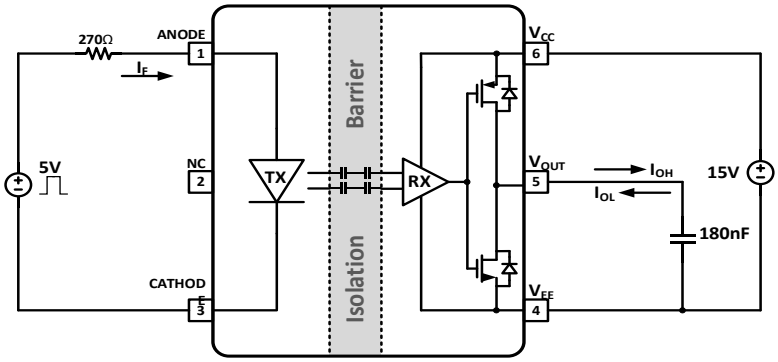


Figure 8-2 I_{OH} and I_{OL} test circuit

8.3. CMTI Test Circuit

Figure 8-3 is the CMTI test configuration.

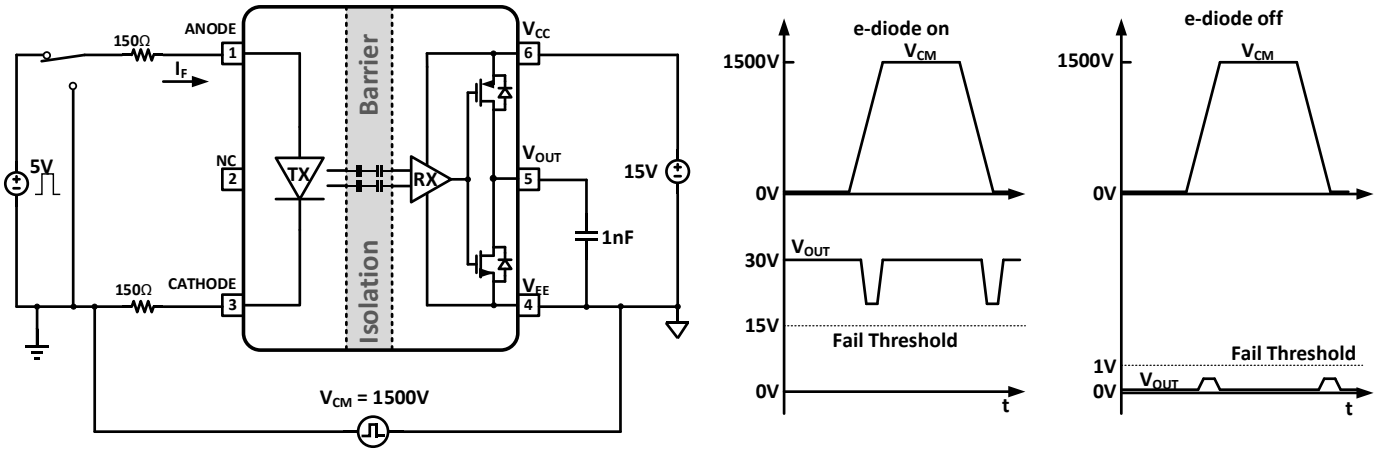


Figure 8-3 Common-mode transient immunity test circuit and waveform

9. Detailed Description

9.1. Overview

The CA-IS3211C is a family of single-channel, opto-compatible isolated gate driver capable of sourcing 4.7A and sinking 6A currents, that can be used to replace industry standard optocoupler-based gate drivers with pin-to-pin compatibility while providing high CMTI, low propagation delay, small pulse width distortion and small part-to-part skew to achieve the fast-switching frequency, and better jitter and propagation delay performance. As the input stage uses an emulated diode (analog diode), these gate drivers offer long term reliability and excellent aging characteristics.

The CA-IS3211C devices are available either in a 6-pin or 8-pin wide-body SOIC packages with 8.5mm of creepage and clearance, also offer DUB8 package with 6.8mm creepage and 6.1mm clearance. All devices are rated for operation at -40°C to +150°C junction temperature. Higher operation temperature range extends gate driver designs in industrial and automotive applications with the high temperature environment that cannot supported by optocoupler-based isolator. Figure 9-1 provides a conceptual block diagram of the CA-IS3211C isolated gate driver. It shows the main elements of CA-IS3211C, including input stage, output stage, V_{CC} UVLO, digital isolator functional groups. Their operations are described separately in the following sections.

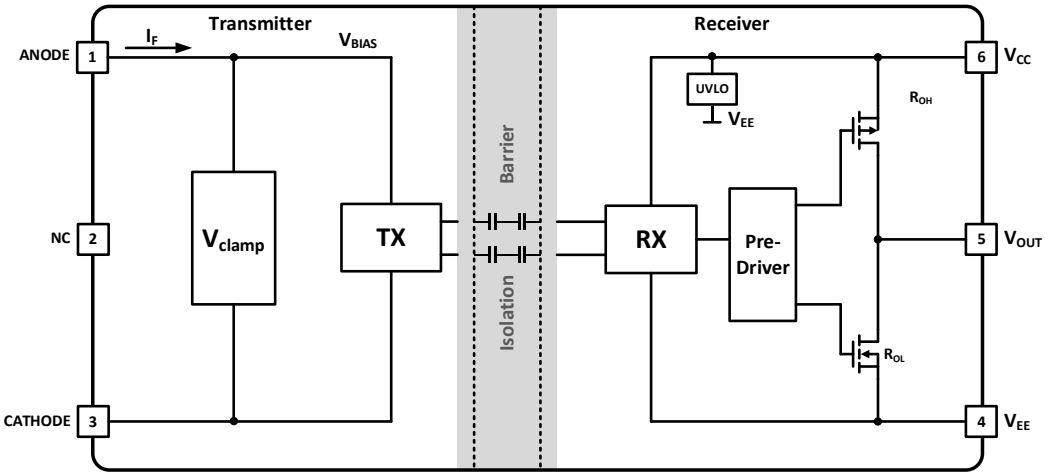


Figure 9-1 Functional block diagram (SOIC6-WB)

9.2. Power Supply

The CA-IS3211C devices operate with dual supplies or a single supply of 10V to 30V (8V UVLO parts) or 14V to 30V (12V UVLO parts) wide voltage range of V_{CC} - V_{EE}, support unbalanced dual supplies operation, making them ideal to drive power MOSFET, IGBT or silicon-carbide (SiC) transistors in various inverter, power supply or motor drive applications. The CA-IS3211CVx offers single terminal gate drive output V_{OUT} and the CA-IS3211CSx offers dual separate output: OUTH and OUTL. All devices can be configured as low-side and high-side drivers. The driver output is pulled to low state to turn-off external power transistors when V_{CC} supply input is either not powered or is in UVLO. Undervoltage lockout (UVLO) with hysteresis is integrated on V_{CC} supply which ensure robust system performance under noisy conditions.

9.3. Input Stage

The input stage of CA-IS3211C integrated an analog diode with anode and cathode pins, see Figure 3-1 the CA-IS3211C input circuit in 6-pin SOIC package. There is no power supply and ground pins on the input-side. Applying a positive voltage between the anode and cathode, the analog diode is forward biased and a forward current I_F flows into the diode. The analog diode features 2.1V typical forward voltage. Like optocoupler-based gate drivers, an external resistor (R_{EXT} in the typical application circuits) is needed to limit the forward current. For the CA-IS3211C devices, the operating forward current range is 7mA to 16mA. If $I_F > I_{FLH}$ (2.8mA, typ.), the isolation transmitter sends a high frequency carrier across the SiO_2 barrier and the isolation receiver demodulates this high-frequency signal and drive output V_{OUT} high; If the anode voltage drops below V_{F_HL} (0.9V, min.), or reverse

biased, the gate driver output is put to low state. The reverse breakdown voltage of the CA-IS3211C input diode is >7V. Refer to Table 9-1 for the inputs vs. output truth table of the CA-IS3211C.

Table 9-1. The CA-IS3211C Inputs vs. Output Truth Table

Input diode	V_{CC}	V_{OUT}
Turn off ($I_F < I_{FLH}$)	$UVLO_R$ to 30V	Low
Turn on ($I_F > I_{FLH}$)	$UVLO_R$ to 30V	High
X[1]	0V to $UVLO_R$, $UVLO_F$ to 0V	Low

Notes:
1. X: Irrelevant

9.4. Driver Output Stage

The output driver stage of the CA-IS3211C integrates a pull-up structure and a pull-down structure. They have distinct current sourcing/sinking capabilities to control the external transistors. Figure 9-2 shows the output stage circuit, The pull-up circuit of CA-IS3211C is simply composed of an p-channel MOSFET. R_{OH} in Figure 9-2 is the on-resistance of the pull-up p-channel MOSFET, the typical value of R_{OH} is 1.2Ω.

The pull-down circuit of CA-IS3211C is simply composed of an n-channel MOSFET. R_{OL} in Figure 9-2 is the on-resistance of the pull-down n-channel MOSFET, the typical value of R_{OL} is 0.6Ω. Because of the very low turn-on impedance of the output stage MOSFETs, the CA-IS3211C isolated gate drivers provide rail-to-rail output (output voltage swings between V_{CC} and V_{EE}). Also, the CA-IS3211C family offers different output option, the CA-IS3211CVx offers single terminal gate drive output and the CA-IS3211CSx offers split output terminals: OUTH and OUTL.

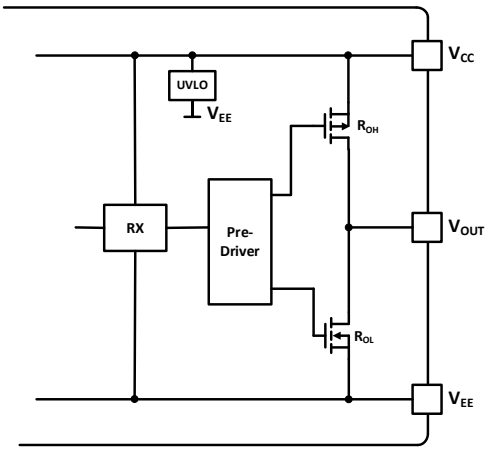


Figure 9-2 Driver output stage

9.5. Undervoltage Lockout (UVLO)

The CA-IS3211C supply (V_{CC}-V_{EE}) is internally monitored for undervoltage conditions. The supply terminal V_{CC} undervoltage detection places the driver output in low state (default state) during an undervoltage event: $V_{CC} < UVLO_R$ during power on, or $V_{CC} < UVLO_F$ during power-down or during normal operation due to a sagging supply voltage. Low state output turns off the external power transistor regardless of the state of the input to avoid under-driven condition on IGBTs and MOSFETs, see Figure 9-3 for more details. The V_{CC} UVLO has hysteresis to avoid chattering when there is ground noise from the power supply, also allows the device to accept small drops in supply voltage and ensures stable operation. Table 9-1 illustrates the output behavior during V_{CC} undervoltage conditions.

Note that before the device enters normal operation and get ready to provide driver output correctly, there is a power-up delay from UVLO rising edge to driver output. This delay time is defined as t_{UVLO_rec} as shown in Figure 9-3. Designers need to leave proper margin before sending PWM signal to gate driver after the V_{CC} supply is ready.

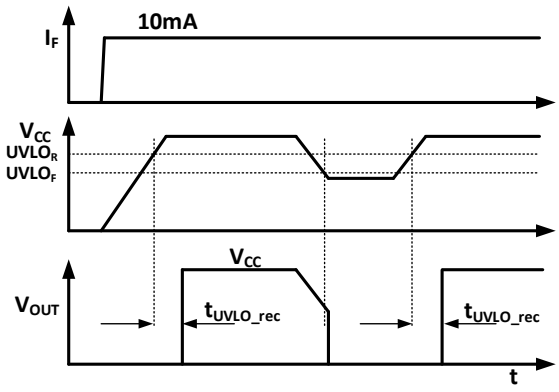


Figure 9-3 UVLO timing diagram

9.6. Active Pulldown

When the V_{CC} supply is in power-off or UVLO condition, the high-side p-channel MOSFET and n-channel MOSFET are held off while the low-side n-channel MOSFET gate is connected to the driver output through a clamp resistor (about 500kΩ). This active clamp circuit holds driver outputs to the threshold voltage of the lower n-channel MOSFET (less than 2.0V) or low state, to turn off the external power transistors when no power is connected to the V_{CC} supply. This prevents the external power transistors from falsely turning on during V_{CC} power off or UVLO.

9.7. Short-Circuit Clamping

The output stage of the CA-IS3211C also features short-circuit clamping function that clamp the driver output voltage and pull the V_{OUT} slightly higher than V_{CC} supply during short-circuit conditions. This protects the external transistors from overvoltage breakdown. The internal conduction diode can support up to 500mA @10μs pulse current and 20mA continuous current. An external diode can be used to provide larger current conduction capability.

10. Application and Implementation

10.1. Typical Application Circuit

The CA-IS3211C isolated gate drivers are designed to drive power MOSFET, IGBT or silicon-carbide (SiC) transistors in various power supply systems to optimize system cost and efficiency. This family of devices can be configured as low-side and high-side drivers. The default-low output keeps the output in low state when V_{CC} supply is in UVLO or power off. The high CMTI rating of 150kV/μs (min), UVLO detection and the propagation delay matching of 25ns (max) part to part make the CA-IS3211C devices ideal to drive high-power transistors in motor drives, industrial inverters, isolated power supply etc. high reliability applications. Figure 10-1 and Figure 10-2 provide the CA-IS3211C typical application circuits for IGBT driving.

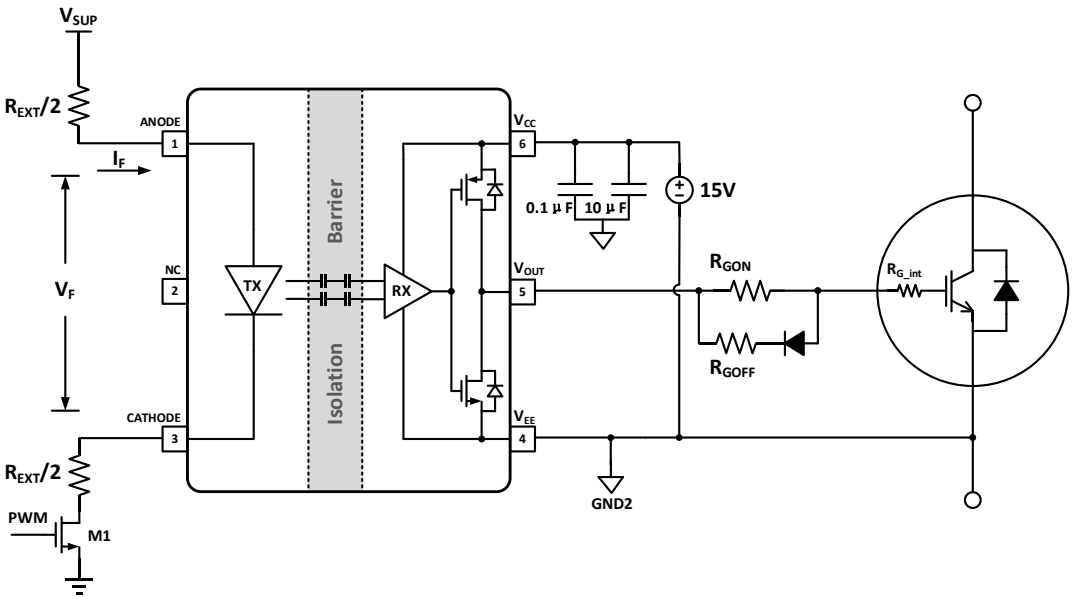


Figure 10-1 Typical application circuit with NMOS & current limit resistor at input side

The gate driver is typically placed between micro-controller (that is MCU or FPGA) and power transistors. As the CA-IS3211C input stage requires 7mA to 16mA forward current to drive the anode to turn-on input diode, most MCUs are not capable of providing enough forward current for this design, an external buffer is needed between the MCU output and CA-IS3211C input in the typical applications, see Figure 9-2. Usually, the buffer power supply is 3.3V or 5.0V, while the forward voltage drop of input diode is typically 2.1V (1.8V to 2.4V) with 1.5mV/°C tempco, needed to add a resistor R_{EXT} before the CA-IS3211C input to limit the forward current. For the input resistor selection, see the Input Current Limit section for more details.

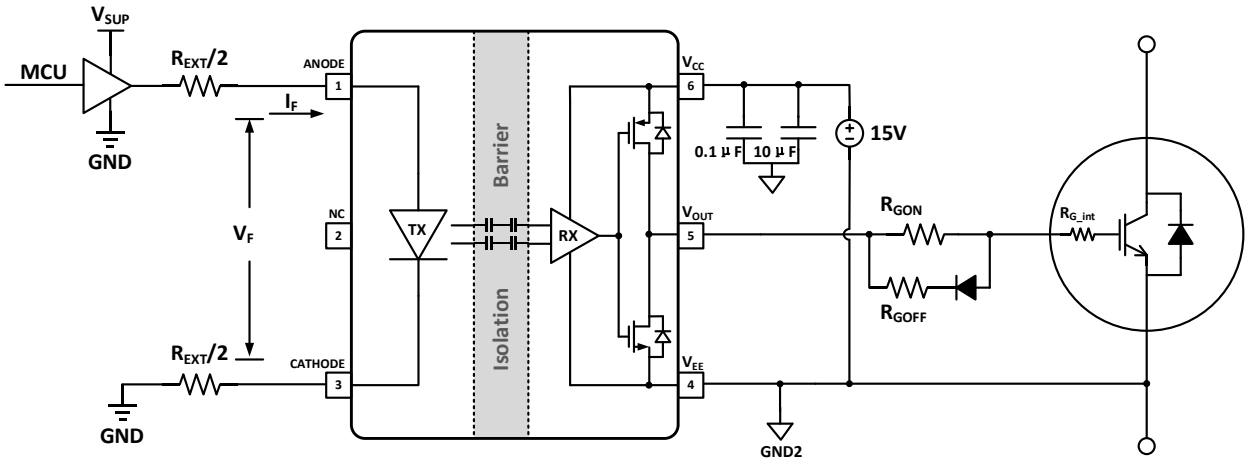


Figure 10-2 Typical application circuit with input buffer and current limit resistor

On the output-side, the power supply V_{CC} can be as high as 30V (32V abs max). The V_{CC} supply can be a single isolated supply up to 30V or isolated bipolar supply such that V_{CC}-V_{EE} does not exceed 30V, or it can be bootstrapped with external diode and capacitors if the system uses a single power supply respected to the power ground. For most operation with single supply, the V_{CC} pin is connected to 15V with respect to ground for IGBT driver, and 18V for SiC MOSFET driver; connect the V_{EE} pin to GND.

For most operation with dual-supplies, the power transistors are turned off with a negative voltage on the gate with respect to the emitter or source. This configuration can prevent the power transistors from unintentionally turning on because of current induced from the Miller effect. The typical supply voltage of the V_{CC} and V_{EE} for bipolar operation are 15V and -8V with respect to GND for IGBT driver, and 18V and -5V for SiC MOSFET driver. Bypass V_{CC} and V_{EE} (for bipolar operation) with at least 10µF/50V low-ESR and low-ESL capacitors to GND. An additional 0.1µF /50V capacitor in parallel with the device biasing capacitor for high frequency filtering. To ensure the best performance, place the decoupling capacitors as close to the power-supply pin as possible.

10.2. Interlock configuration

In the typical applications, the gate drivers are used to drive high-side and low-side power transistors. The MCU generates complementary PWM pulses during normal operation. However, MCU failures or software faults can cause both the high-side and low-side PWM signals from the MCU to latch high. Interlock configuration can be used to prevent the output from being high at same time even both high-side and low-side inputs are pulled high. As shown in Figure 10-3, the anode of the high-side driver's input diode is connected to the cathode of the low-side driver's input diode. The cathode of the high-side driver's input diode is connected to the anode of the low-side driver's input diode. This architecture prevents both the input diodes from being "ON" at the same time, preventing shoot through in the external power transistors.

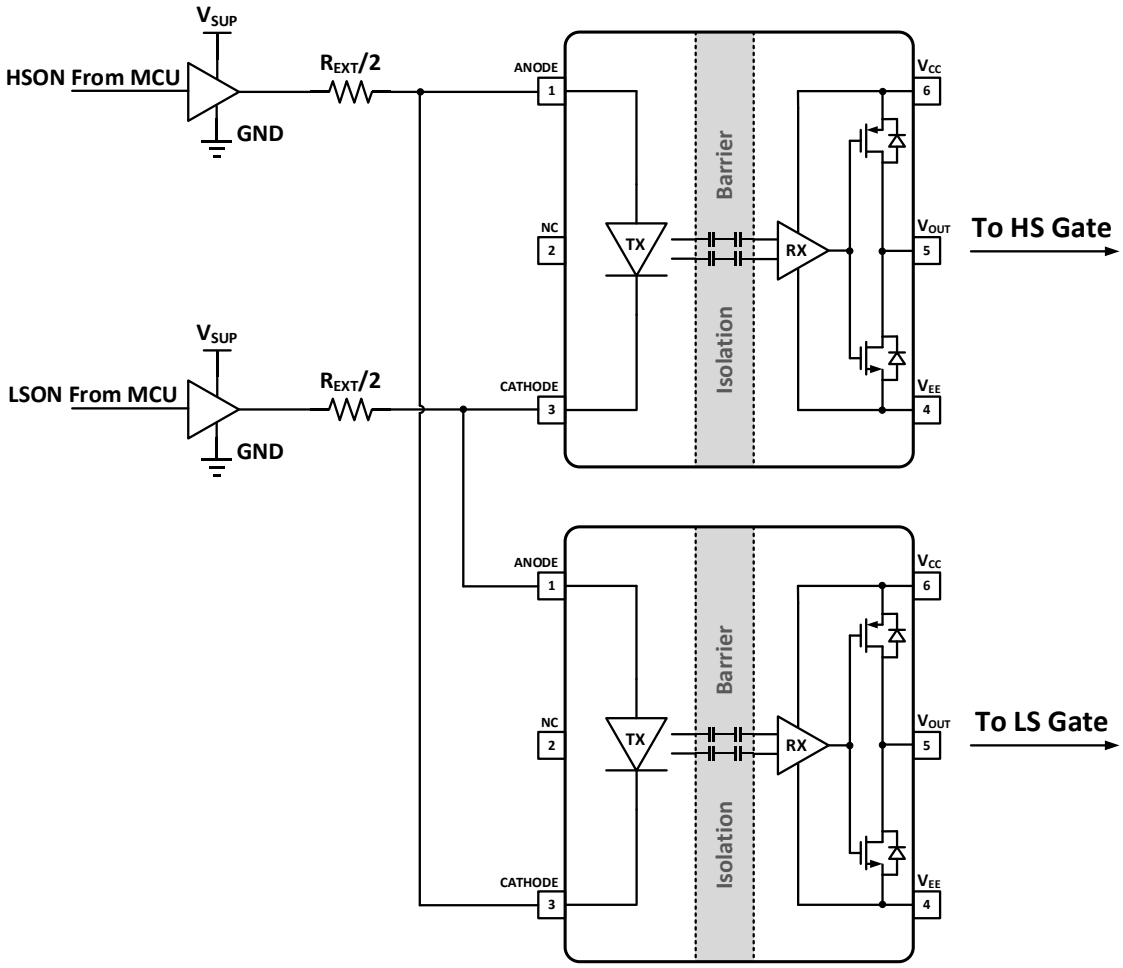


Figure 10-3 Interlock configuration

10.3. Input Current Limit

It is important to select a suitable resistor R_{EXT} to keep the diode forward current within 7mA to 16mA, and must be less than 16mA over the temperature range. The typical value of input diode forward threshold (I_{FLH}) is 2.8mA. In Figure 10-2 application circuit, the R_{EXT} is determined as follows:

$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{OH\_buf}$$

Where:

- I_F is input forward current, the typical value is 10mA, with 7mA minimum value and 16mA maximum value;
- V_{SUP} is the supply voltage of the buffer, typical value is 5V, with 4.75V minimum value and 5.25V maximum value;
- V_F is the input diode forward voltage, typical value is 2.1V (1.8V minimum value and 2.4V maximum value);
- R_{OH_buf} is the buffer's output resistances, typical value is 18Ω (13Ω minimum value and 22Ω maximum value).

Calculate the external resistor R_{EXT} using the above equation,

R_{EXT} =272Ω (typ), or from 204Ω to 310Ω

To turn the input diode off, the voltage between anode and cathode should be less than 0.8V, or IF < IFLH. The input diode can also be reverse biased up to 7V to turn it off and put the gate driver output low.

10.4. Driver Output Resisters Selection

In the typical application circuits Figure 9-1 and Figure 9-2, there are two external gate driver resistors: R_{GOFF} and R_{GON}, R_{GOFF} is the external turn-off resistance; R_{GON} is the external turn-on resistance. These two resistors are chosen to limit the ringing caused by fast switching and parasitic inductances and capacitances, reduce EMI, also can be used to fine-tune gate drive strength and optimize the switching loss. Use the following equations to estimate R_{GOFF} and R_{GON} resistor values.

I_{OH} peak current calculation:

$$I_{OH} = \min\left[4.7A, \frac{V_{CC} - V_{EE}}{\left(R_{OH} + R_{GON} + R_{GFET_{int}}\right)}\right]$$

Where:

- R_{OH} is about1.2Ω.
- R_{GON} is the external turn-on resistance.
- $R_{GFETint}$ is the gate resistance of the external power transistor, this number is available from power transistor datasheet.

I_{OL} peak current calculation:

$$I_{OL} = \min\left[6A, \frac{V_{CC} - V_{EE}}{\left(R_{OL} + R_{GOFF} + R_{GFET_{int}}\right)}\right]$$

Where:

- R_{OL} is about 0.6Ω.
- R_{GOFF} is the external turn-off resistance;
- $R_{GFETint}$ is the gate resistance of the external power transistor, this number is available from power transistor datasheet.

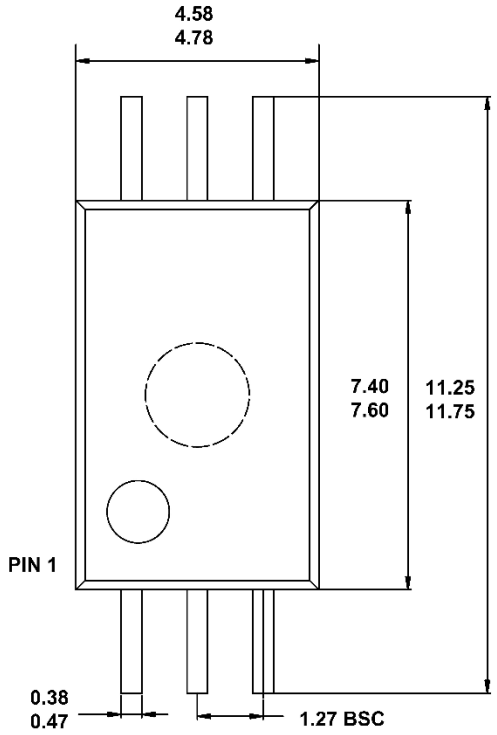
10.5. PCB Layout Guideline

Due to high current levels and fast switching (high dv/dt and di/dt) that radiate noise, proper PC board layout is essential. Follow these guidelines for good PCB layout:

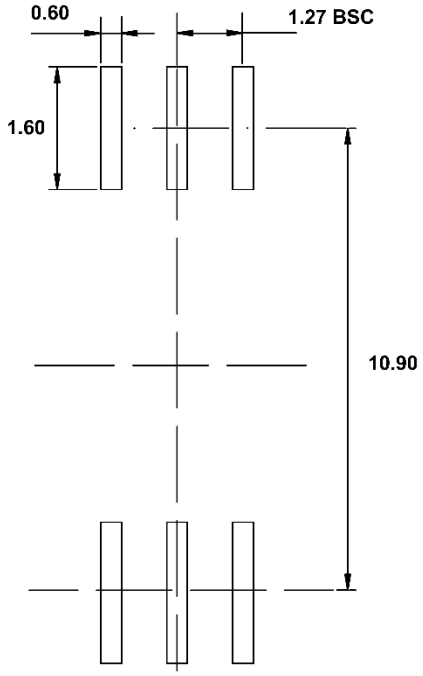
- To ensure the best performance and keep lower supply ripple, place the decoupling capacitors as close to the power-supply pin as possible. We recommend to use low ESR, low ESL MLCC capacitors.
- V_{OUT} connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency-switching operation. This implies that the V_{OUT} loop areas should be minimized. Additionally, small current loop areas reduce radiated EMI. Place the external transistor as close to the gate driver as possible.
- Connect the supply pins (V_{CC}, V_{EE}) to as large a copper pour or plane area as possible for best heat-sinking.
- To ensure isolation performance between the primary side and secondary side, on the top layer and bottom layer keep the space under the CA-IS3211C device free from traces, vias, and pads to maintain maximum creepage distance.
- For the multiple layers design, it is recommended to connect the V_{CC} and V_{EE} pins to internal ground or power planes through multiple vias. These vias should be located close to the IC pins to maximize thermal conductivity, also keep lower parasitic value.

11. Package Information

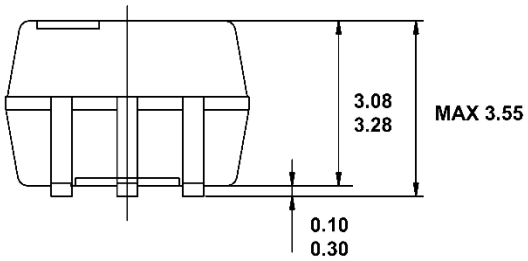
11.1. SOIC6-WB Package Outline



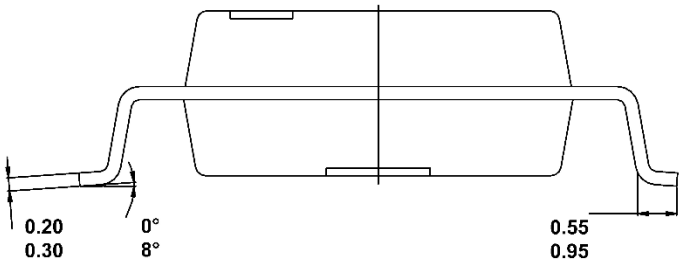
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW

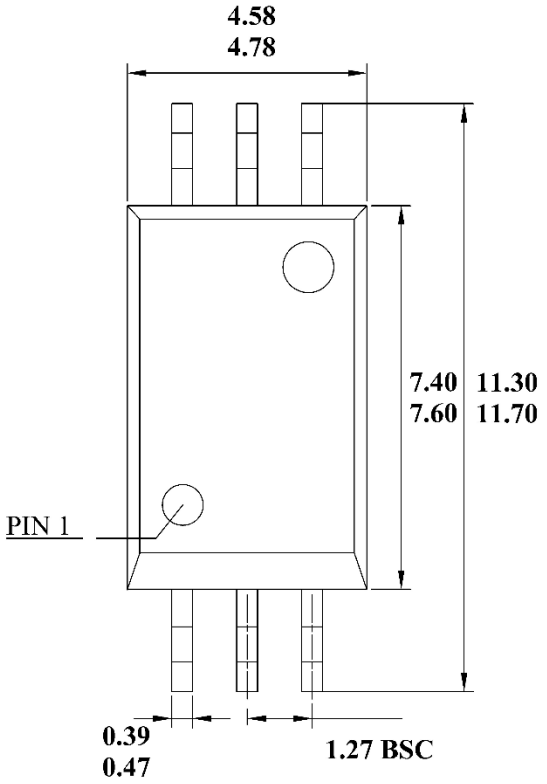


LEFT SIDE VIEW

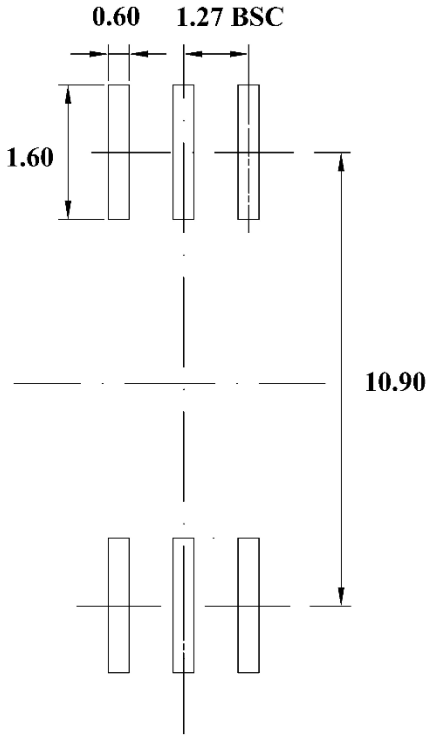
Note:

1. All dimensions are in millimeters, angles are in degrees.

11.2. TSOIC6-WB Package Outline



TOP VIEW



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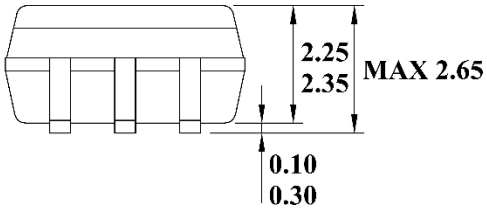
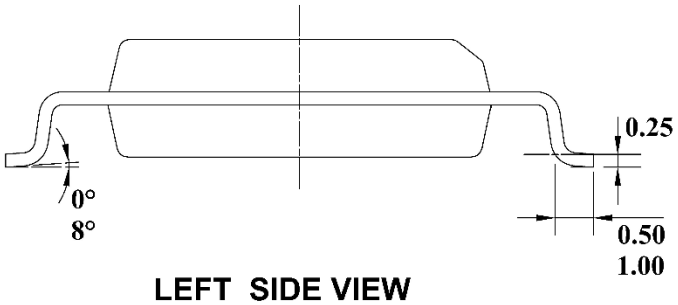


FRONT VIEW

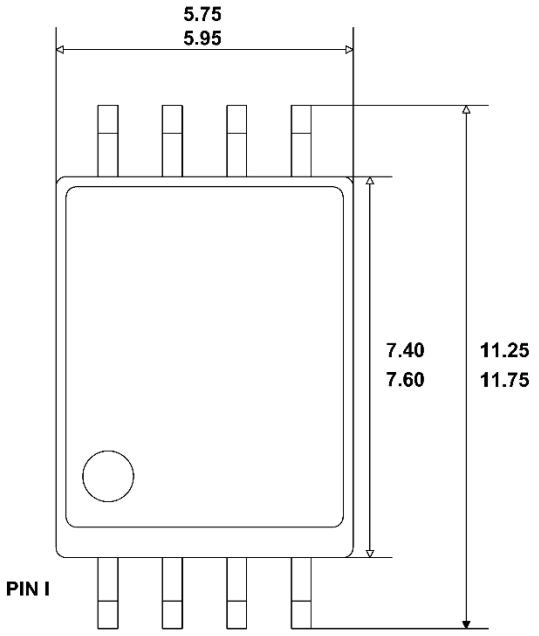


LEFT SIDE VIEW

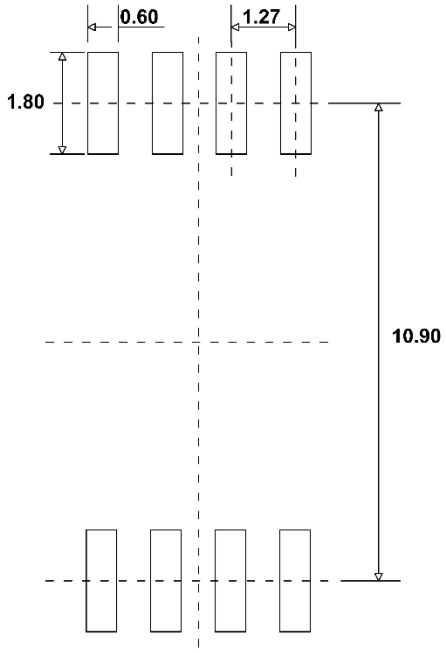
Note:

1. All dimensions are in millimeters, angles are in degrees.

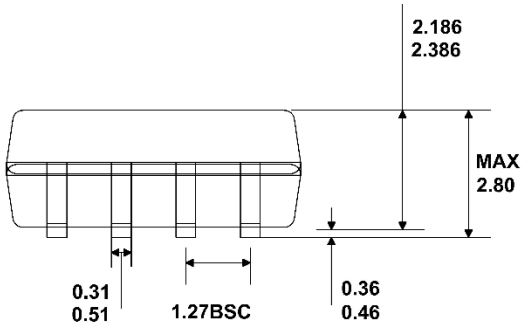
11.3. SOIC8-WB Package Outline



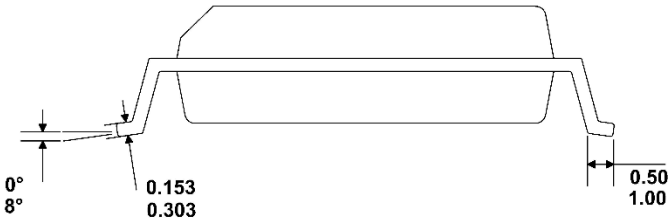
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW

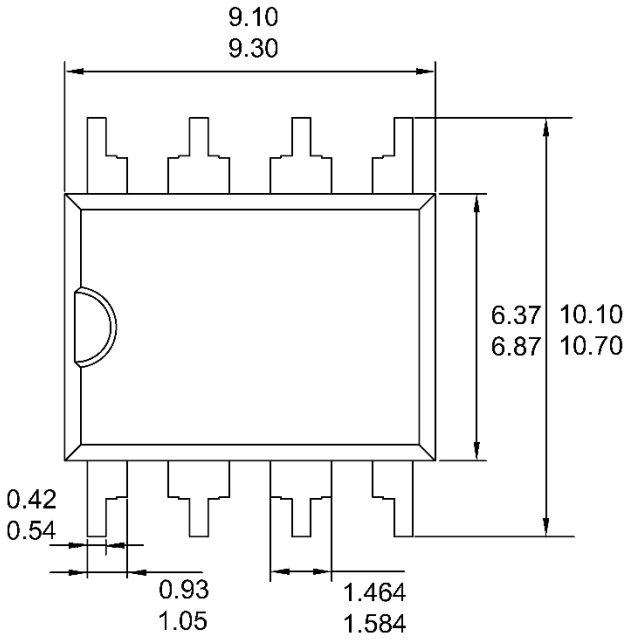


LEFT-SIDE VIEW

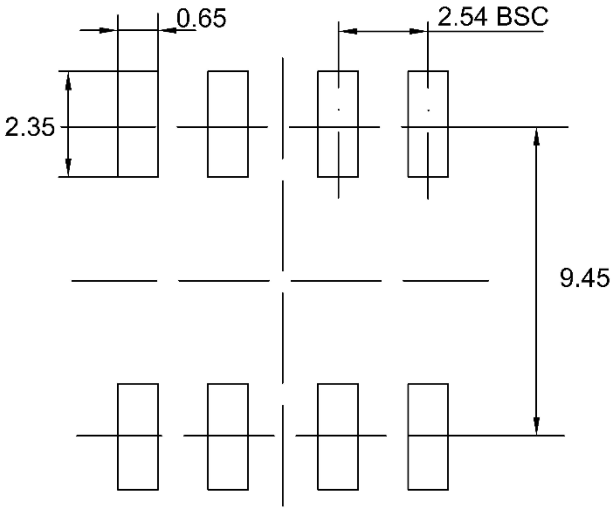
Note:

1. All dimensions are in millimeters, angles are in degrees.

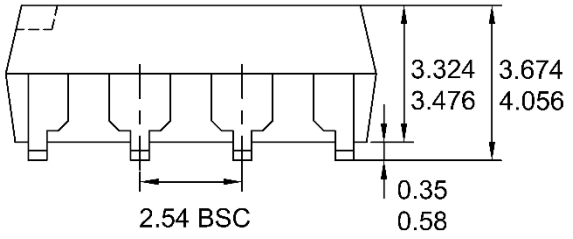
11.4. DUB8 Package Outline



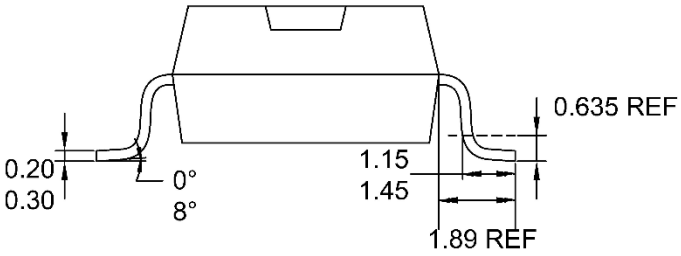
TOP VIEW



RECOMMEDNED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature Profile

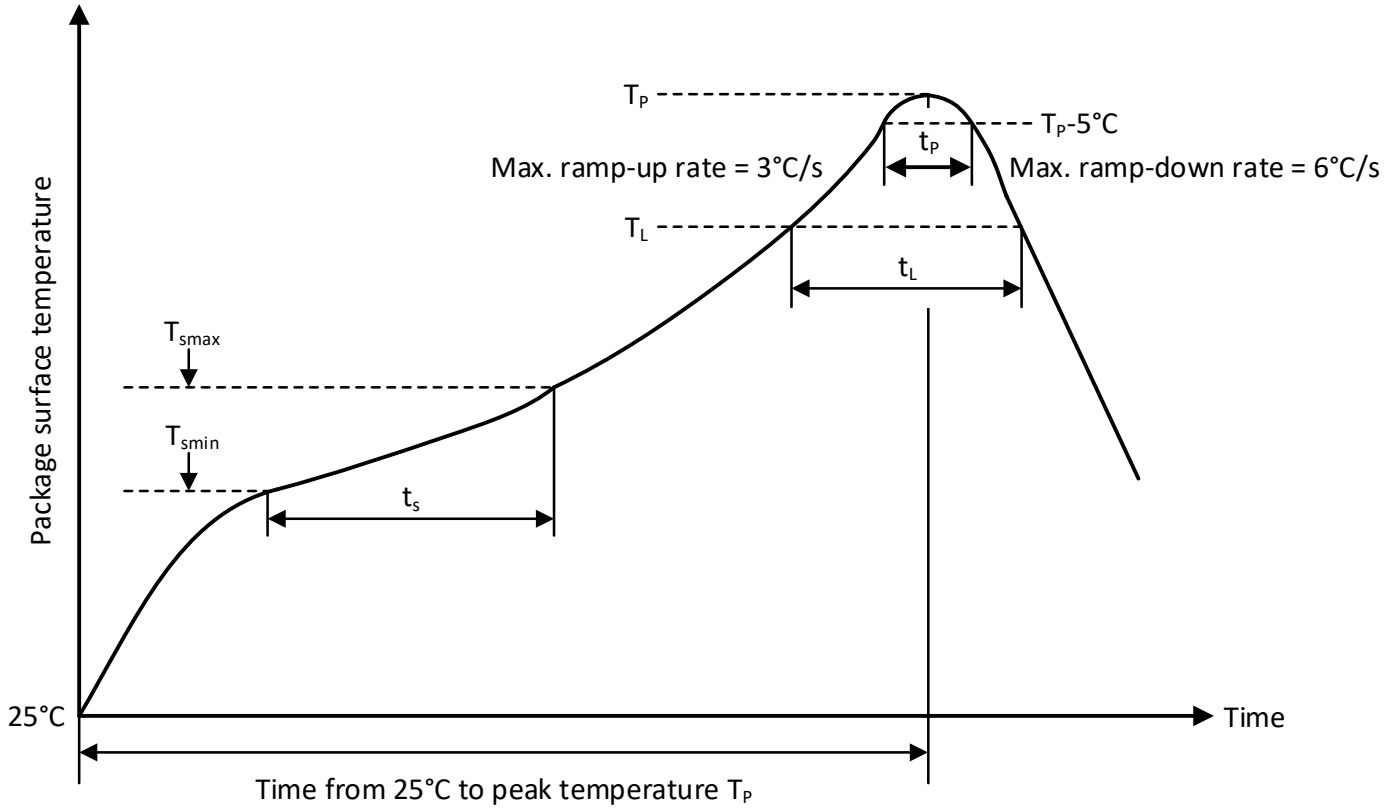


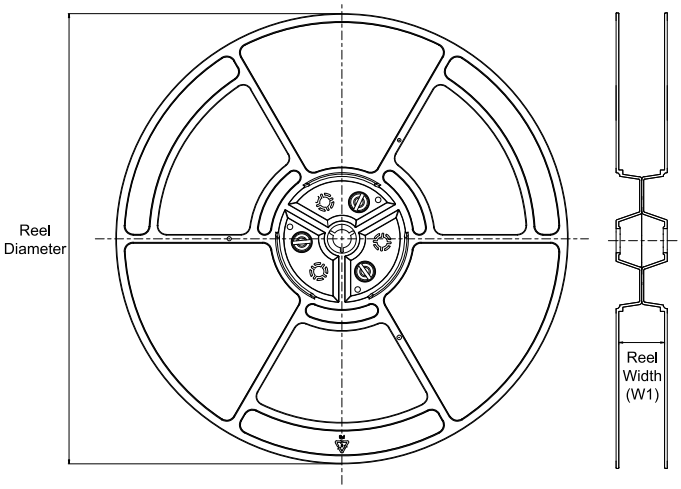
Figure 12-1 Soldering Temperature (Reflow) Profile

Table 12-1 Soldering Temperature Parameter

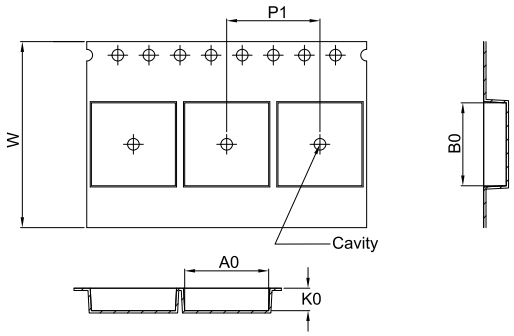
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

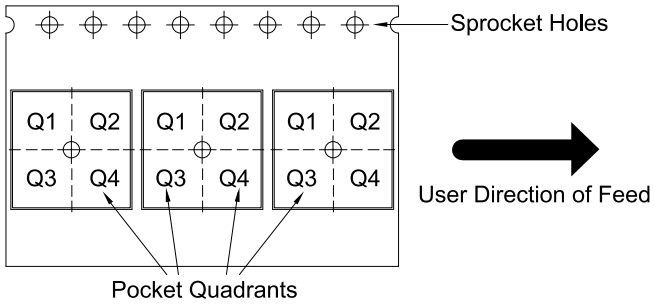


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3211CVBJ	SOIC	J	6	1000	330	16.40	11.95	4.98	3.95	16.00	16.00	Q1
CA-IS3211CVCJ	SOIC	J	6	1000	330	16.40	11.95	4.98	3.95	16.00	16.00	Q1
CA-IS3211CVBTJ	TSOIC	TJ	6	1000	330	16.40	11.95	4.98	TBD	16.00	16.00	Q1
CA-IS3211CVCTJ	TSOIC	TJ	6	1000	330	16.40	11.95	4.98	TBD	16.00	16.00	Q1
CA-IS3211CVBG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3211CVCG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3211CSBG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3211CSCG	SOIC	G	8	1000	330	16.40	11.95	6.15	3.20	16.00	16.00	Q1
CA-IS3211CVBU	DUB	U	8	800	330	24.40	10.90	9.60	4.30	16.00	24.00	Q1
CA-IS3211CVCU	DUB	U	8	800	330	24.40	10.90	9.60	4.30	16.00	24.00	Q1

14. Revision History

Revision Number	Description	Revised Date	Page Changed
Version 1.00	NA	2025/06/20	NA
Version 1.01	Add new part number: CA-IS3211CVCTJ	2025/12/26	1, 2, 4, 8, 13, 21, 25
Version 1.02	Update minimum value of I_{OH} to 3A and I_{OL} to 3.5A Add new part number: CA-IS3211CVBTJ	2026/05/13	9 1, 2, 4, 25
Version 1.03	Update typical value of I_{OH} to 4.7A and I_{OH} to 6A Update Figure 7-6	2026/07/15	1, 9, 13, 18 10

15. Important statement

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