CA-IS382x High-Performance Reinforced Dual-Channel Digital Isolators

1. Key Features

- Signal Rate: DC to 150Mbps
- Wide Operating Supply Voltage: 2.5V to 5.5V
- Wide Operating Temperature Range: -40°C to 125°C
- No Start-Up Initialization Required
- Default Output High and Low Options
- High Electromagnetic Immunity
- High CMTI: ±150kV/μs (Typical)
- Low Power Consumption (Typical):
  - 1.5mA per Channel at 1Mbps with 5.0V Supply
  - 6.6mA per Channel at 100Mbps with 5.0V Supply
- Precise Timing (Typical)
  - 12ns Propagation Delay
  - 1ns Pulse Width Distortion
  - 2ns Propagation Delay Skew
  - 5ns Minimum Pulse Width
- Isolation Rating up to 5.7kVrms (wide body)
- Isolation Rating up to 7.5kVrms (extra wide body)
- ESD：±8kV HBM
- Isolation Barrier Life: >40 Years
- Schmitt Trigger Inputs
- RoHS-Compliant Packages
  - SOIC16 Extra Wide Body
  - SOIC8 Wide Body
  - SOIC16 Wide Body

2. Applications

- Solar Inverter
- Wind-Generated Electricity
- High Voltage Power Storage
- High Voltage Grid System
- EV Charging Station
- Medical Electronics

3. Description

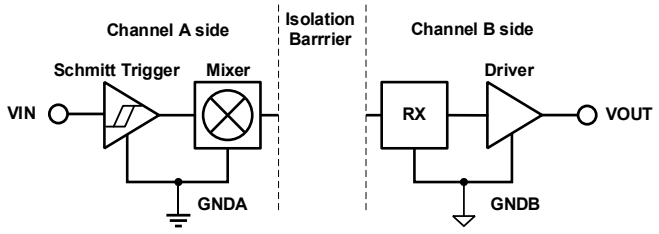
The CA-IS382X devices are high-performance dual - channel digital isolators with precise timing characteristics and low power consumption. The CA-IS382X devices provide high electromagnetic immunity and low emissions, while isolating CMOS digital I/Os. All device versions have Schmitt trigger input for high noise immunity. Each isolation channel consists of a transmitter and a receiver separated by silicon dioxide (SiO_2) insulation barrier. The CA-IS382X device has one forward and one reverse-direction channels. All devices have fail-safe mode option. If the input power or signal is lost, default output is low for devices with suffix L and high for devices with suffix H.

CA-IS382X devices has high insulation capability to handle noise and surge on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. High CMTI ability promises the correct transmission of digital signal. The CA-IS382x devices are available in SOIC8/SOIC16 wide body package and SOIC16 extra wide body package. Products support insulation withstanding up to 5.7kVrms (wide body) and 7.5kVrms (extra wide body)

Device Information

零件号	封装	封装尺寸(标称值)
CA-IS3820 CA-IS3821 CA-IS3822	SOIC8-WB(G)	5.85 mm ×7.50 mm
	SOIC16-WB(W)	10.30mm ×7.50 mm
	SOIC16-WWB(WW)	10.30 mm × 14.00 mm

Simplified Channel Structure



Channel A side and B side are separated by isolation capacitors. GNDA and GNDB are the isolated ground for signals and supplies of A side and B side respectively.

4. Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV_{RMS})	Output Enable	Package
CA-IS3820LG	2	0	Low	5.7	No	SOIC8-WB
CA-IS3820LW	2	0	Low	5.7	No	SOIC16-WB
CA-IS3820LWW	2	0	Low	7.5	Yes	SOIC16-WWB
CA-IS3820HG	2	0	High	5.7	No	SOIC8-WB
CA-IS3820HW	2	0	High	5.7	No	SOIC16-WB
CA-IS3820HWW	2	0	High	7.5	Yes	SOIC16-WWB
CA-IS3821LG	1	1	Low	5.7	No	SOIC8-WB
CA-IS3821LW	1	1	Low	5.7	No	SOIC16-WB
CA-IS3821LWW	1	1	Low	7.5	Yes	SOIC16-WWB
CA-IS3821HG	1	1	High	5.7	No	SOIC8-WB
CA-IS3821HW	1	1	High	5.7	No	SOIC16-WB
CA-IS3821HWW	1	1	High	7.5	Yes	SOIC16-WWB
CA-IS3822LG	1	1	Low	5.7	No	SOIC8-WB
CA-IS3822LW	1	1	Low	5.7	No	SOIC16-WB
CA-IS3822LWW	1	1	Low	7.5	Yes	SOIC16-WWB
CA-IS3822HG	1	1	High	5.7	No	SOIC8-WB
CA-IS3822HW	1	1	High	5.7	No	SOIC16-WB
CA-IS3822HWW	1	1	High	7.5	Yes	SOIC16-WWB

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5. Revision History

Version	Revision history	Page
Version1.00	NA	NA
Version1.01	1. Remove CA-IS382x parts except CA-IS3821HWW,CA-IS3821LWW 2. Updated UL certification information	10
Version1.02	Updated UL, TUV certification information	10
Version1.03	Updated Isolated certification information	9
Version1.04	1. Updated VDE certification information 2. Update Tape and reel information	10 25
Version1.05	Update insulation specifications	8

6. PIN Descriptions and Functions

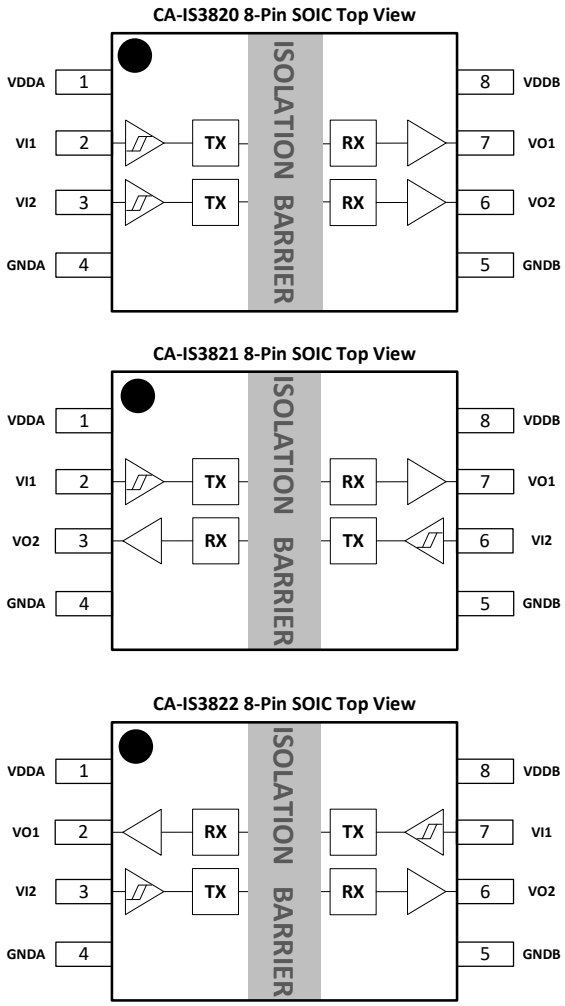


Figure 6-1 SOIC8 wide body package top view

Table 6-1 CA-IS382x SOIC8 Pin Description

Name	SOIC8 Pin No.	Type	Description
V_{DDA}	1	Supply	A side power supply
VI1/VO1	2	Digital I/O	CA-IS3820/21 A side digital input，CA-IS3822 A side digital output
VI2/VO2	3	Digital I/O	CA-IS3820/22 A side digital input，CA-IS3821 A side digital output
GNDA	4	Ground	A side ground
GNDB	5	Ground	B side ground
VI2/VO2	6	Digital I/O	CA-IS3821 B side digital input，CA-IS3820/22 B side digital output
VI1/VO1	7	Digital I/O	CA-IS3822 B side digital input，CA-IS3820/21 B side digital output
V_{DDB}	8	Supply	B side power supply

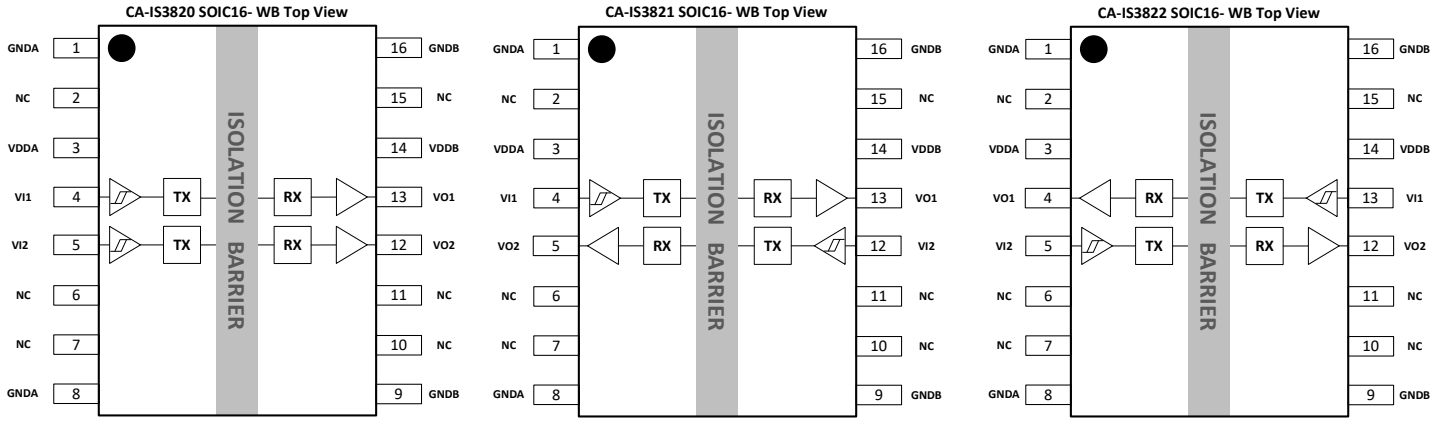


Figure 6-2 CA-IS382x SOIC16-WB wide body package top view

Table 6-2 CA-IS382x SOIC16-WB Pin Description

Name	SOIC16-WB Pin No.	Type	Description
GNDA	1	Ground	A side ground
NC	2	NC	Not connected
VDDA	3	Supply	A side power supply
VI1/VO1	4	Digital I/O	CA-IS3820/21 A side digital input，CA-IS3822 A side digital output
VI2/VO2	5	Digital I/O	CA-IS3820/22 A side digital input，CA-IS3821 A side digital output
NC[1]	6	NC	Not connected
NC	7	NC	Not connected
GNDA	8	Ground	A side ground
GNDB	9	Ground	B side ground
NC	10	NC	Not connected
NC	11	NC	Not connected
VI2/VO2	12	Digital I/O	CA-IS3821 B side digital input，CA-IS3820/22 B side digital output
VI1/VO1	13	Digital I/O	CA-IS3822 B side digital input，CA-IS3820/21 B side digital output
VDDB	14	Supply	B side power supply
NC	15	NC	Not connected
GNDB	16	Ground	B side ground

Note:
1. NC, not connected. Could be floating, or tied to V_{DD} or GND.

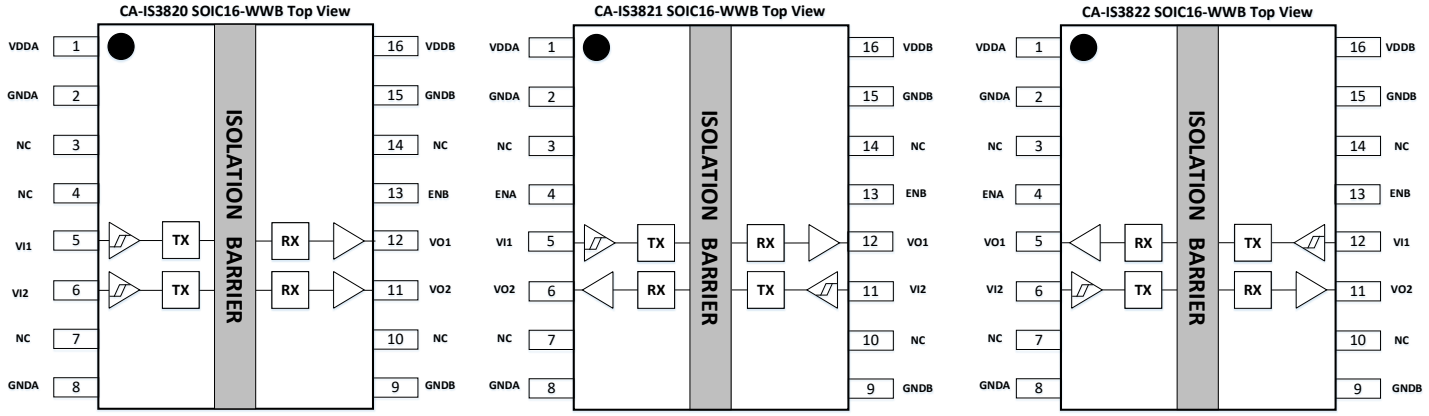


Figure 6- 3 CA-IS382x SOIC16-WWB extra wide body package top view

Table 6- 3 CA-IS382x SOIC16-WWB Pin Description

Name	SOIC16-WWB Pin No.	Type	Description
VDDA	**1**	Supply	A side power supply
GNDA	2	Ground	A side ground
NC	3	NC	Not connected
ENA/NC	4	Enable/NC	CA-IS3821/22 A side output enable. For CA-IS3820, not connected
VI1/VO1	5	Digital I/O	CA-IS3820/21 A side digital input，CA-IS3822 A side digital output
VI2/VO2	6	Digital I/O	CA-IS3820/22 A side digital input，CA-IS3821 A side digital output
NC[1]	7	NC	Not connected
GNDA	8	Ground	A side ground
GNDB	9	Ground	B side ground
NC	10	NC	Not connected
VI2/VO2	11	Digital I/O	CA-IS3821 B side digital input，CA-IS3820/22 B side digital output
VI1/VO1	12	Digital I/O	CA-IS3822 B side digital input，CA-IS3820/21 B side digital output
ENB	13	Enable	B side output enable
NC	14	NC	Not connected
GNDB	15	Ground	B side ground
VDDB	16	Supply	B side power supply

Note:
NC, not connected. Could be floating, or tied to V_{DD} or GND

7. Specifications

7.1. Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
V_{DDA}, V_{DDB}	Supply Voltage[2]	-0.5	6.0	V
V_{in}	Voltage at Ax, Bx, ENx	-0.5	V_{DDA}+0.5[3]	V
I_O	Output Current	-20	20	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 7 V.

7.2. ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, to the Pins on the same side[1]	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±2000	

NOTE:

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3. Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{DDA}, V_{DDB}	Supply Voltage		2.375	3.3	5.5	V
$V_{DD\ (UVLO+)}$	VDD Undervoltage Threshold When Supply Voltage is Rising		1.95	2.24	2.375	V
$V_{DD\ (UVLO-)}$	VDD Undervoltage Threshold When Supply Voltage is Falling		1.88	2.10	2.325	V
$V_{HYS\ (UVLO)}$	VDD Undervoltage Threshold Hysteresis		70	140	250	mV
I_{OH}	High-level Output Current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO} = 3.3V	-2			
		V_{DDO} = 2.5V	-1			
I_{OL}	Low-level Output Current	V_{DDO} = 5V			4	mA
		V_{DDO} = 3.3V			2	
		V_{DDO} = 2.5V			1	
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
DR	Data Rate		0		150	Mbps
T_A	Ambient Temperature		-40	27	125	°C

NOTE:

1. V_{DDO} = Output-side V_{DD}

7.4. Thermal Information

thermal resistance		CA-IS382x			Unit
		SOIC8-WB(G)	SOIC16-WB(W)	SOIC16-WWB(WW)	
$R_{\theta JA}$	Junction-to-ambient	92.3	83.4	83.4	°C/W

7.5. Power Rating

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CA-IS3820						
P_D	Max. Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, input 75MHz 50% duty cycle square wave			240	mW
P_{DA}	A side dissipation				30	mW
P_{DB}	B side dissipation				210	mW
CA-IS3821						
P_D	Max. Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, input 75MHz 50% duty cycle square wave			240	mW
P_{DA}	A side dissipation				120	mW
P_{DB}	B side dissipation				120	mW
CA-IS3822						
P_D	Max. Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, input 75MHz 50% duty cycle square wave			240	mW
P_{DA}	A side dissipation				120	mW
P_{DB}	B side dissipation				120	mW

7.6. Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE		UNIT
			G/W	WW	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	>15	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	>15	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28		μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600		V
	Material group	According to IEC 60664-1	I		
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	I-IV	
DIN V VDE V 0884-17:2021-10[2]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	2828	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1500	2000	V_{RMS}
		DC voltage	2121	2828	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	8000		V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000		V_{PK}
q_{pd}	Apparent charge[4]	Method a, After Input/Output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5		pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5		
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5		
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5700	7500	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.7. Safety-Related Certifications

VDE	UL	TUV
Certified according to DIN V VDE V 0884-17:2021-10	Recognized under UL 1577 Component Recognition Program	Recognized under EN 61010-1:2010+A1
Maximum transient isolation voltage： 8000V_{pk}(SOIC8-WB), 8000V_{pk}(SOIC16-WB) and 8000V_{pk}(SOIC16-WWB) Maximum repetitive peak isolation voltage： 2121V_{pk}(SOIC8-WB), 2121V_{pk}(SOIC16-WB) and 2828V_{pk}(SOIC16-WWB) Maximum surge isolation voltage： 8000V_{pk}(SOIC8-WB), 8000V_{pk}(SOIC16-WB) and 8000V_{pk}(SOIC16-WWB)	Single Protection: SOIC8-WB:5700V_{RMS}; SOIC16-WB:5700V_{RMS}; SOIC16-WWB: 7500 V_{RMS}	SOIC8-WB:5700V_{RMS}; SOIC16-WB: 5700 V_{RMS}; SOIC16-WWB: 5700 V_{RMS}
Certification number: 40057278	Certification Number：E511334	Certification Number：CN23RC4J 001

7.8. Electrical Characteristics

7.8.1. V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; *See Figure 8-1*	V_{DDO}[1]-0.4	4.8		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; *See Figure 8-1*		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Logic High		2			V
$V_{IT-(IN)}$	Negative-going Input Logic Low				0.8	V
$V_{IT+(EN)}$	EN Pin input Logic High		0.7*V_{DD}			V
$V_{IT-(EN)}$	EN Pin input Logic Low				0.3*V_{DD}	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at Ax or Bx			20	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-20			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; *See Figure 8-3*	100	150		kV/μS
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 5 V		2		pF

NOTE:

1. V_{DDI} = Input-side V_{DD}, V_{DDO} = Output-side V_{DD}
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω ± 40%.
3. Measured from pin to Ground.

7.8.2. V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -2mA; *See Figure 8-1*	V_{DDO}[1]-0.4	3.1		V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA; *See Figure 8-1*		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Logic High		2			V
$V_{IT-(IN)}$	Negative-going Input Logic Low				0.8	V
$V_{IT+(EN)}$	EN Pin input Logic High		0.7*V_{DD}			V
$V_{IT-(EN)}$	EN Pin input Logic Low				0.3*V_{DD}	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at Ax or Bx			20	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-20			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; *See Figure 8-3*	100	150		kV/μS
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 3.3 V		2		pF

NOTE:

4. V_{DDI} = Input-side V_{DD}, V_{DDO} = Output-side V_{DD}
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω ± 40%.
6. Measured from pin to Ground.

7.8.3. V_{DDA} = V_{DDB} = 2.5 V ± 5%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -1mA; *See Figure 8-1*	V_{DDO}[1]-0.4	2.3		V
V_{OL}	Low-level Output Voltage	I_{OL} = 1mA; *See Figure 8-1*		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Logic High		2			V
$V_{IT-(IN)}$	Negative-going Input Logic Low				0.8	V
$V_{IT+(EN)}$	EN Pin input Logic High		0.7*V_{DD}			V
$V_{IT-(EN)}$	EN Pin input Logic Low				0.3*V_{DD}	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at Ax or Bx			20	μA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-20			μA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; *See Figure 8-3*	100	150		kV/μS

C_I Input Capacitance[3]	$V_I = V_{DD}/2 + 0.4\times\sin(2\pi ft)$, f = 1 MHz, V_{DD} = 5 V	2	pF

NOTE:

7. V_{DDI} = Input-side V_{DD}, V_{DDO} = Output-side V_{DD}
8. The nominal output impedance of an isolator driver channel is approximately 50 Ω ± 40%.
9. Measured from pin to Ground.

7.9. Supply Current Characteristics

7.9.1. V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40°C to 125°C

PARAMETER	TEST CONDITION		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3820							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3820L); V_{IN} = V_{DDI}[1] (CA-IS3820H)		I_{DDA}		0.9	1.3	mA
			I_{DDB}		1.4	2.2	
	V_{IN} = V_{DDI} (CA-IS3820L); V_{IN} = 0V(CA-IS3820H)		I_{DDA}		2.5	4.1	
			I_{DDB}		1.5	2.3	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		1.7	2.7	
			I_{DDB}		2.2	3.2	
		10Mbps (5MHz)	I_{DDA}		1.8	2.9	
			I_{DDB}		8.8	11.8	
		100Mbps (50MHz)	I_{DDA}		2.5	3.9	
			I_{DDB}		22	30.0	
CA-IS3821							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3821L); V_{IN} = V_{DDI} (CA-IS3821H)		I_{DDA}		1.6	3.2	mA
			I_{DDB}		1.6	3.2	
	V_{IN} = V_{DDI} (CA-IS3821L); V_{IN} = 0V(CA-IS3821H)		I_{DDA}		2.9	5.8	
			I_{DDB}		2.9	5.8	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		2.1	3.2	
			I_{DDB}		2.1	3.2	
		10Mbps (5MHz)	I_{DDA}		5.6	7.8	
			I_{DDB}		5.6	7.8	
		100Mbps (50MHz)	I_{DDA}		12.9	22	
			I_{DDB}		12.9	22	
CA-IS3822							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3822L); V_{IN} = V_{DDI} (CA-IS3822H)		I_{DDA}		1.6	3.2	mA
			I_{DDB}		1.6	3.2	
	V_{IN} = V_{DDI} (CA-IS3822L); V_{IN} = 0V(CA-IS3822H)		I_{DDA}		2.9	5.8	
			I_{DDB}		2.9	5.8	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		2.1	3.2	
			I_{DDB}		2.1	3.2	
		10Mbps (5MHz)	I_{DDA}		5.6	7.8	
			I_{DDB}		5.6	7.8	
		100Mbps (50MHz)	I_{DDA}		12.9	22	
			I_{DDB}		12.9	22	

Note:
1. V_{DDI} = input side V_{DD}

7.9.2. V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C

PARAMETER	TEST CONDITION		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3820							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3820L); V_{IN} = V_{DDI}[1] (CA-IS3820H)		I_{DDA}		0.8	1.3	mA
			I_{DDB}		1.3	2.0	
	V_{IN} = V_{DDI} (CA-IS3820L); V_{IN} = 0V(CA-IS3820H)		I_{DDA}		2.4	4.0	
			I_{DDB}		1.4	2.2	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		1.6	2.7	
			I_{DDB}		1.9	2.7	
		10Mbps (5MHz)	I_{DDA}		1.7	2.7	
			I_{DDB}		6.2	8.4	
		100Mbps (50MHz)	I_{DDA}		2.2	3.5	
			I_{DDB}		14.4	19.7	
CA-IS3821							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3821L); V_{IN} = V_{DDI} (CA-IS3821H)		I_{DDA}		1.2	1.9	mA
			I_{DDB}		1.2	1.9	
	V_{IN} = V_{DDI} (CA-IS3821L); V_{IN} = 0V(CA-IS3821H)		I_{DDA}		2.3	3.3	
			I_{DDB}		2.3	3.3	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		1.9	2.9	
			I_{DDB}		1.9	2.9	
		10Mbps (5MHz)	I_{DDA}		4.2	5.9	
			I_{DDB}		4.2	5.9	
		100Mbps (50MHz)	I_{DDA}		8.8	12.1	
			I_{DDB}		8.8	12.1	
CA-IS3822							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3822L); V_{IN} = V_{DDI} (CA-IS3822H)		I_{DDA}		1.2	1.9	mA
			I_{DDB}		1.2	1.9	
	V_{IN} = V_{DDI} (CA-IS3822L); V_{IN} = 0V(CA-IS3822H)		I_{DDA}		2.3	3.3	
			I_{DDB}		2.3	3.3	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 3.3V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		1.9	2.9	
			I_{DDB}		1.9	2.9	
		10Mbps (5MHz)	I_{DDA}		4.2	5.9	
			I_{DDB}		4.2	5.9	
		100Mbps (50MHz)	I_{DDA}		8.8	12.1	
			I_{DDB}		8.8	12.1	

Note:
1. V_{DDI} = input side V_{DD}

7.9.3. V_{DDA} = V_{DDB} = 2.5 V ± 5%, T_A = -40 to 125°C

PARAMETER	TEST CONDITION		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3820							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3820L); V_{IN} = V_{DDI}[1] (CA-IS3820H)		I_{DDA}		0.8	1.2	mA
			I_{DDB}		1.4	2.0	
	V_{IN} = V_{DDI} (CA-IS3820L); V_{IN} = 0V(CA-IS3820H)		I_{DDA}		2.4	4.0	
			I_{DDB}		1.4	2.1	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		1.6	2.6	
			I_{DDB}		1.7	2.5	
		10Mbps (5MHz)	I_{DDA}		1.7	2.7	
			I_{DDB}		5.0	6.8	
		100Mbps (50MHz)	I_{DDA}		2.1	3.4	
			I_{DDB}		10.8	14.7	
CA-IS3821							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3821L); V_{IN} = V_{DDI} (CA-IS3821H)		I_{DDA}		1.5	1.9	mA
			I_{DDB}		1.5	1.9	
	V_{IN} = V_{DDI} (CA-IS3821L); V_{IN} = 0V(CA-IS3821H)		I_{DDA}		2.1	3.1	
			I_{DDB}		2.1	3.1	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		1.9	2.8	
			I_{DDB}		1.9	2.8	
		10Mbps (5MHz)	I_{DDA}		3.6	5.2	
			I_{DDB}		3.6	5.2	
		100Mbps (50MHz)	I_{DDA}		6.9	9.5	
			I_{DDB}		6.9	9.5	
CA-IS3822							
Supply Current – DC Signal	V_{IN} = 0V (CA-IS3822L); V_{IN} = V_{DDI} (CA-IS3822H)		I_{DDA}		1.5	1.9	mA
			I_{DDB}		1.5	1.9	
	V_{IN} = V_{DDI} (CA-IS3822L); V_{IN} = 0V(CA-IS3822H)		I_{DDA}		2.1	3.1	
			I_{DDB}		2.1	3.1	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 2.5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		1.9	2.8	
			I_{DDB}		1.9	2.8	
		10Mbps (5MHz)	I_{DDA}		3.6	5.2	
			I_{DDB}		3.6	5.2	
		100Mbps (50MHz)	I_{DDA}		6.9	9.5	
			I_{DDB}		6.9	9.5	

Note:
1. V_{DDI} = input side V_{DD}

7.10. Timing Characteristics

7.10.1. V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	*See Figure 8-1*		12.0	15.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]			2.0	4.5	ns
t_r	Output Signal Rise Time	*See Figure 8-1*		2.5	4.0	ns
t_f	Output Signal Fall Time	*See Figure 8-1*		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	*See Figure 8-2*		8	12	µs
t_{SU}	Start-up Time			15	40	µs

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.10.2. V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	*See Figure 8-1*		12.0	17.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]			2.0	4.5	ns
t_r	Output Signal Rise Time	*See Figure 8-1*		2.5	4.0	ns
t_f	Output Signal Fall Time	*See Figure 8-1*		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	*See Figure 8-2*		8	12	µs
t_{SU}	Start-up Time			15	40	µs

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

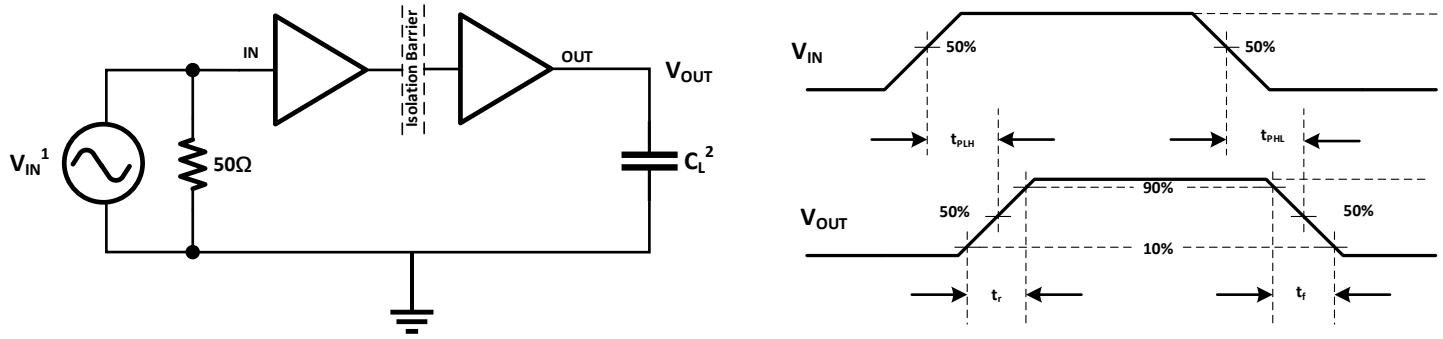
7.10.3. V_{DDA} = V_{DDB} = 2.5 V ± 5%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	*See Figure 8-1*		12.0	20.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	5.0	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]			2.0	5.0	ns
t_r	Output Signal Rise Time	*See Figure 8-1*		2.5	4.0	ns
t_f	Output Signal Fall Time	*See Figure 8-1*		2.5	4.0	ns
t_{DO}	Default Output Delay Time from Input Power Loss	*See Figure 8-2*		8	12	µs
t_{SU}	Start-up Time			15	40	µs

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

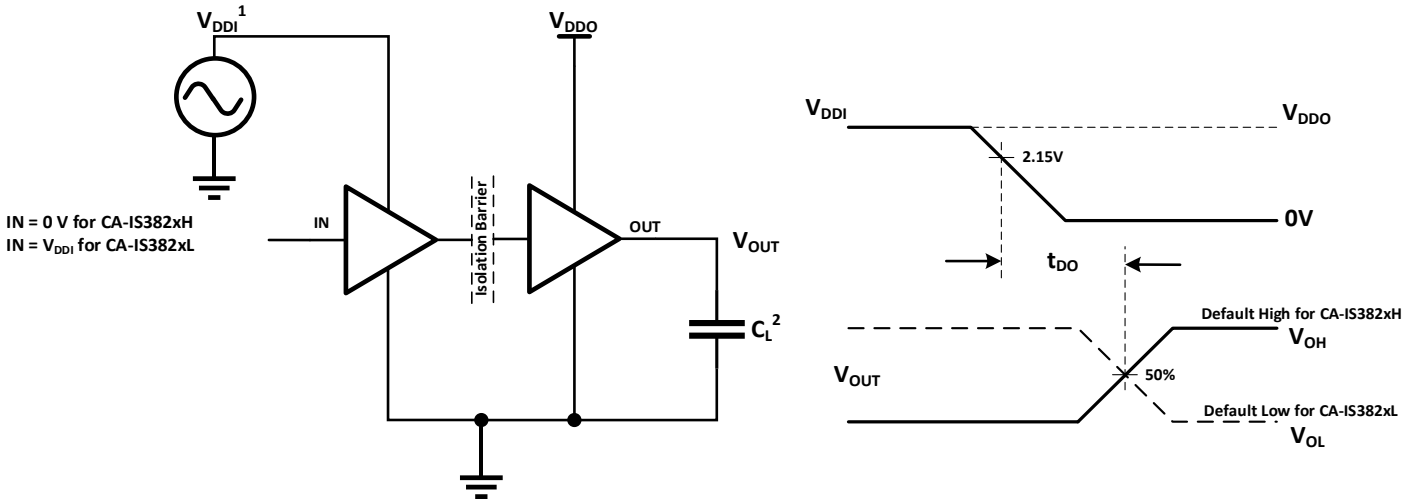
8. Parameter Measurement Information



NOTE:

1. A square wave generator generate the V_{IN} input signal with the following constraints: waveform frequency ≤ 100kHz, 50% duty cycle, t_r≤3ns, t_f≤3ns. Since the waveform generator has an output impedance of Z_{out} = 50Ω, the 50Ω resistor in the figure is used for matching. There is no need in the actual application.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

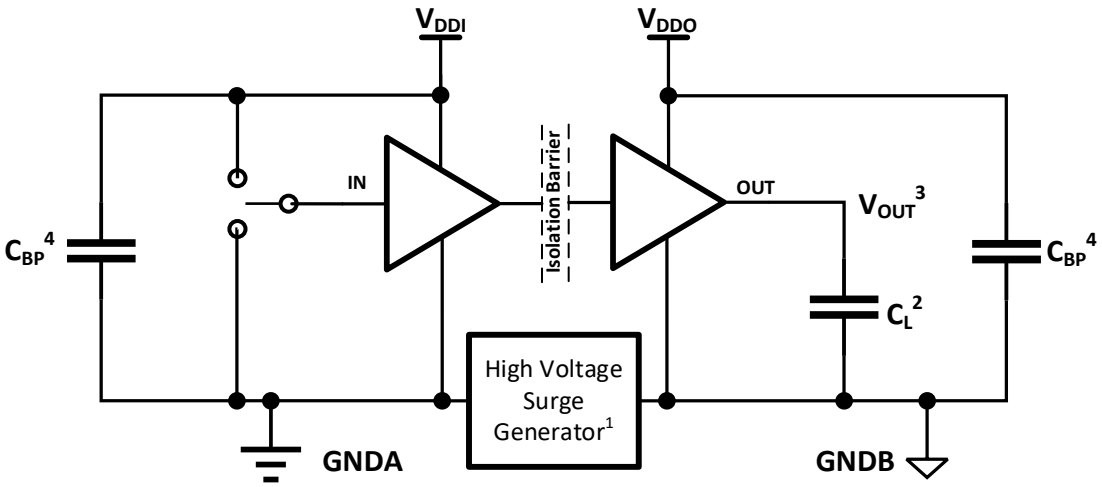
Figure 8-1 Timing Characteristics Test Circuit and Voltage Waveforms



NOTE:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DDI} should ramp over 2.375V but no higher than 5.5V.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-2 Default Output Delay Time Test Circuit and Voltage Waveforms



NOTE:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude and <10ns rise time and fall time to reach common-mode transient noise with > 150kV/μs slew rate.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance.
3. Pass-fail criteria: The output must remain stable whenever the high voltage surges come.
4. C_{BP} is the 0.1 ~ 1uF bypass capacitance.

Figure 8-3 Common-Mode Transient Immunity Test Circuit

9. Detailed Description

9.1. Theory of Operation

The CA-IS38xx family of devices use a simple ON-OFF keying (OOK) modulation scheme to transmit signal across the SiO_2 isolation capacitors that provide a robust insulation between two different voltage domain and act as a high frequency signal path between the input and the output. The transmitter (TX) modulates the input signal onto the carrier frequency, that is, TX delivers high frequency signal across the isolation barrier in one input state and delivers no signal across the barrier in the other input state. Then the receiver rebuilds the input signal according to the detected in-band energy. This simple architecture offers a robust isolated data path and requires no special considerations or initialization at start-up. The capacitor-based signal path is fully differential to maximize noise immunity, which is also known as common-mode transient immunity. Advanced circuitry techniques are applied for better EMI introduced by the carrier signal and IO switching. The capacitively-coupled architecture provides much higher electromagnetic immunity compared to the inductively-coupled one. And OOK modulation scheme eliminates the missing-pulse error that occurs in the pulse modulation method. A simplified functional block diagram and conceptual operation waveforms of a single channel is shown in Figure 9-1 and Figure 9-2.

9.2. Functional Block Diagram

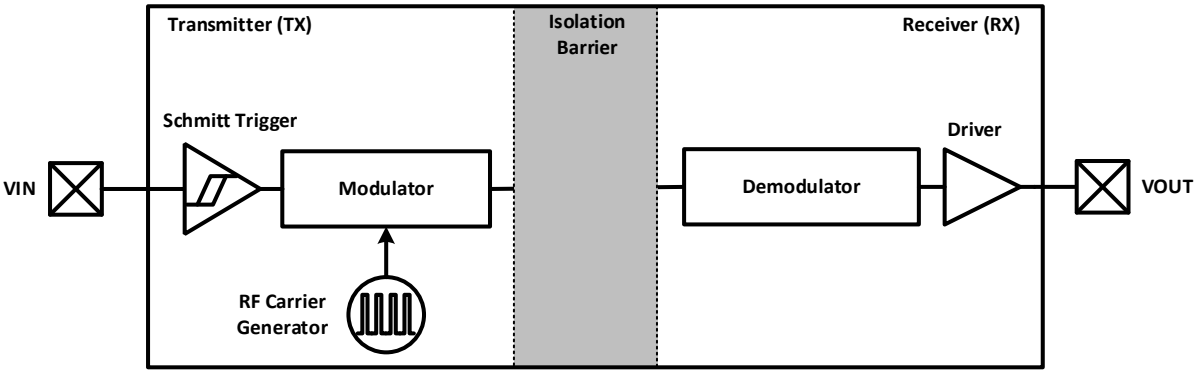


Figure 9-1 Functional Block Diagram of a Single Channel

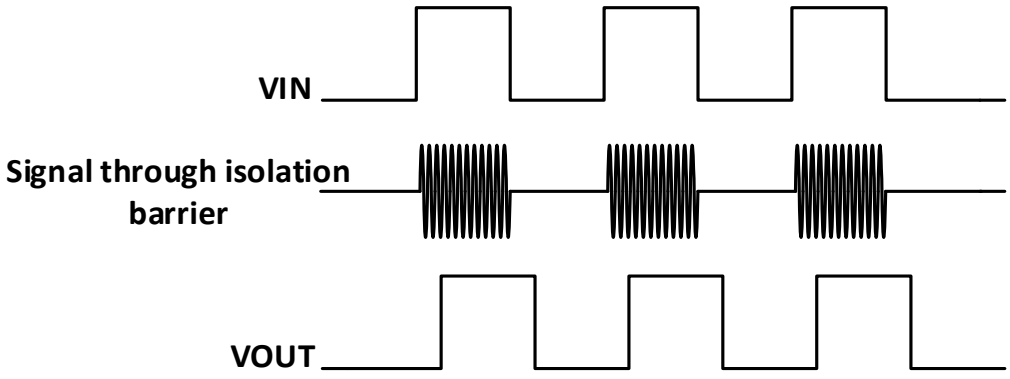


Figure 9-2 Conceptual Operation Waveforms of a Single Channel

9.3. Device Operation Modes

Table 9- 1 provides the operation modes for the CA-IS382x devices.

Table 9- 1 Operation Mode Table[1]

V_{DDI}	V_{DDO}	INPUT(Ax/Bx)[2]	OUTPUT (Ax/Bx)	OPERATION	V_{DDI}
PU	PU	H	H or NC	H	Normal operation mode: A channel's output follows the input state
		L	H or NC	L	
		Open	H or NC	Default	Default output fail-safe mode: If a channel's input is left open, its output goes to the default value (Low for CA-IS382xL and High for CA-IS382xH).
X	PU	X	L	Z	High impedance： If Enable pin is low, output is high impedance
PD	PU	X	H or NC	Default	Default output fail-safe mode: If the input side VDD is unpowered, the outputs go to the default output fail-safe mode (Low for CA-IS382xL and High for CA-IS382xH)
X	PD	X	X	Undetermined	If the output side V_{DD} is unpowered, the outputs' states are undetermined [5]

Note:
1. V_{DDI} = Input-side V_{DD}; V_{DDO} = Output-side V_{DD}; PU = Powered up (VCC ≥ 2.375 V); PD = Powered down (VCC ≤ 2.25 V); X = Irrelevant; H = High level; L = Low level; Z = High impedance
2. A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output
3. When CA-IS382x working in a noisy environment, EN pin is recommend to tie to external High or Low
4. NC, not connected. Could be floating, or tied to V_{DD} or GND
5. The outputs are in undetermined state when 2.25V < V_{DDI}, V_{DDO} < 2.375V

Table 9-1 EN Pin Truth Table

Part No.	ENA[1,2]	ENB[1,2]	Status
CA-IS3820	—	H	Enable VO1, VO2 output channel， output status follow input status
	—	L	Disable VO1, VO2 output channel ， output high Impedance
CA-IS3821	H	X	Enable VO1 output channel，output status follow input status
	L	X	Disable VO1 output channel ， output high Impedance
	X	H	Enable VO1 output channel，output status follow input status
	X	L	Disable VO1 output channel ， output high Impedance
CA-IS3822	H	X	Enable VO1 output channel，output status follow input status
	L	X	Disable VO1 output channel ， output high Impedance
	X	H	Enable VO2 output channel，output status follow input status
	X	L	Disable VO2 output channel ， output high Impedance

Note:
1. ENA/ENB could be used as MUX, clock sync and output control. Table 9-2 lists the logic control combination of ENA/ENB of each part. These pins are connected to local supply and allow to connect to external supply or floating. For better EMI immunity, when the isolation device working in a noisy environment, ENA/ENA should be tied to external logic high or low if not used.
2. X =Irrelevant; H =High Level; L = Low Level

10. Application and Implementation

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, the CA-IS382x family device CMOS digital isolator needs only two external VDD bypass capacitors (0.1μF to 1 μF) to operate. Its TTL level compatible input terminals draw only micro amps of leakage current, allowing them to be driven without external buffering circuits. The output terminals have a characteristic impedance of 50 Ω (rail-to-rail swing) and are available in both forward and reverse channel configurations. Figure 10-1 shows the typical application schematic of CA-IS3821. And the circuit of Figure 10-2 is typical for most applications of CA-IS38xx series products and is as easy to use as a standard logic gate.

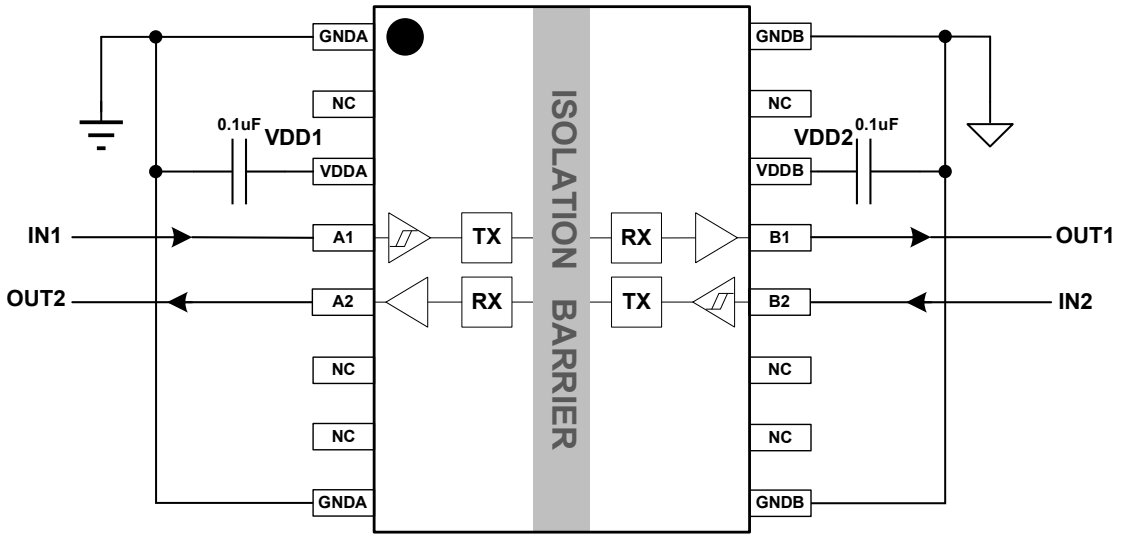


Figure 10-1 CA-IS3821 Digital Isolator Application Schematic

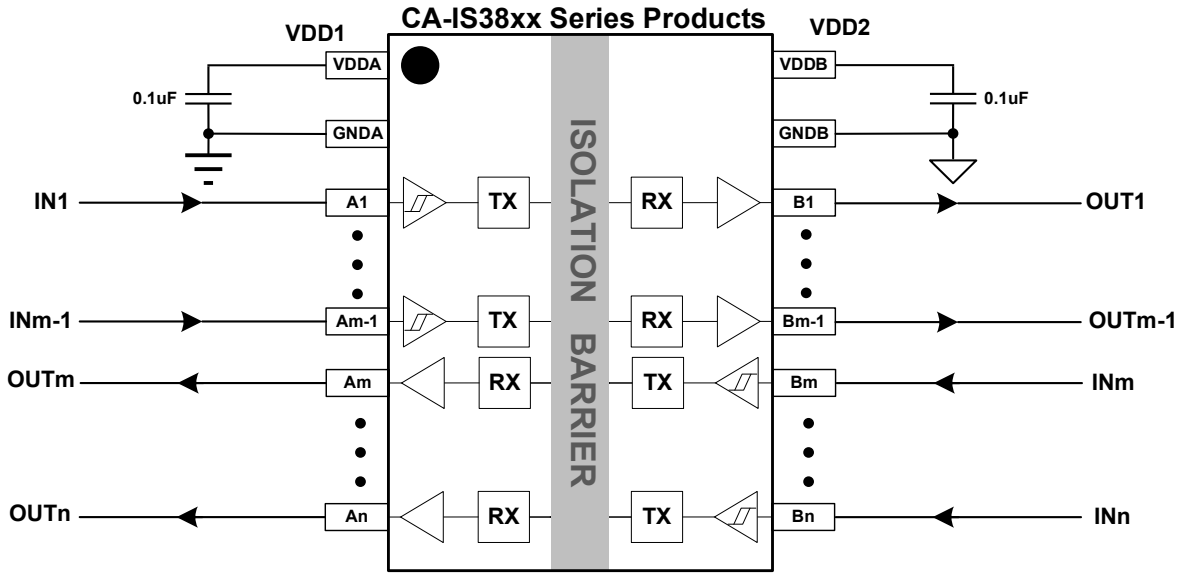
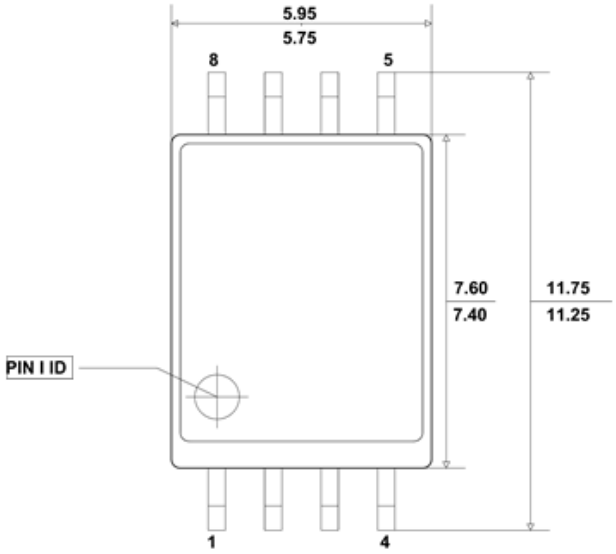


Figure 10-2 CA-IS38xx Series Digital Isolator Application Schematic

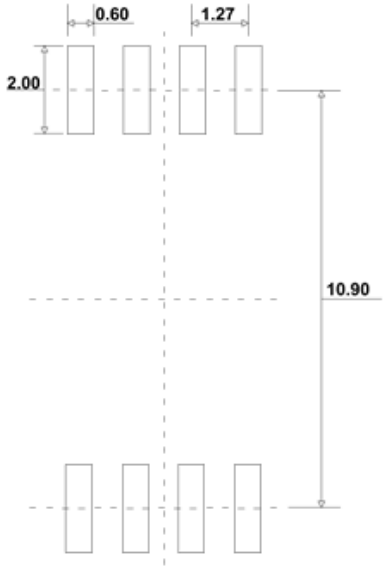
11. Package Information

11.1 SOIC8 wide body package

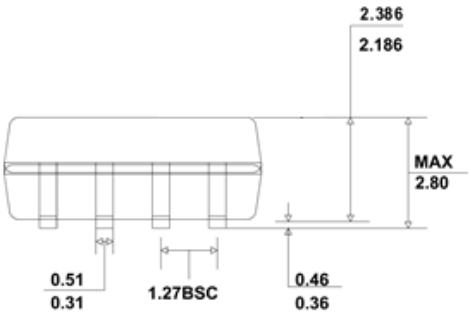
The figure below illustrates the package details and the recommended land pattern details for the CA-IS382x digital isolator in a 8-pin wide body SOIC package. The values for the dimensions are shown in millimeters



TOP VIEW



RECOMMENDED LAND PATTERN

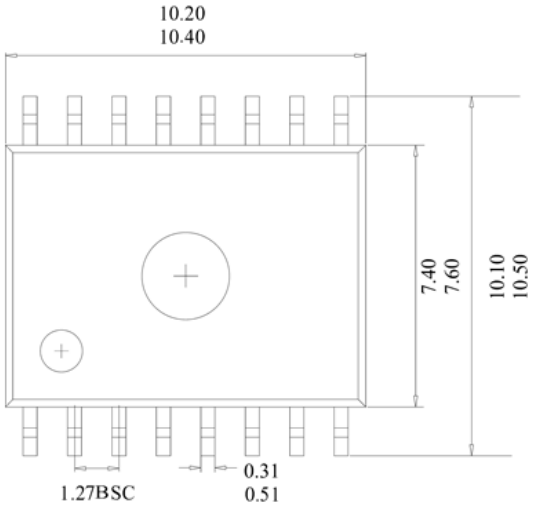


FRONT VIEW

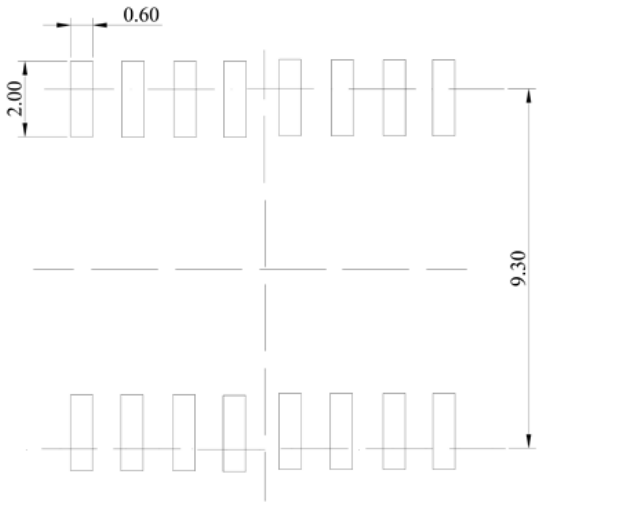
LEFT-SIDE VIEW

11.2 SOIC16 wide body package

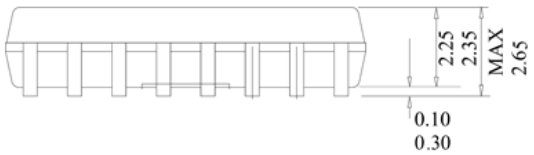
The figure below illustrates the package details and the recommended land pattern details for the CA-IS382x digital isolator in a 16-pin wide body SOIC package. The values for the dimensions are shown in millimeters



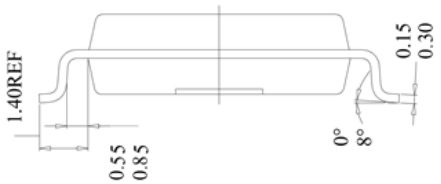
TOP VIEW



RECOMMENDED LAND PATTERN



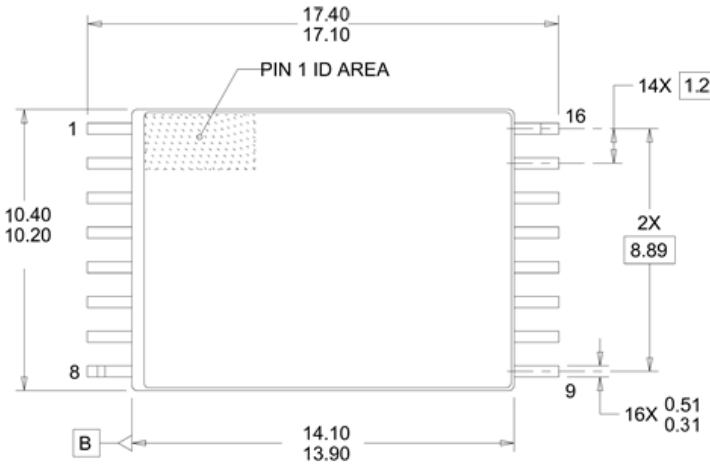
FRONT VIEW



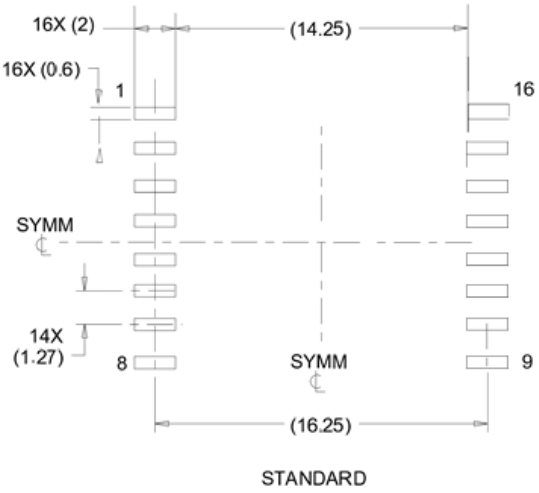
SIDE VIEW

11.3 16-Pin Extra Wide Body SOIC Package

The figure below illustrates the package details and the recommended land pattern details for the CA-IS382x digital isolator in a 16-pin extra wide body SOIC package. The values for the dimensions are shown in millimeters.



TOP VIEW



STANDARD
RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

12 Soldering Information

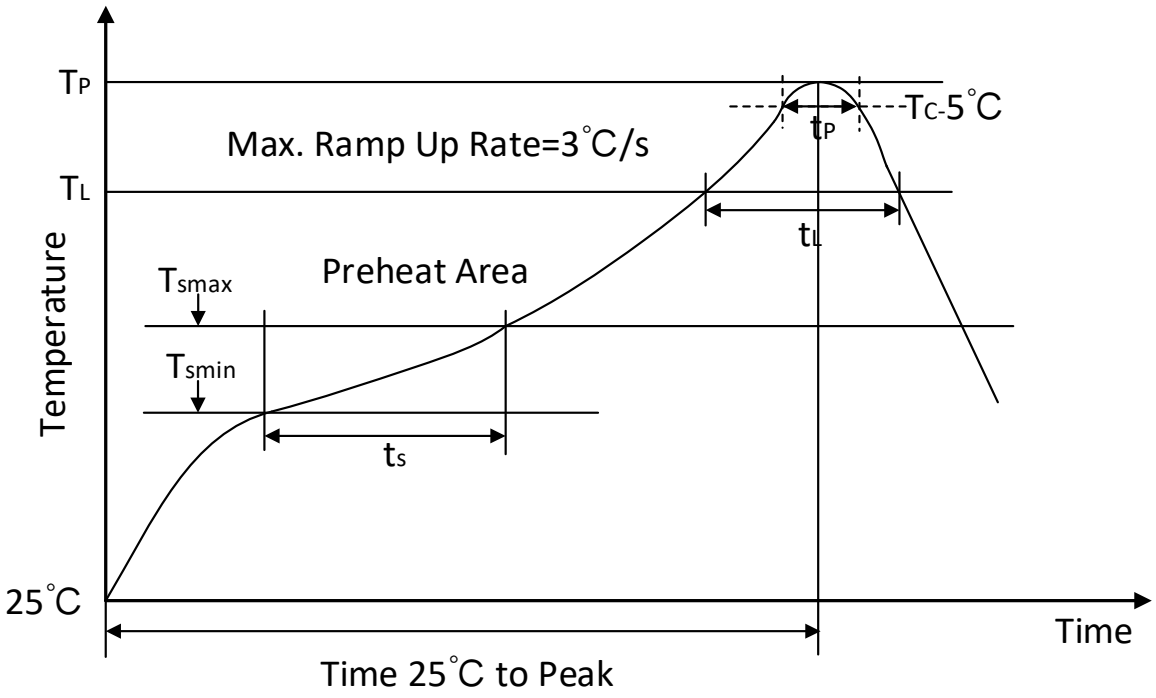


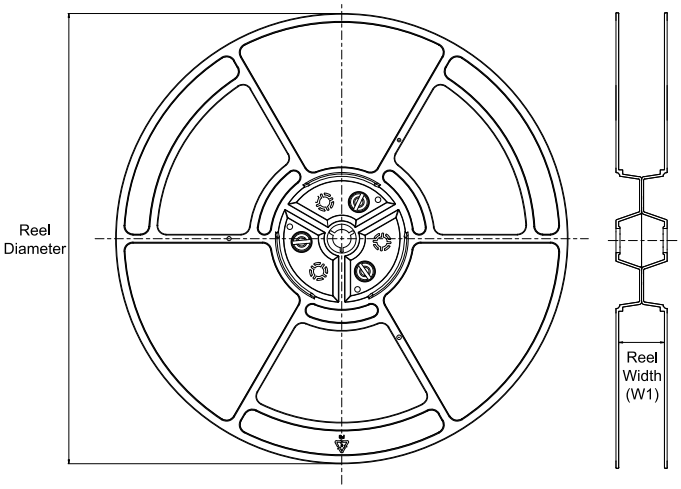
Figure12- 1 Soldering Temperature (reflow) Profile

Table12- 1 Soldering Temperature Parameter

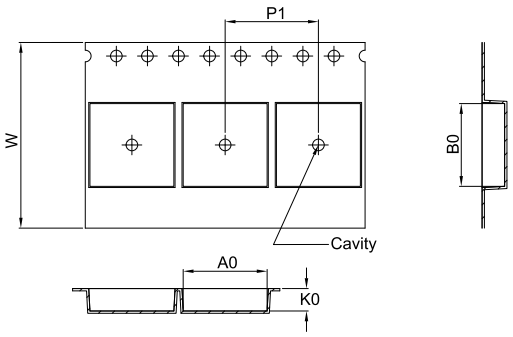
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 ℃ to Peak)	3℃ /second max
Time of Preheat temp(from 150 ℃ to 200 ℃)	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5℃ of actual peak temp	30 second
Ramp-down rate	6 ℃ /second max.
Time from 25℃ to peak temp	8 minutes max

13 Tape And Reel Information

REEL DIMENSIONS

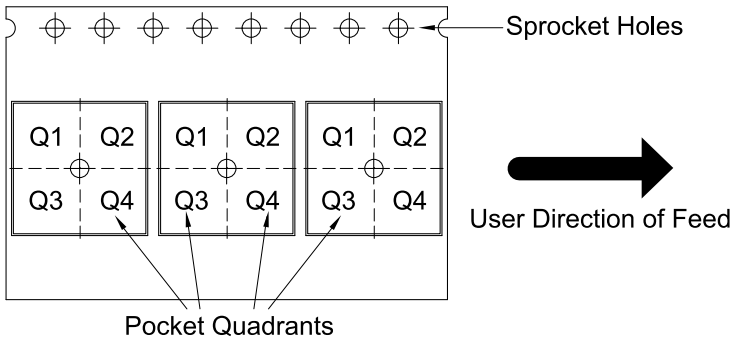


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3820LG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.2	16.0	16.0	Q1
CA-IS3820LW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3820LWW	SOIC	WW	16	1000	330	24.4	17.6	10.8	3.0	20.0	24.0	Q1
CA-IS3820HG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.2	16.0	16.0	Q1
CA-IS3820HW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3820HWW	SOIC	WW	16	1000	330	24.4	17.6	10.8	3.0	20.0	24.0	Q1
CA-IS3821LG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.2	16.0	16.0	Q1
CA-IS3821LW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3821LWW	SOIC	WW	16	1000	330	24.4	17.6	10.8	3.0	20.0	24.0	Q1
CA-IS3821HG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.2	16.0	16.0	Q1
CA-IS3821HW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3821HWW	SOIC	WW	16	1000	330	24.4	17.6	10.8	3.0	20.0	24.0	Q1
CA-IS3822LG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.2	16.0	16.0	Q1
CA-IS3822LW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3822LWW	SOIC	WW	16	1000	330	24.4	17.6	10.8	3.0	20.0	24.0	Q1
CA-IS3822HG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.2	16.0	16.0	Q1
CA-IS3822HW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3822HWW	SOIC	WW	16	1000	330	24.4	17.6	10.8	3.0	20.0	24.0	Q1

14 Important Notice

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